4-LVPECL Output Ultra-Low Additive Jitter/Differential Clock Buffer

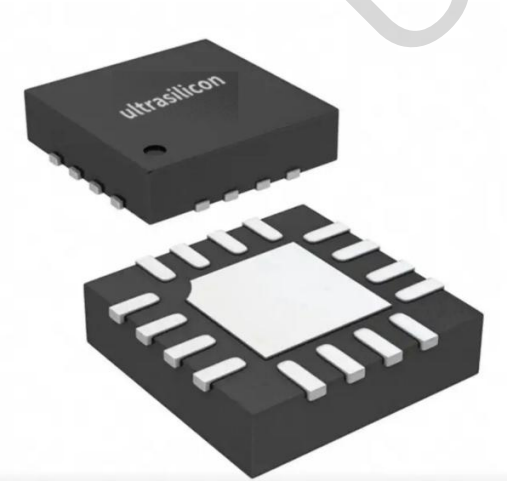
US5D1204P
Datasheet

Description

The US5D1204P is a 2-GHz,4-output differential high-performance clock fanout buffer.

The US5D1204P is a highly versatile, low additive jitter buffer that can generate four copies of LVPECL clock outputs from one of two selectable LVPECL,and LVDS, or LVCMOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.



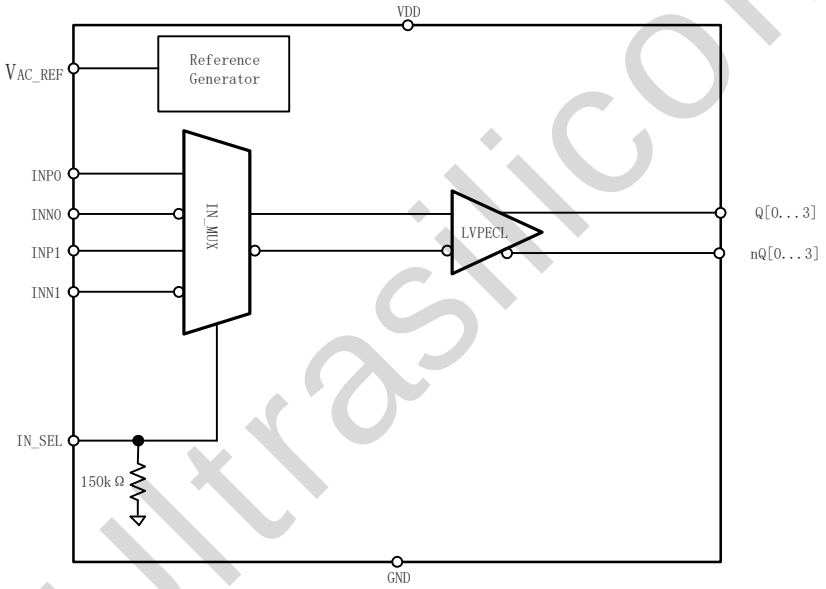
Features

- 2:4 Differential Buffer
- Universal Input Accept LVPECL,LVDS and LVCMOS/LVTTL
- Four LVPECL output
- Maximum Output Frequency LVPECL - 2-GHz
- Maximum Propagation Delay:500 ps(typical)
- Output skew: 20 ps (typical)
- Part-to-part skew< 300ps
- Additive RMS phase jitter @ 156.25MHz: 38fs RMS (12kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage : VDD= 3.3V or 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-16 package

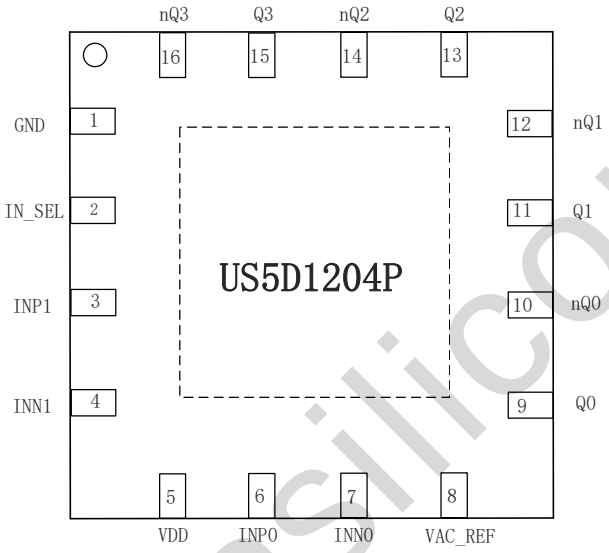
Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Block Diagram



Pin Assignment for QFN-16 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
2	IN_SEL	Input	Input selection with an internal 150-kΩ pulldown, selects input port.
3	INP1	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
4	INN1	Input	Differential input pair.
5	VDD	Power	2.5-V and 3.3-V supply for the core.
6	INP0	Input	Differential input pair or single-ended input. Unused input pair can be left floating
7	INN0	Input	Differential input pair.
8	VAC_REF	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1-μF to GND on this pin.
9	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating
10	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating
11	Q1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating
12	nQ1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating
13	Q2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating
14	nQ2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating
15	Q3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating
16	nQ3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating

Table 2: Input Selection Table

IN_SEL	CLOCK INPUT
0	INP0,INN0
1	INP1,INN1

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

Electrical Characteristics(INPUT)

At VCC = 2.375 V to 3.6 V and TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
LVCMOS input						
FIN	Input Frequency	VDD=3.3V	0.1		250	MHz
Vth	Input threshold voltage	External threshold voltage applied to complementary input.	1.1		1.8	V
VIH	Input high voltage		1.2		VDD	V
VIL	Input low voltage		0		1.7	V
IIH	Input high current	VDD = 3.6 V, VIH = 3.6 V			100	μA
IIL	Input low current	VDD = 3.6 V, VIL = 0 V			-100	μA
ΔV/ΔT	Slew rate	20% to 80%	1.5			V/ns
C_{IN}	Input capacitance			2.5		pF
Differential Input						
FIN	Input frequency	VDD=3.3V	0.1		2000	MHz
$V_{IN,DIFF,PP}$	Differential input peal-peak voltage	FIN ≤ 1.5 GHz	0.1		1.5	V
		1.5 GHz ≤ FIN ≤ 2 GHz	0.2		1.5	V
V_{ICM}	Input common-mode level		1		VDD-0.3	V
IIH	Input high current	VDD = 3.6 V, VIH = 3.6 V			100	μA
IIL	Input low current	VDD = 3.6 V, VIL = 0 V			-100	μA
ΔV/ΔT	Slew rate	20% to 80%	1.5			V/ns
C_{IN}	Input capacitance			2.5		pF

Electrical Characteristics(OUTPUT)

VCC = 2.375 V to 2.625 V; TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

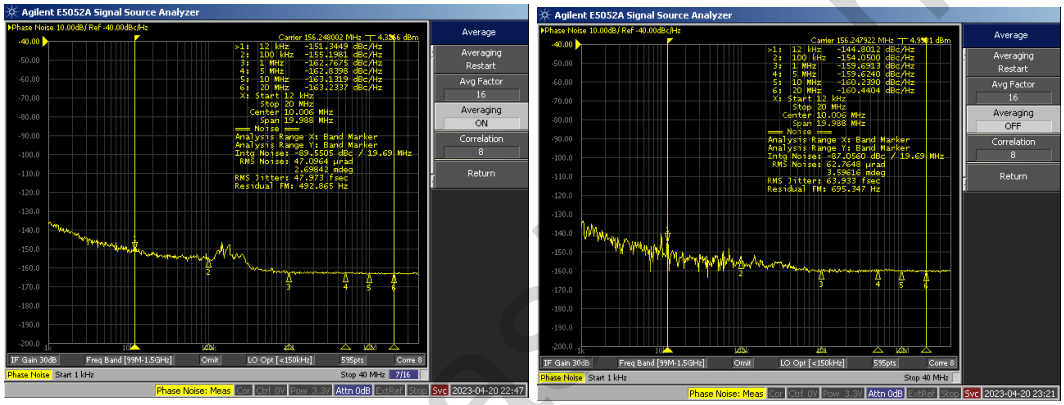
Parameter		Test Conditions	Min	Typ	Max	Unit
LVPECL Output						
VOH	Output high voltage		VDD-1.2		VDD-0.9	V
VOL	Output low voltage		VDD-1.7		VDD-1.3	V
$V_{OUT,DIFF,PP}$	Differential output peak-peak voltage	FIN ≤ 2 GHz		1.15		V
V_{AC_REF}	Output bias voltage		VDD-1.6		VDD-1.1	V
t_{PD}	Propagation delay			0.5	1.5	ns
$t_{SK,PP}$	Part-to-part skew				300	ps
$t_{SK,O}$	Output skew			20	50	ps
$T_{sk,p}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, F_{OUT}=100MHz	-50		50	ps
t_{RJIT}		Additive RMS phase jitter @ 156.25MHz: (12kHz - 20MHz)		47	70	fs
t_R/t_F	Output rise/fall time	20% to 80%			500	ps

Tip:Internally generated bias voltage (VAC_REF) is for 3.3 V operation only. It is recommended to apply externally generated bias voltage for VCC < 3 V.

VCC = 3.125 V to 3.6 V; TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
LVPECL Output						
VOH	Output high voltage		VDD-1.2		VDD-0.9	V
VOL	Output low voltage		VDD-1.7		VDD-1.3	V
$V_{OUT,DIFF,PP}$	Differential output peak-peak voltage	FIN ≤ 2 GHz	0.65		1.35	V
V_{AC_REF}	Output bias voltage		VDD-1.6		VDD-1.1	V
t_{PD}	Propagation delay			0.5	1.5	ns
$t_{SK,PP}$	Part-to-part skew				300	ps
$t_{SK,O}$	Output skew				50	ps
$T_{sk,p}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion, F_{OUT}=100MHz	-50		50	ps
t_{RJIT}		Additive RMS phase jitter @ 156.25MHz: (12kHz - 20MHz)		38	70	fs
t_R/t_F	Output rise/fall time	20% to 80%			500	ps

PHASE JITTER



(a)Jitter_Source **(b)3V3_156M25_LVPECL**

Figure 1 .RMS_Jitter_3V3=Sqrt(64^2-48^2)=38fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

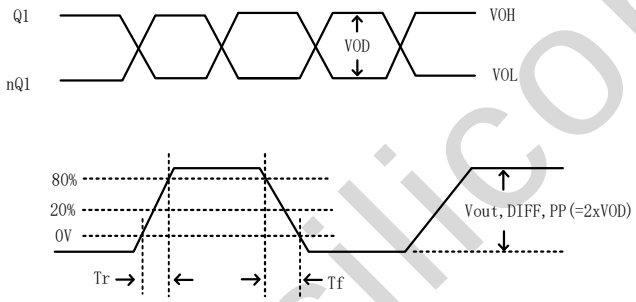
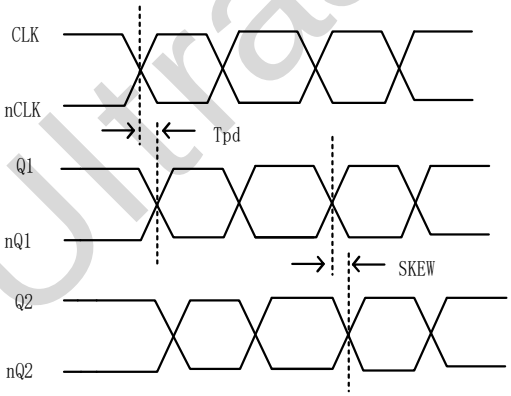


Figure 2.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 3.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

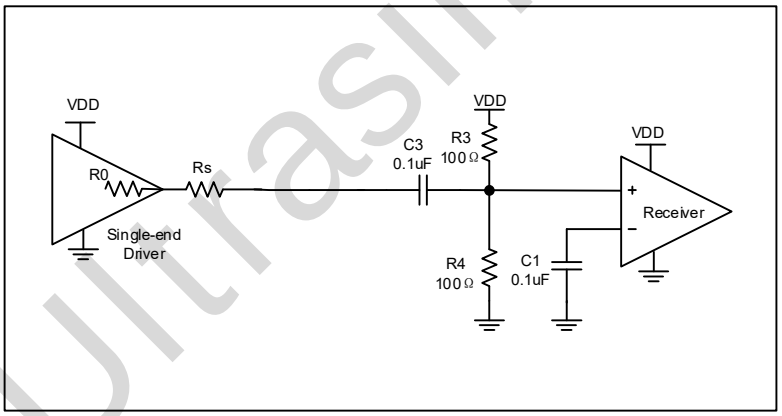
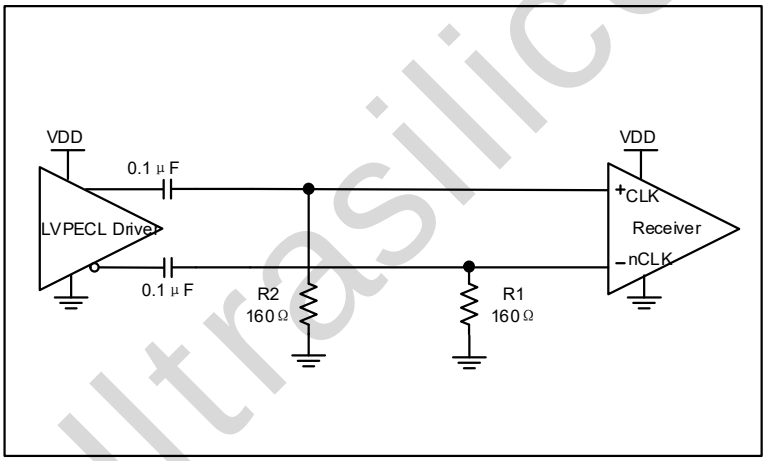
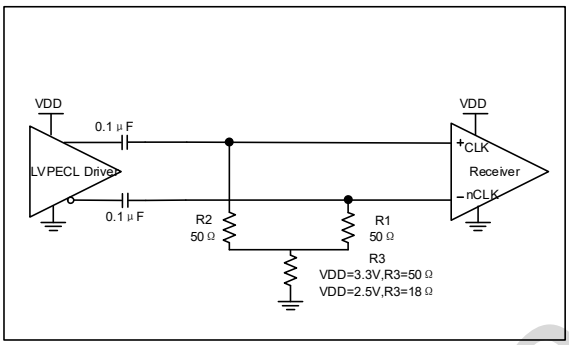


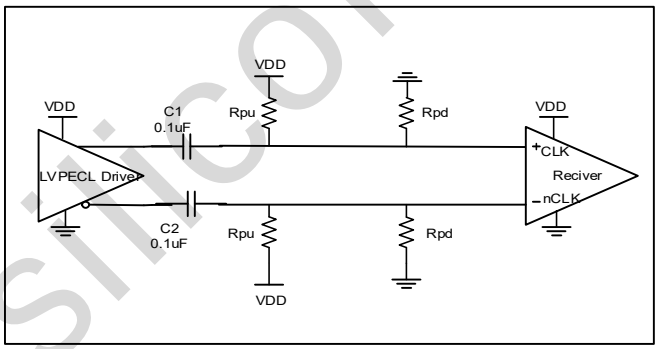
Figure4.Single-termination method of differential input

Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure5 to Figure9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

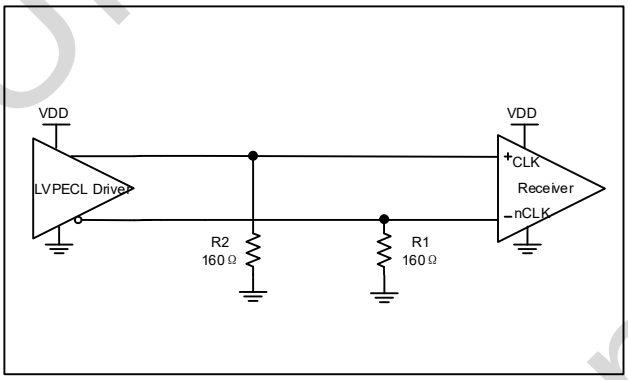


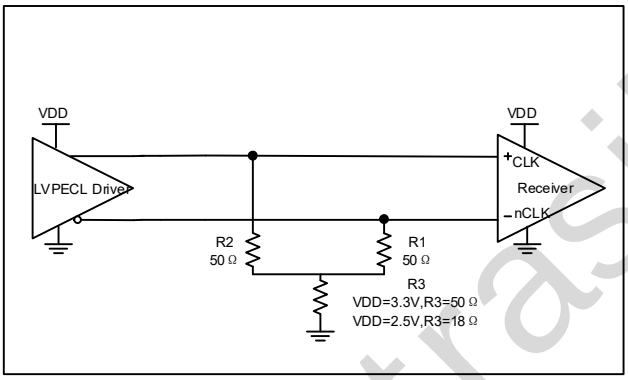


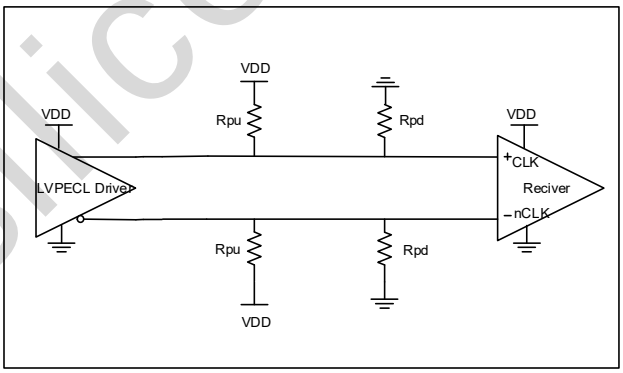


VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure5.LVPECL Driver(AC)

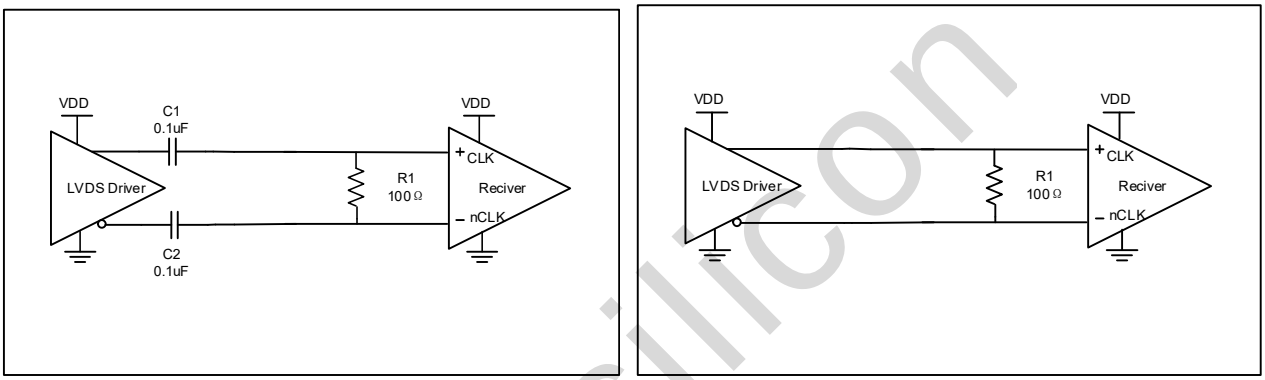






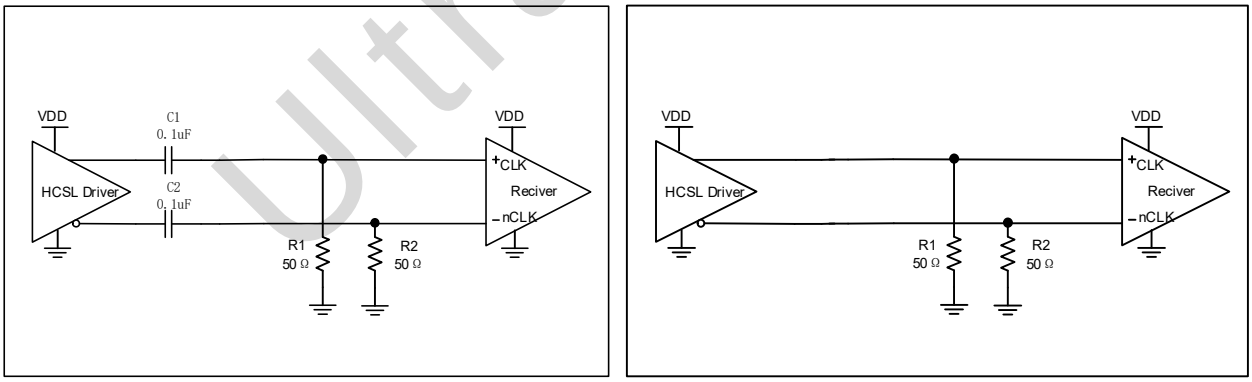
VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure6.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

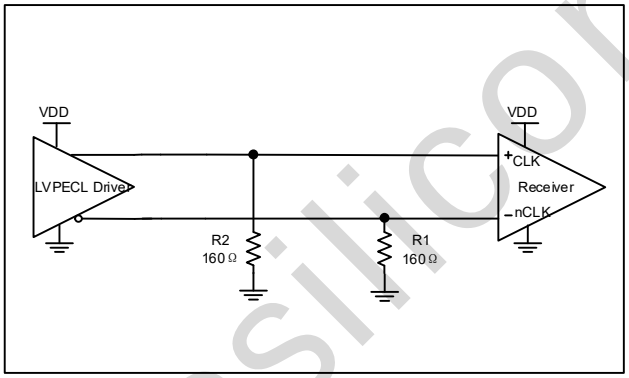
Figure7.LVDS Driver

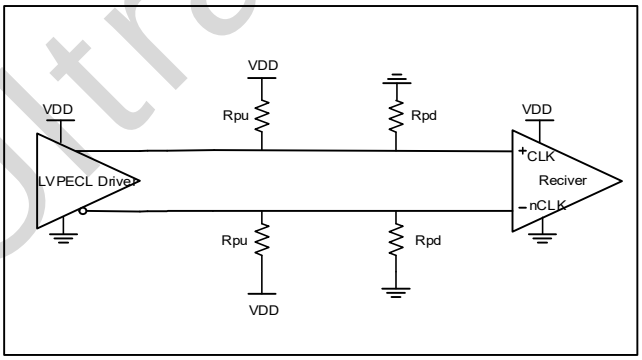


a)AC coupling **b)DC coupling**

Figure8.HCSL Driver

Output connection circuit





VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

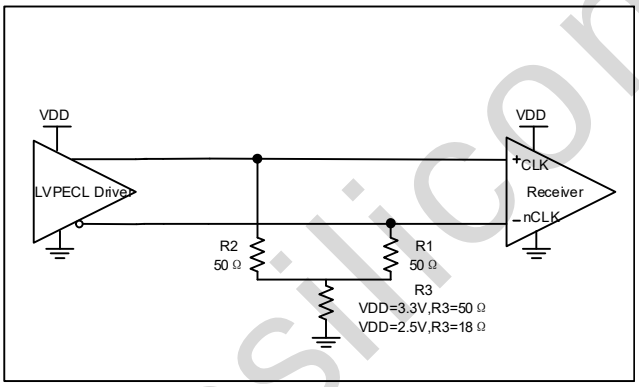
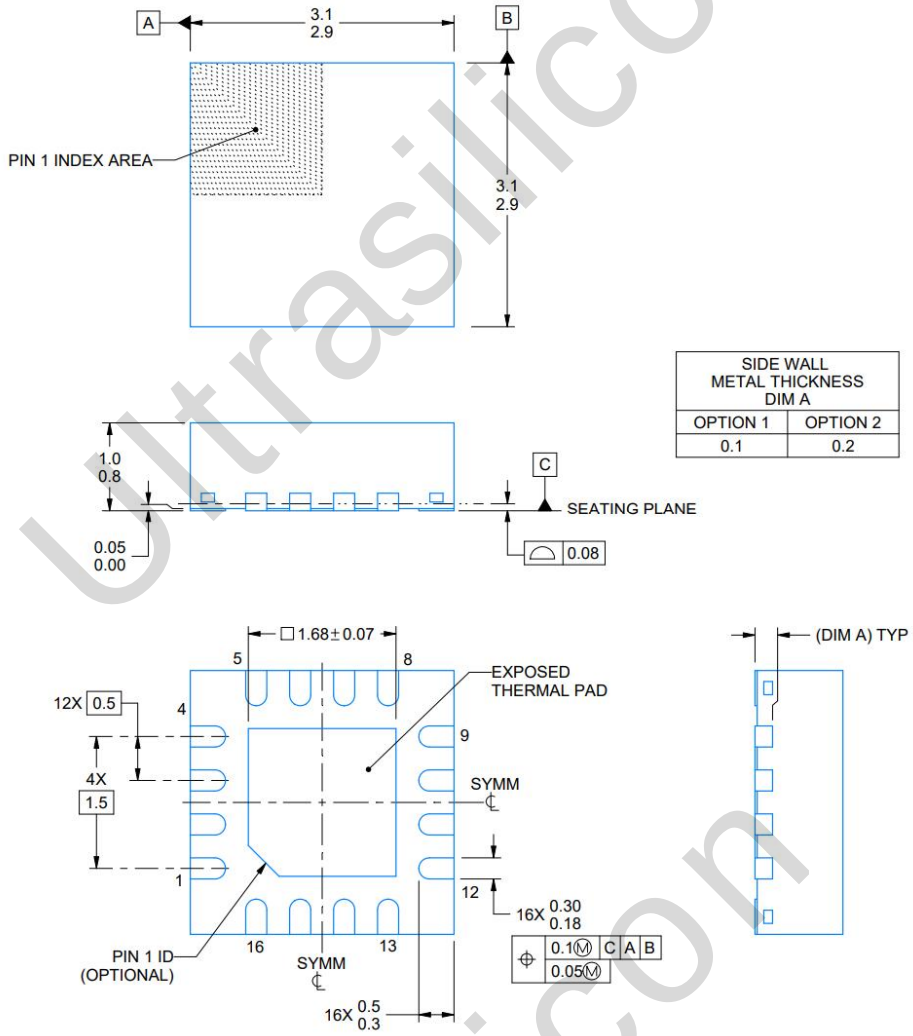


Figure9.LVPECL Driver

PACKAGE DIMENSIONS(QFN-16)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.20	0.30	0.40
A3	-	0.20Ref	-	aaa	0.05		
b	0.20	0.25	0.30	bbb	0.10		
D	3.00BSC			ccc	0.10		
E	3.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	1.60	1.70	1.80				
E2	1.60	1.70	1.80				

Reflow profile

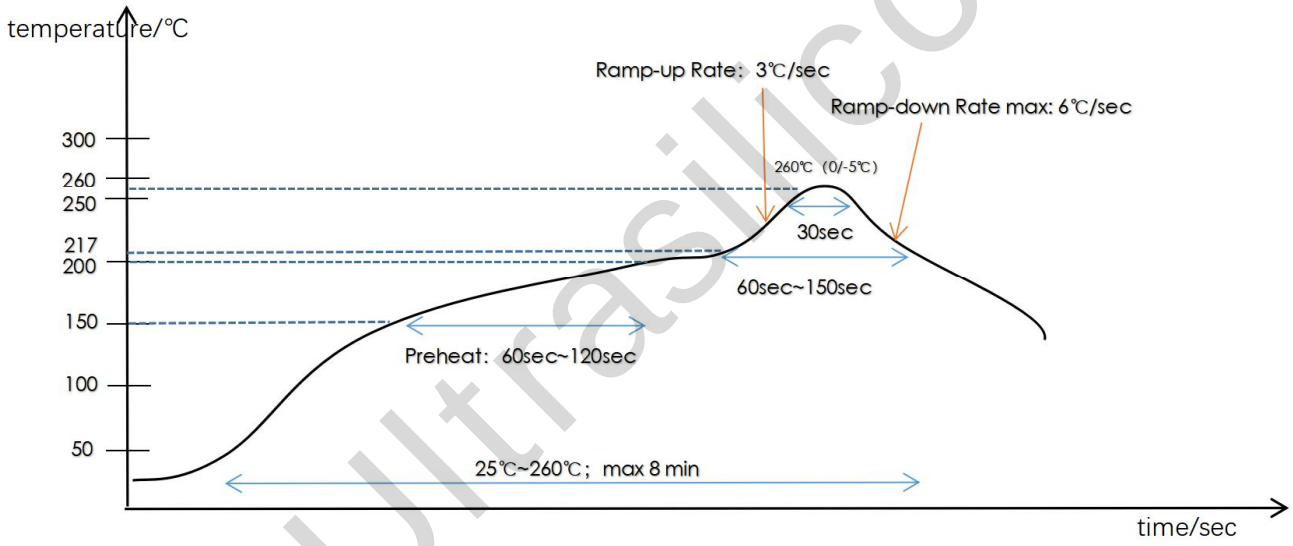


Figure10: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.12.26	First Draft.	1.0
2023.4.3	Update electrical performance parameters and Matching circuit diagram.	1.5
2023.5.11	Update Timing Diagrams and input selecton.	2.0
2023.8.8	Update the pin definition.	2.5
2025.7.10	Update the current Characteristics.	3.0