ZDV4(5)256M16

4Gb DDR3(L) SDRAM Datasheet

Key Features

●VDD=VDDQ=1.5V(1.425V~1.575V)

VDD=VDDQ=1.35V(1.28V~1.45V)，backward compatible to 1.5V applications.

- 8 banks
- 8n-bit prefetch architecture
- Fully differential clock inputs (CK,$\overline{CK}$) operation
- Bi-directional differential data strobe (DQS,$\overline{DQS}$)
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition With CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13, 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9, 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Driver strength selected by MRS
- Dynamic On Die Termination
- Asynchronous RESET pin
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- TDQS (Termination Data Strobe) supported (x8 only)
- Write leveling
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- JEDEC standard package
  - 96ball FBGA(x16)
- Lead free & RoHS compliant
- JEDEC compliant
- Operating Temperature (Tcase)
  - Commercial -C (0°C ≤ T_C ≤ 95°C)- Industrial -I (-40°C ≤ T_C ≤ 95°C)

Speed	1600	1866	2133	Unit
	11-11-11	13-13-13	14-14-14	
tCK(min)	1.25	1.071	0.938	ns
CAS Latency	11	13	14	nCK
tRCD(min)	13.75	13.91	13.09	ns
tRP(min)	13.75	13.91	13.09	ns
tRAS(min)	35	34	33	ns
tRC(min)	48.75	47.91	46.09	ns

Note:
The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Descriptions

The 4Gb Double-Data-Rate-3 (DDR3(L)) DRAM is a high-speed CMOS SDRAM. It is internally configured as an octal-bank DRAM.

The 4Gb chip is organized as 32Mbit x16 I/O x 8 banks. These synchronous devices achieve high speed double-data-rate transfer rates of up to 2133 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3(L) DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V or 1.35V -0.067V/+0.1V power supply and are available in BGA packages.

Addressing

Configuration	512Mb x 8	256Mb x 16
Number of Bank	8	8
Bank address	BA0-BA2	BA0-BA2
Autoprecharge	A10/AP	A10/AP
Row address	A0-A15	A0-A14
Column address	A0-A9	A0-A9
BC switch on the fly	A12/$\overline{BC}$	A12/$\overline{BC}$
Page Size	1KB	2KB
tREFI	Tc ≤ 85°C : 7.8μs, 85°C < Tc ≤ 105°C : 3.9μs	
tRFC	260ns	

Package

4Gb (Org. / Package)		Dimension (mm)	Ball pitch (mm)
512Mbx8	78-ball FBGA	9 x 10.6	0.80
256Mbx16	96-ball FBGA	9 x 13	0.80
256Mbx16	96-ball FBGA	8 x 14	0.80

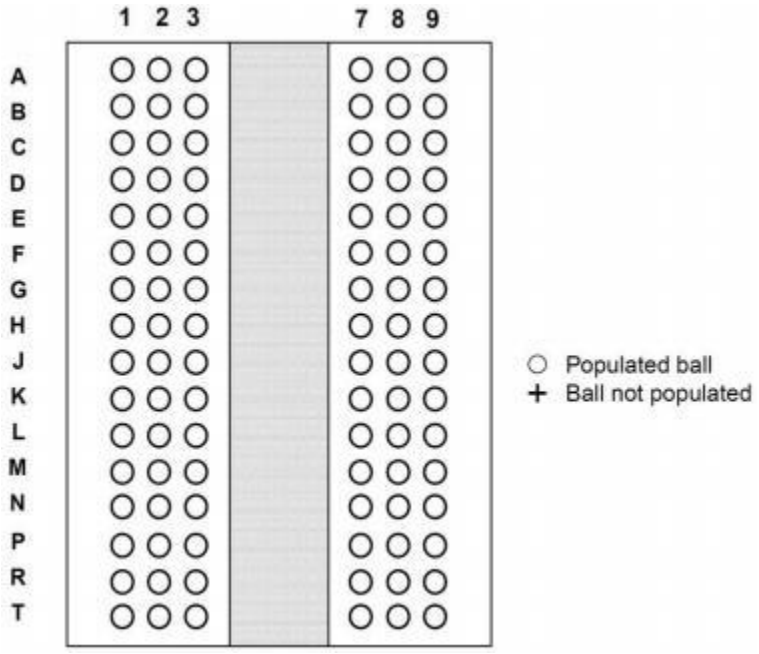
Ordering Information

Organization	Part No.	Speed			Package
		Clock (MHz)	Data Rate (Mb/s)	CL-TRCD-TRP	
DDR3(L) Commercial Grade (-C)					
256Mx16	ZDV4256M16A-14DPH	1066	DDR3L-2133	14-14-14	96-ball
	ZDV4256M16A-13DPH	933	DDR3L-1866	13-13-13	
	ZDV4256M16A-11DPH	800	DDR3L-1600	11-11-11	
	ZDV5256M16A-14DPH	1066	DDR3-2133	14-14-14	
	ZDV5256M16A-13DPH	933	DDR3-1866	13-13-13	
	ZDV5256M16A-11DPH	800	DDR3-1600	11-11-11	
	ZDV5256M16A-11DGN	800	DDR3-1600	11-11-11	
DDR3(L) Industrial Grade (-I)					
256Mx16	ZDV4256M16A-14IPH	1066	DDR3L-2133	14-14-14	96-ball
	ZDV4256M16A-13IPH	933	DDR3L-1866	13-13-13	
	ZDV4256M16A-11IPH	800	DDR3L-1600	11-11-11	
	ZDV5256M16A-14IPH	1066	DDR3-2133	14-14-14	
	ZDV5256M16A-13IPH	933	DDR3-1866	13-13-13	
	ZDV5256M16A-11IPH	800	DDR3-1600	11-11-11	

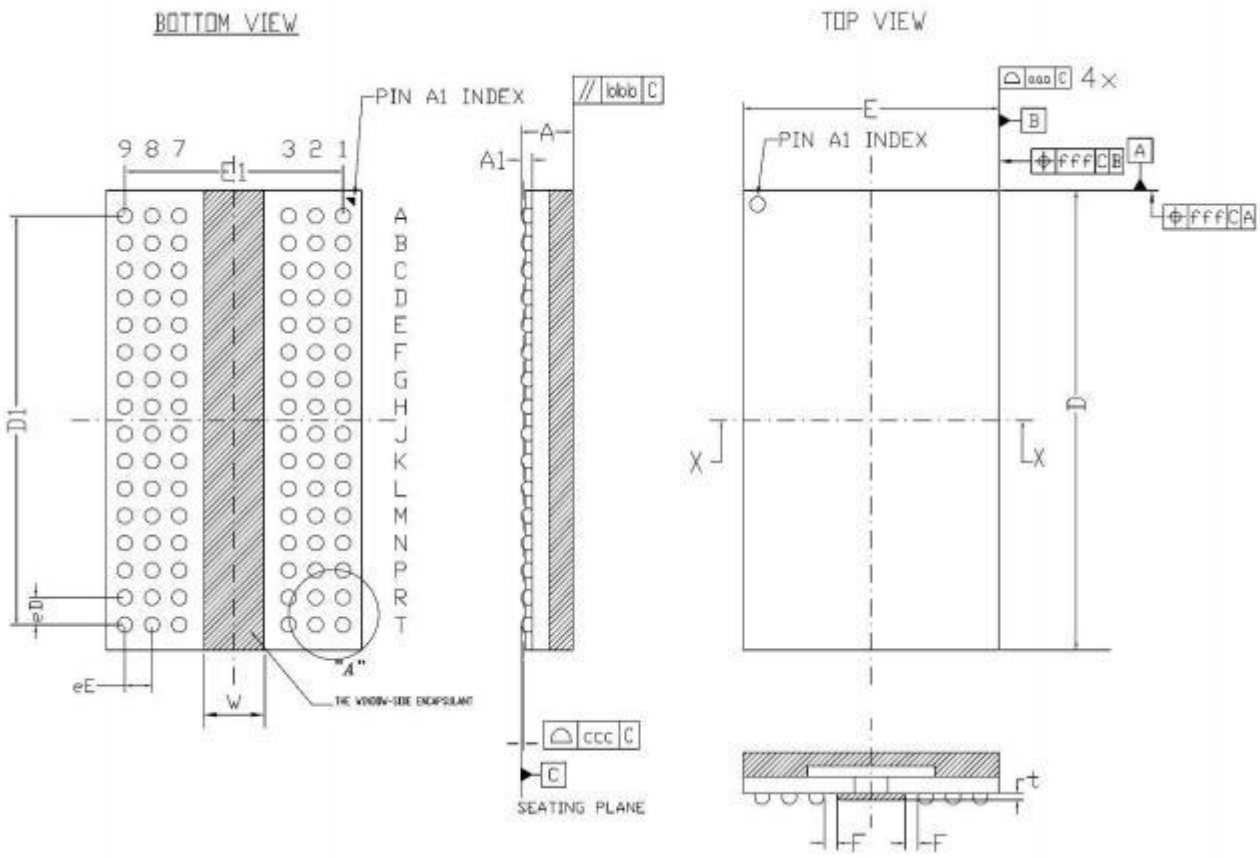
X16 Package Ballout (Top View): 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				$\overline{\text{DQSU}}$	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	$\overline{\text{DQSL}}$				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	J
K	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	K
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/$\overline{\text{BC}}$	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	$\overline{\text{RESET}}$	A13				A14	A8	VSS	T
	1	2	3	4	5	6	7	8	9	

Top View: See the balls through the Package

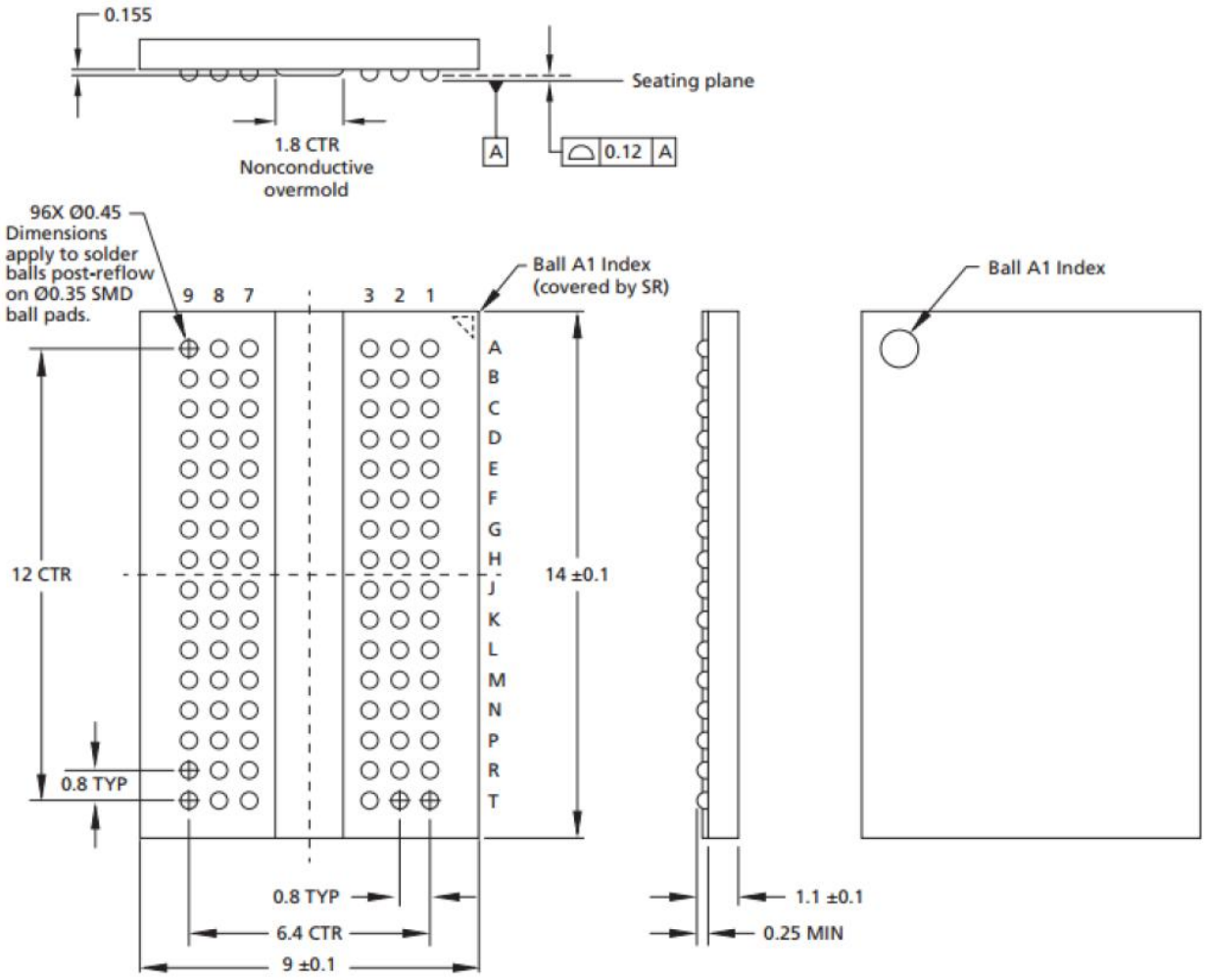


Packge Dimensions – 96 balls BGA Package (x16)



REF.	Dimension in mm		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.25	---	0.40
b	0.40	0.45	0.50
D	12.90	13.00	13.10
E	8.90	9.00	9.10
D1	12.00 BSC		
E1	6.40 BSC		
eE	0.80 BSC		
eD	0.80 BSC		
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.12
ddd	---	---	0.15
eee	---	---	0.08
F	0.1	---	---
t	---	---	0.20
W	---	---	2.00

96-ball (8mm x 14mm) GNF



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Pin Functions

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$
CKE	Input	Clock Enable: CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered high. provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (along with $\overline{CS}$) define the command being
DM, (DMU, DML)	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access.
BA0 ~ BA2	Input	Bank Address Inputs: BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A10 / AP	Input	Auto-Precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A0 ~ A15	Input	Address Inputs: Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12, $\overline{BC}$ have additional function as below.) The address inputs also provide the op-code during Mode Register Set commands.
A12, $\overline{BC}$	Input	Burst Chop: A12, $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped).
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM, $\overline{TDQS}$, NU, $\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT.

Symbol	Type	Function
$\overline{RESET}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V
DQ	Input/Output	Data Inputs/Output: Bi-directional data bus.
DQL, DQU, DQS, ($\overline{DQS}$) DQSL, ($\overline{DQSL}$), DQSU, ($\overline{DQSU}$)	Input/Output	Data Strobe: output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS, DQSL, DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$, $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS,($\overline{TDQS}$)	Output	TDQS and $\overline{TDQS}$ is applicable for ×8 configuration only. When enabled via mode register A11 = 1 in MR1, DRAM will enable the same termination resistance function on TDQS, $\overline{TDQS}$ as is applied to DQS, DQS. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and $\overline{TDQS}$ is not used.
NC	-	No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.35V -0.067V/+0.1V or 1.5V ± 0.075V
VDD	Supply	Power Supply: 1.35V -0.067V/+0.1V or 1.5V ± 0.075V
VSSQ	Supply	DQ Ground
VSS	Supply	Ground
VREFCA	Supply	Reference voltage for CA
VREFDQ	Supply	Reference voltage for DQ
ZQ	Supply	Reference pin for ZQ calibration.

Note: Input only pins (BA0-BA2, A0-A14, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$, do not supply termination.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameters	Rating	Unit	Note
VDD	Voltage on VDD pin relative to VSS	-0.4 ~ 1.8	V	1,3
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4 ~ 1.8	V	1,3
VIN, VOUT	Voltage on input/output pin relative to VSS	-0.4 ~ 1.8	V	1
TSTG	Storage Temperature	-55 ~ 100	°C	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.

3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

Refresh parameters by device density

Parameter	Symbol	1Gb	4Gb	4Gb	8Gb	Unit
REF command to ACT or REF command time	tRFC	110	160	260	350	ns

Temperature Range

Symbol	Parameters	Rating	Unit	Note
Commercial (-C)	Normal Operating Temperature Range	0 ≤ TOPER ≤ 85	°C	1
	Extended Temperature Range	85 < TOPER ≤ 95	°C	1,2
Industrial (-I)	Normal Operating Temperature Range	-40 ≤ TOPER ≤ 85	°C	1
	Extended Temperature Range	85 < TOPER ≤ 95	°C	1,2

Notes:

1. Operating Temperature Toper is the case surface temperature on the center/top side of the DRAM.
2. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional apply:
   a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameters		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
3. Maximum DC value may not be great than 1.425V. The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).
4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
5. Under these supply voltages, the device operates to this DDR3L specification.
6. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.
7. VDD= VDDQ= 1.35V (1.283–1.45V) Backward compatible to VDD= VDDQ= 1.5V ±0.075V Supports DDR3L devices to be backward com-partible in 1.5V applications.

IDD Specifications and Measurement Conditions

IDD Specifications (DDR3L)

Symbol	Parameter	Width	DDR3L-1600 11-11-11	DDR3L-1866 13-13-13	DDR3L-2133 14-14-14	Units
IDD0	Operating Current 0 One Bank Activate -> Precharge	x8	100	120	130	mA
		x16	110	130	150	mA
IDD1	Operating Current 1 One Bank Activate -> Read -> Precharge	x8	110	125	135	mA
		x16	120	135	155	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	x8	20	20	20	mA
		x16	22	22	22	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	x8	43	45	47	mA
		x16	45	47	49	mA
IDD2Q	Precharge Quiet Standby Current	x8	58	63	68	mA
		x16	60	65	70	mA
IDD2N	Precharge Standby Current	x8	61	66	71	mA
		x16	63	68	73	mA
IDD2NT	Precharge Standby ODT Current	x8	83	90	96	mA
		x16	85	92	96	mA
IDD3N	Active Standby Current	x8	88	96	100	mA
		x16	90	100	105	mA
IDD3P	Active Power-Down Current Always Fast Exit	x8	68	77	82	mA
		x16	70	80	85	mA
IDD4R	Operating Current Burst Read	x8	180	210	230	mA
		x16	190	220	240	mA
IDD4W	Operating Current Burst Write	x8	200	240	265	mA
		x16	210	250	280	mA
IDD5B	Burst Refresh Current	x8	170	185	200	mA
		x16	180	195	210	mA
IDD6 [1]	Self-Refresh Current Normal	x8	25	25	25	mA
		x16	25	25	25	mA
IDD6ET [2]	Self-Refresh Current Extended	x8	28	28	28	mA
		x16	28	28	28	mA
IDD7	All Bank Interleave Read Current	x8	220	255	275	mA
		x16	240	270	290	mA
IDD8	RESET Low Current	x8	21	21	22	mA
		x16	23	23	24	mA

Notes

1. Tc = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDD*x* by up to an additional 2mA.
3. Restricted to TC (MAX) = 85°C.
4. Tc = 85°C; ASR and ODT are disabled; SRT is enabled.

IDD Specifications and Measurement Conditions

IDD Specifications (DDR3)

Symbol	Parameter	Width	DDR3-1600 11-11-11	DDR3-1866 13-13-13	DDR3-2133 14-14-14	Unit
IDD0	Operating Current 0 One Bank Activate -> Precharge	x8	100	120	130	mA
		x16	110	130	150	mA
IDD1	Operating Current 1 One Bank Activate -> Read - >Precharge	x8	110	125	135	mA
		x16	120	135	155	mA
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	x8	20	20	20	mA
		x16	22	22	22	mA
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	x8	43	45	47	mA
		x16	45	47	49	mA
IDD2Q	Precharge Quiet Standby Current	x8	58	63	68	mA
		x16	60	65	70	mA
IDD2N	Precharge Standby Current	x8	61	66	71	mA
		x16	63	68	73	mA
IDD2NT	Precharge Standby ODT Current	x8	83	90	96	mA
		x16	85	92	98	mA
IDD3N	Active Standby Current	x8	88	96	100	mA
		x16	90	100	105	mA
IDD3P	Active Power-Down Current Always Fast Exit	x8	68	77	82	mA
		x16	70	80	85	mA
IDD4R	Operating Current Burst Read	x8	180	210	230	mA
		x16	190	220	240	mA
IDD4W	Operating Current Burst Write	x8	200	240	265	mA
		x16	210	250	280	mA
IDD5B	Burst Refresh Current	x8	170	185	200	mA
		x16	180	195	210	mA
IDD6 [1]	Self-Refresh Current Normal	x8	25	25	25	mA
		x16	25	25	25	mA
IDD6ET [2]	Self-Refresh Current Extended	x8	28	28	28	mA
		x16	28	28	28	mA
IDD7	All Bank Interleave Read Current	x8	220	255	275	mA
		x16	240	270	290	mA
IDD8	RESET Low Current	x8	21	21	22	mA
		x16	23	23	24	mA

Notes

1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDD*x* by up to an additional 2mA.
3. Restricted to TC (MAX) = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.

Revision History

Revision	Date	Page	Notes
0.1	Nov., 2020	-	Preliminary
0.2	Dec., 2020	12~13	IDDx value updated
1.0	Dec., 2025	7	Add package information