

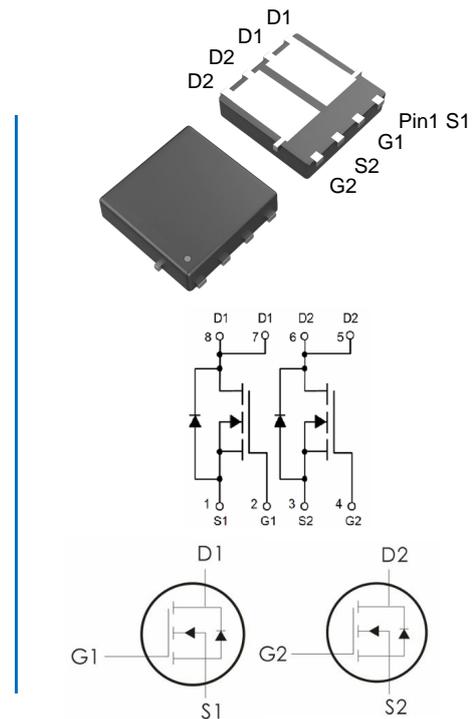
Description:

This Dual N-Channel MOSFET uses advanced SGT technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=60V, I_D=20A, R_{DS(ON)} < 20m\ \Omega @ V_{GS}=10V$ (Typ: $15.6m\ \Omega$)
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density SGT technology for ultra low $R_{DS(ON)}$.
- 5) Excellent package for good heat dissipation.
- 6) MSL3



Package Marking and Ordering Information:

| Part NO. | Marking | Package | Packing |
|----------|---------|-----------|---------------|
| ZE017DTG | E017DT | DFN3*3-8D | 5000 pcs/Reel |

Absolute Maximum Ratings: ($T_c=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Ratings | Units |
|----------------|--|----------|------------------|
| V_{DS} | Drain-Source Voltage | 60 | V |
| V_{GS} | Gate-Source Voltage | ± 20 | V |
| I_D | Continuous Drain Current ¹ | 20 | A |
| | Continuous Drain Current- $T_c=100^\circ\text{C}$ ¹ | 14 | |
| I_{DM} | Pulsed Drain Current ² | 80 | |
| P_D | Power Dissipation | 16.5 | W |
| E_{AS} | Single pulse avalanche energy ³ | 25 | mJ |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55-+150 | $^\circ\text{C}$ |

Thermal Characteristics:

| Symbol | Parameter | Max | Units |
|-----------------|--------------------------------------|-----|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 7.5 | $^\circ\text{C}/\text{W}$ |

Electrical Characteristics: ($T_c=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|-----|------|-----------|---------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=250\ \mu\text{A}$ | 60 | --- | --- | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{GS}=0V, V_{DS}=60V$ | --- | --- | 1 | μA |
| I_{GSS} | Gate-Source Leakage Current | $V_{GS}=\pm 20V, V_{DS}=0A$ | --- | --- | ± 100 | nA |
| On Characteristics | | | | | | |
| $V_{GS(th)}$ | Gate-Source Threshold Voltage | $V_{GS}=V_{DS}, I_D=250\ \mu\text{A}$ | 1 | 1.5 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance ⁴ | $V_{GS}=10V, I_D=10A$ | --- | 15.6 | 20 | m Ω |
| | | $V_{GS}=4.5V, I_D=5A$ | --- | 20 | 26 | |
| Dynamic Characteristics | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$ | --- | 605 | --- | pF |
| C_{oss} | Output Capacitance | | --- | 195 | -- | |
| C_{rss} | Reverse Transfer Capacitance | | --- | 6.5 | --- | |
| Switching Characteristics | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DS}=30V, I_D=20A,$ $R_G=6\ \Omega, V_{GS}=10V$ | --- | 3.2 | --- | ns |
| t_r | Rise Time | | --- | 3.9 | --- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | --- | 12 | --- | ns |
| t_f | Fall Time | | --- | 5.6 | --- | ns |
| Q_g | Total Gate Charge | $V_{GS}=10V, V_{DS}=30V,$ $I_D=20A$ | --- | 12 | --- | nC |
| Q_{gs} | Gate-Source Charge | | --- | 1.2 | --- | nC |
| Q_{gd} | Gate-Drain "Miller" Charge | | --- | 2.6 | --- | nC |
| Drain-Source Diode Characteristics | | | | | | |
| V_{SD} | Diode Forward Voltage | $V_{GS}=0V, I_{SD}=20A$ | --- | --- | 1.2 | V |
| I_S | Continuous Drain Current | $V_D=V_G=0V$ | --- | --- | 16.6 | A |
| I_{SM} | Pulsed Drain Current | | --- | --- | 66.6 | A |
| T_{rr} | Reverse Recovery Time | $I_F=15A, T_J=25^\circ\text{C}$ | --- | 20 | --- | ns |
| Q_{rr} | Reverse Recovery Charge | $dI/dt=100A/\mu\text{s}$ | --- | 8.1 | --- | nC |

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C, V_{DD}=30V, V_G=10V, L=0.5mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

Test Circuit

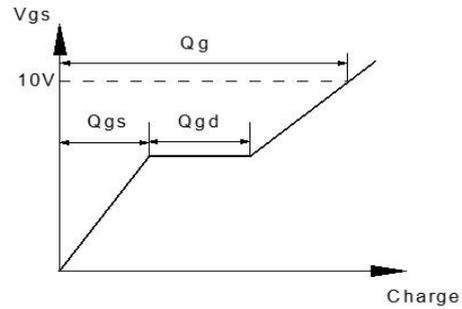
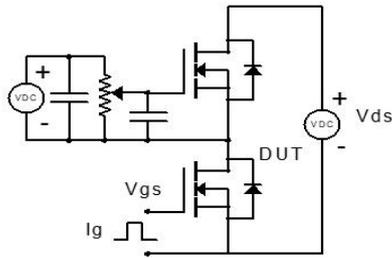


Figure 1: Gate Charge Test Circuit & Waveform

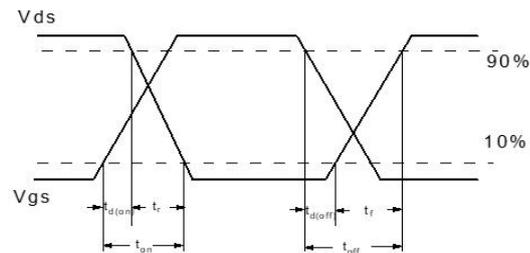
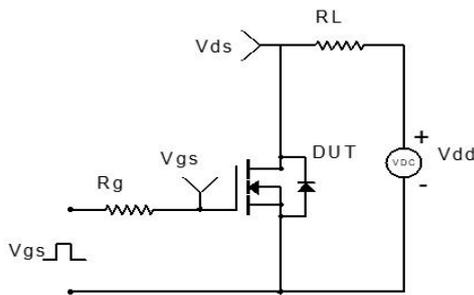


Figure 2: Resistive Switching Test Circuit & Waveform

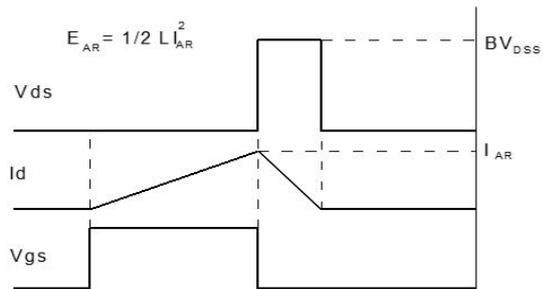
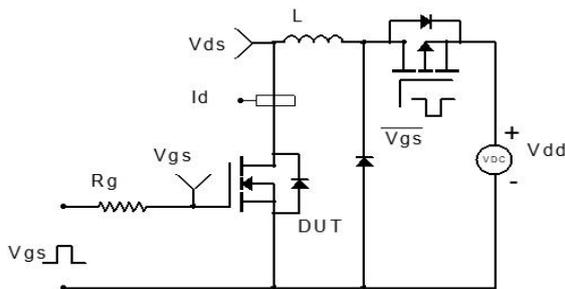


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

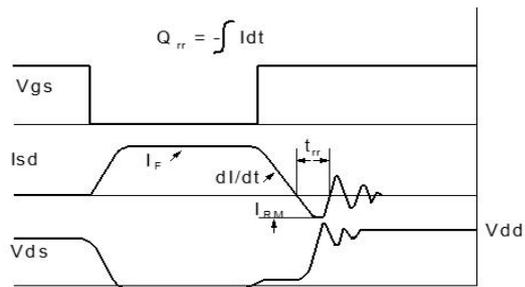
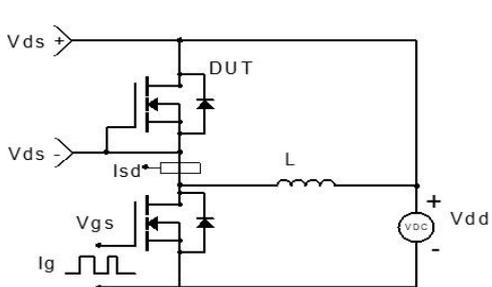
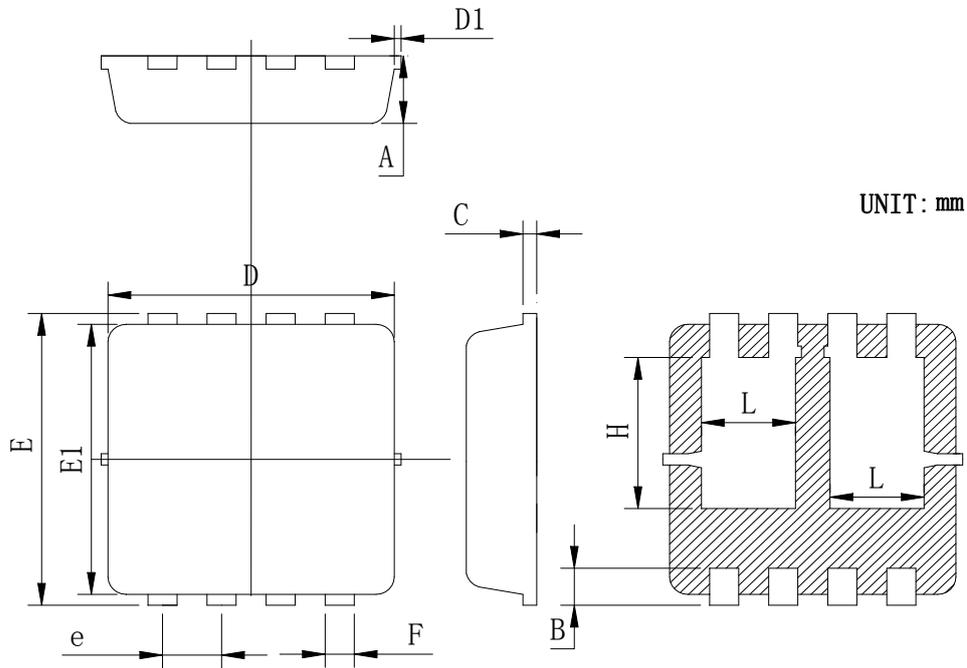


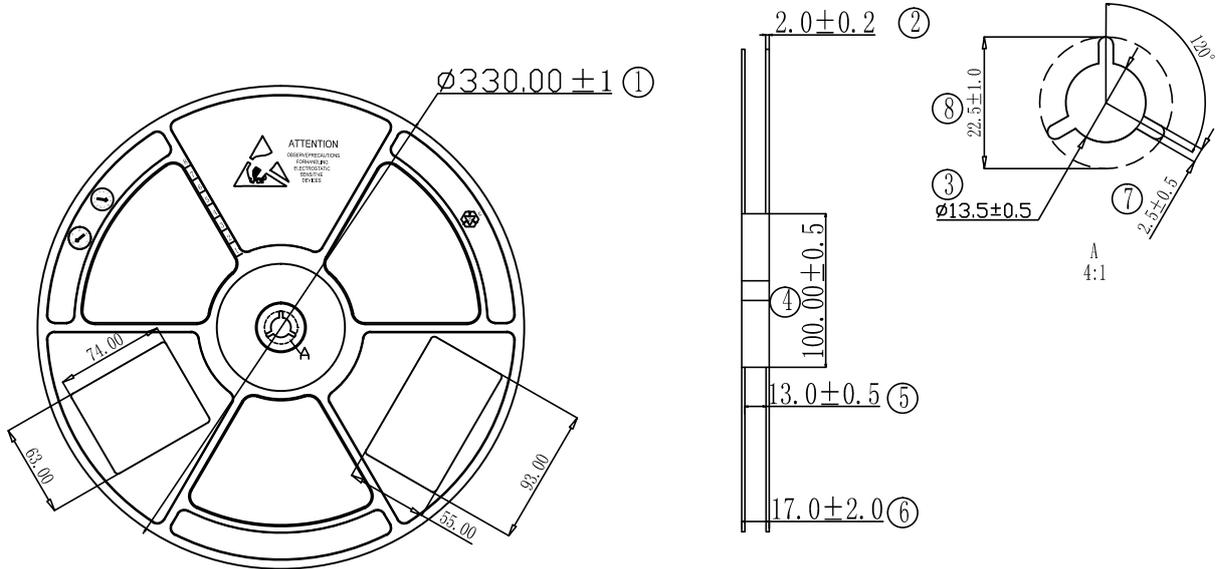
Figure 4: Diode Recovery Test Circuit & Waveform

DFN3X3-8D Package Outline Data


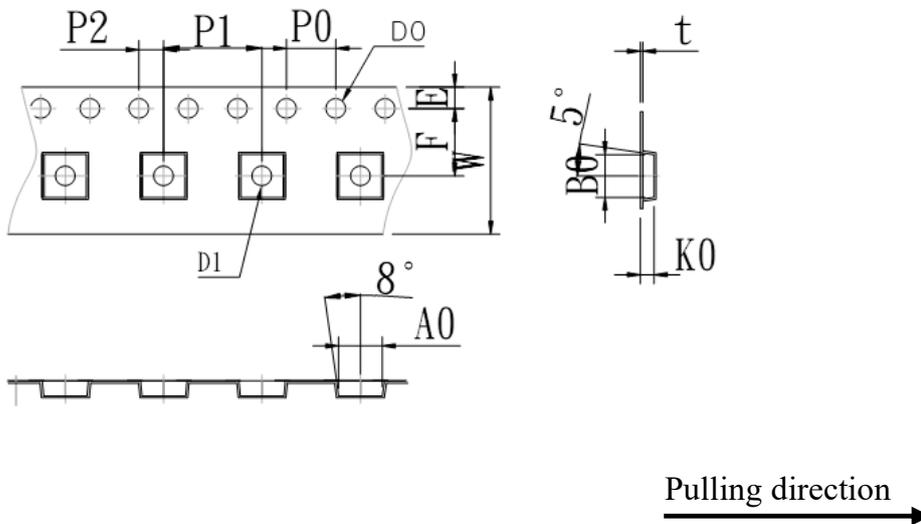
| Symbol | Min | Typ | Max |
|--------|-------|-------|-------|
| A | 0.725 | 0.775 | 0.825 |
| B | 0.28 | 0.38 | 0.48 |
| C | 0.13 | 0.15 | 0.20 |
| D | 3.05 | 3.15 | 3.25 |
| D1 | | | 0.10 |
| E | 3.25 | 3.35 | 3.45 |
| E1 | 3.0 | 3.1 | 3.2 |
| e | 0.60 | 0.65 | 0.70 |
| F | 0.27 | 0.32 | 0.37 |
| H | 1.63 | 1.73 | 1.83 |
| L | 0.93 | 1.03 | 1.13 |

Tape & Reel Information

Dimensions in mm



| | | | | | | | | |
|--------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Symbol | A0 | B0 | K0 | D0 | D1 | P0 | P1 | 10*P0 |
| Spec | 3.55±0.10 | 3.45±0.10 | 1.13±0.10 | 1.55±0.10 | 1.55±0.10 | 4.00±0.10 | 8.00±0.10 | 40.0±0.10 |
| Symbol | W | E | F | P2 | t | | | |
| Spec | 12.00±0.10 | 1.75±0.10 | 5.50±0.10 | 2.00±0.10 | 0.20±0.05 | | | |



Marking Information:

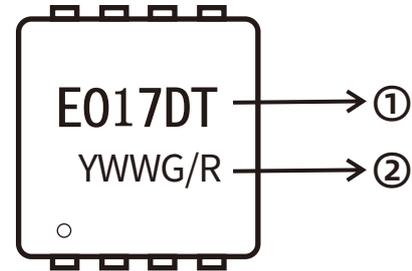
①. Part NO.

②. Date Code(YWWG / R)

Y : Year Code , last digit of the year

WW : Week Code(01-53)

G/R : G(Green) /R(Lead Free)

**Previous Version**

| Version | Date | Subjects (major changes since last revision) |
|---------|------------|--|
| 1.0 | 2025-09-06 | Release of final version |

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