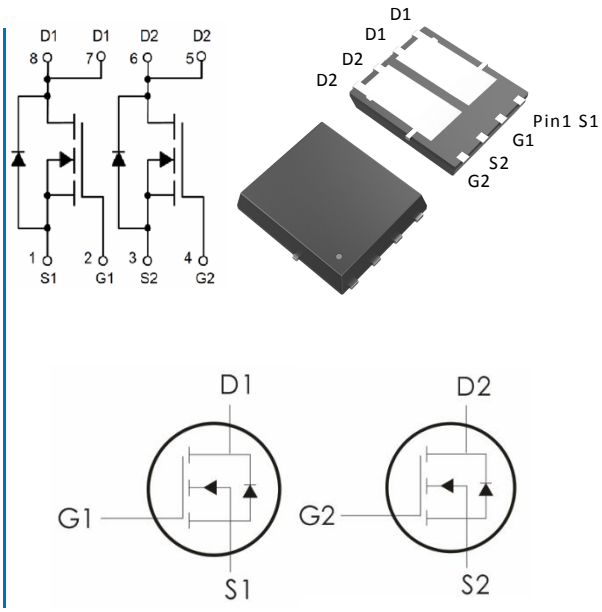
Description：

This Dual N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.



Features：

1) V_{DS}=40V,I_D=50A,$R_{DS(ON)}$<8mΩ @V_{GS}=10V（Typ：6mΩ）
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra low $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.
6) MSL3

Package Marking and Ordering Information：

Part NO.	Marking	Package	Packing
ND008DNG	D008DN	DFN5*6-8D	5000 pcs/Reel

Absolute Maximum Ratings：(T_C=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1]	50	A
	Continuous Drain Current-T_C=100℃[1]	35	
I_{DM}	Pulsed Drain Current [2]	200	
P_D	Power Dissipation	83	W
E_{AS}	Single pulse avalanche energy [3]	100	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance,Junction to Case	1.5	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient	50	℃/W

Electrical Characteristics: (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	40	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=40V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics (Note3)						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1	---	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=10V,I_D=20A	---	6	8	mΩ
		V_{GS}=4.5V,I_D=10A	---	8	10	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1MHz	---	2450	---	pF
C_{oss}	Output Capacitance		---	175	--	
C_{rss}	Reverse Transfer Capacitance		---	144	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=20V, I_D=20A, R_G=3Ω,V_{GS}=10V	---	10	---	ns
t_r	Rise Time		---	29	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	42	---	ns
t_f	Fall Time		---	7	---	ns
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=20A	---	35	---	nC
Q_{gs}	Gate-Source Charge		---	10	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	10	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=30A	---	---	1.2	V
I_S	Continuous Drain Curren	V_D=V_G=0V	---	---	50	A
I_{SM}	Pulsed Drain Current		---	---	200	A
Trr	Reverse Recovery Time	I_F=20A,T_J=25℃ dI/dt=100A/us	---	11	---	ns
Qrr	Reverse Recovery Charge		---	5	---	nC

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : TJ=25℃,VDD=20V,V_G=10V,L=0.5mH
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics: (T_C=25℃ unless otherwise noted)

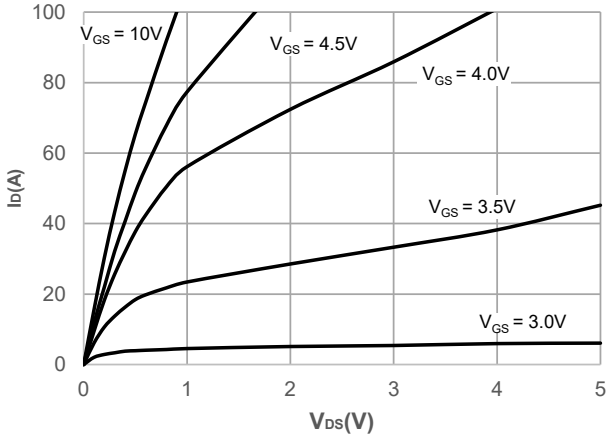


Figure 1: Output Characteristics

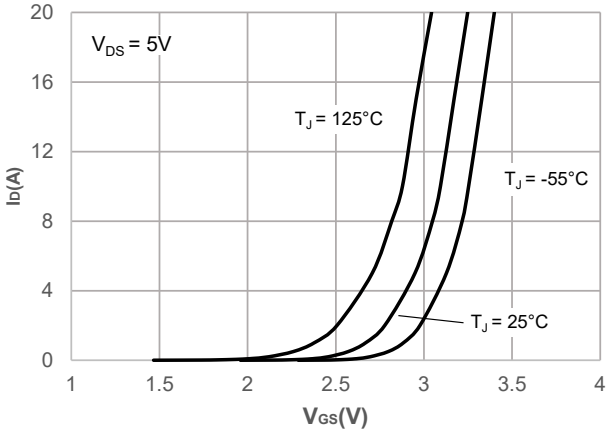


Figure 2: Typical Transfer Characteristics

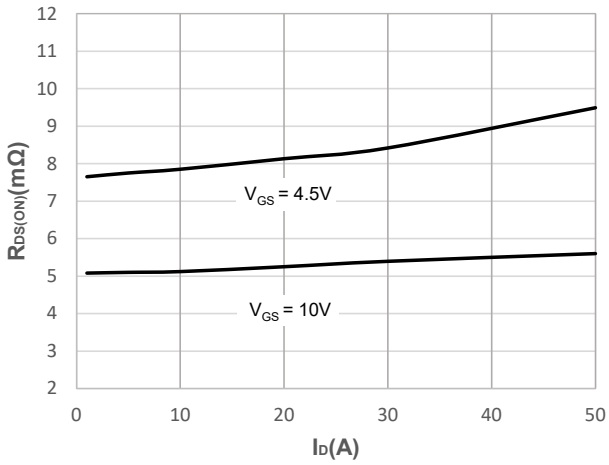


Figure 3: On-resistance vs. Drain Current

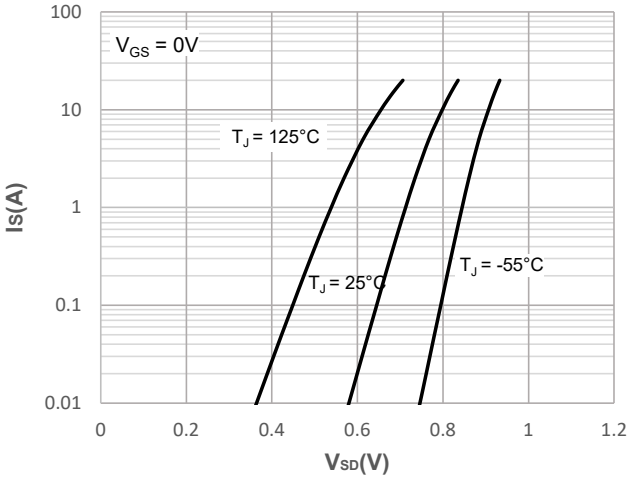


Figure 4: Body Diode Characteristics

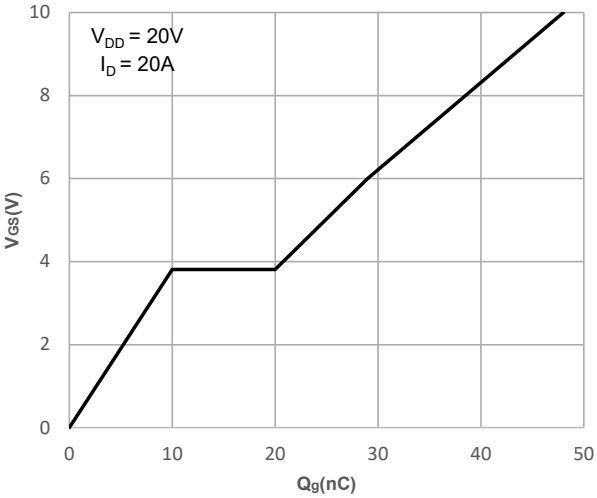


Figure 5: Gate Charge Characteristics

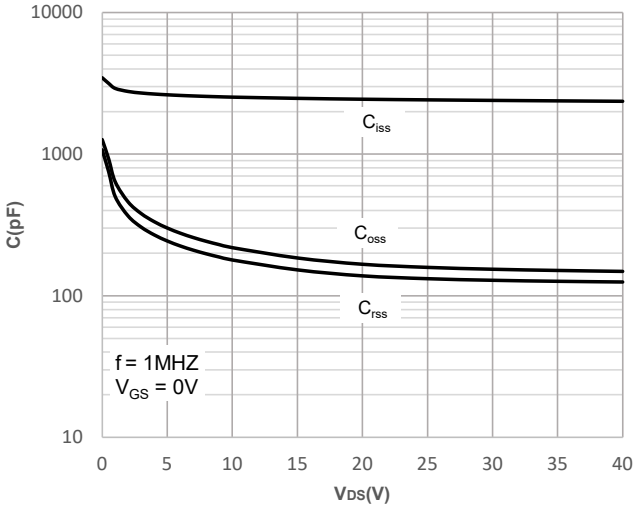


Figure 6: Capacitance Characteristics

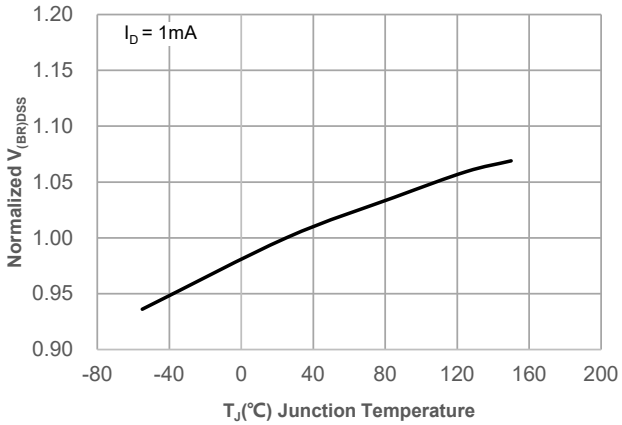


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

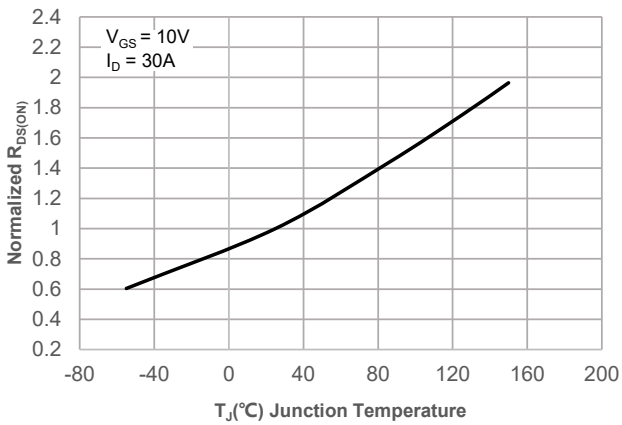


Figure 8: Normalized on Resistance vs. Junction Temperature

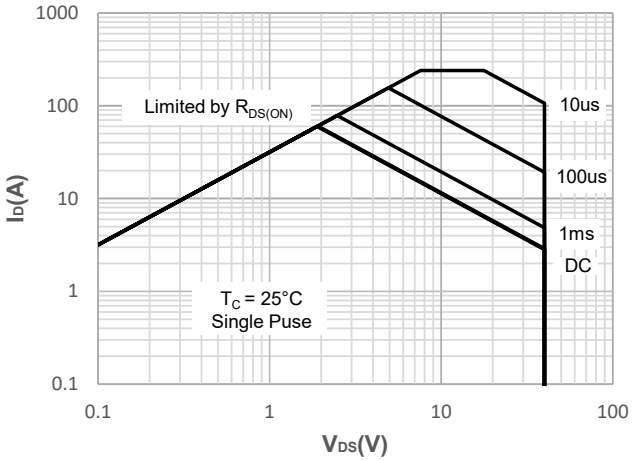


Figure 9: Maximum Safe Operating Area

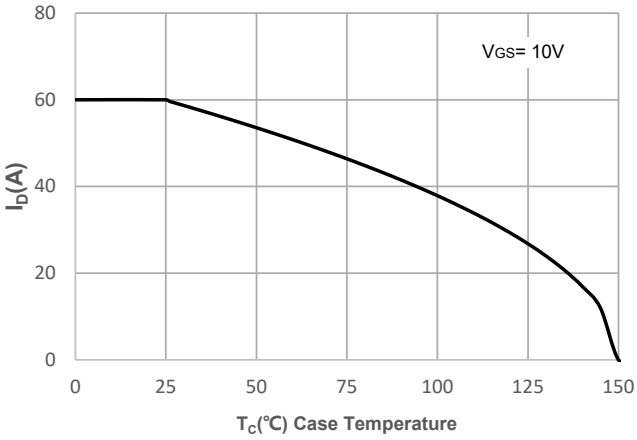


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

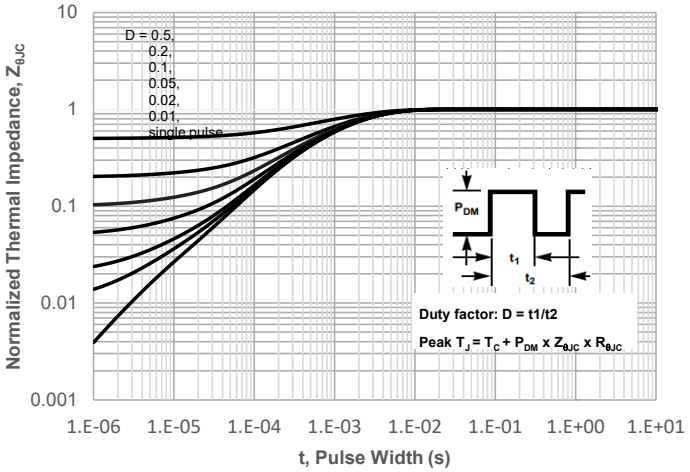


Figure 11: Normalized Maximum Transient Thermal Impedance

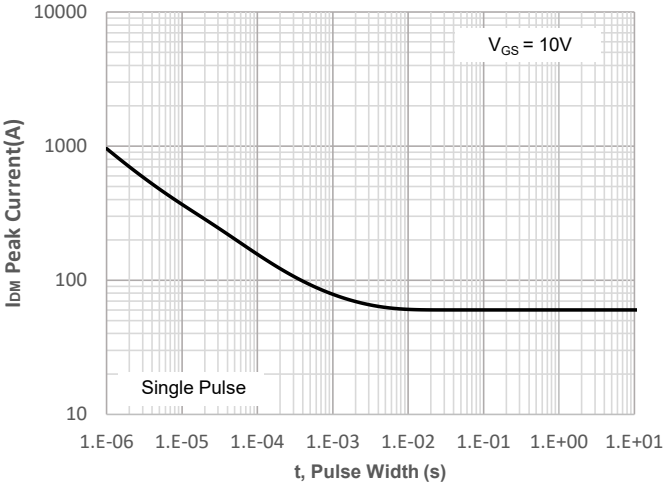
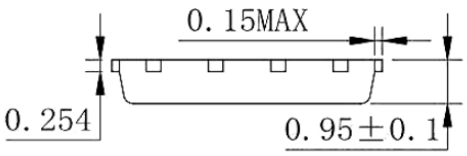
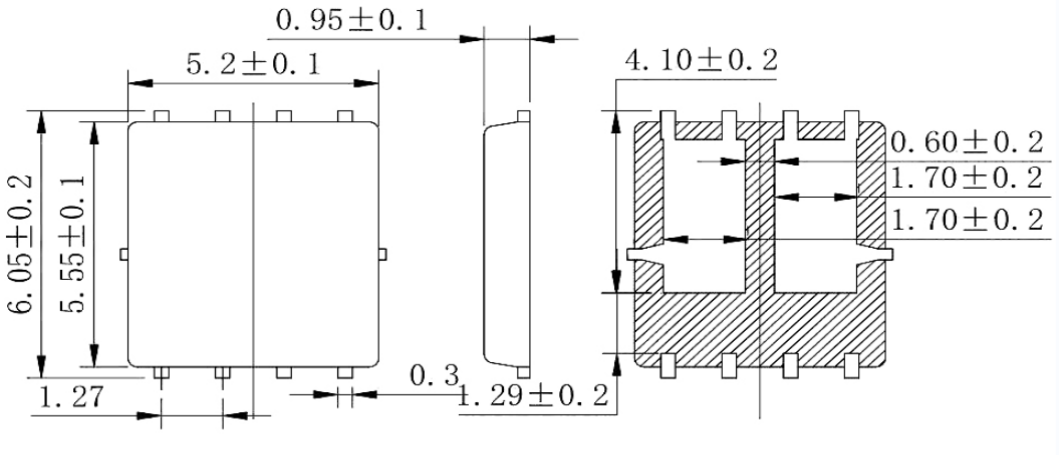


Figure 12: Peak Current Capacity

DFN5×6-8D Package Information：

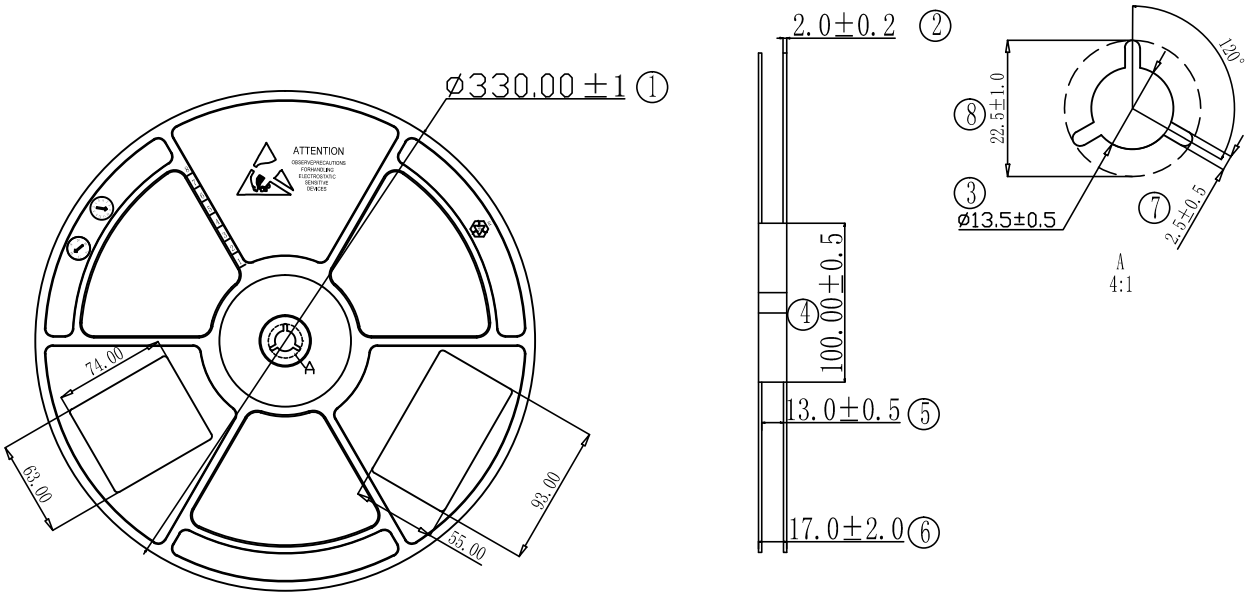


UNIT：mm

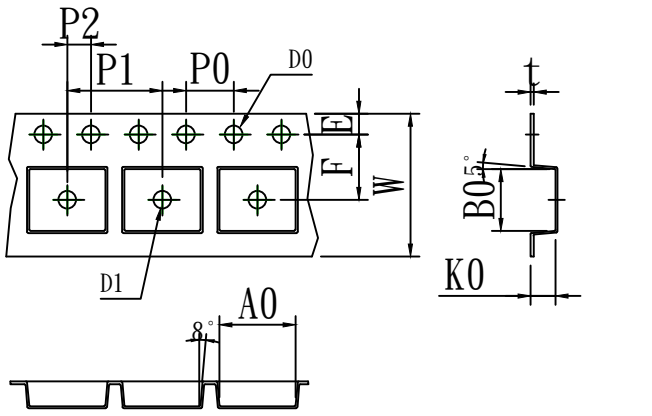


Tape & Reel Information

Dimensions in mm



Symbol	A0	B0	K0	D0	D1	P0	P1	10*P0
Spec	6.15±0.10	5.40±0.10	1.30±0.10	1.55±0.10	1.55±0.10	4.00±0.10	8.00±0.10	40.00±0.10
Symbol	W	E	F	P2	t			
Spec	12.00±0.10	1.75±0.10	5.50±0.10	2.00±0.10	0.20±0.05			



Pulling direction

Marking Information：

①. Doingter LOGO

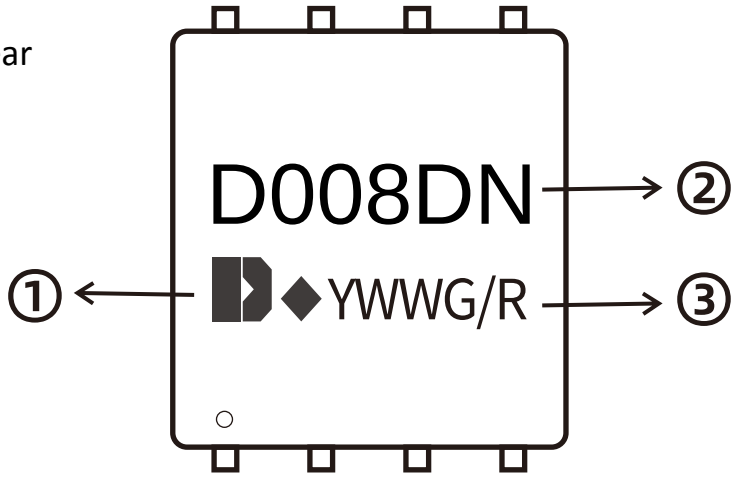
②. Part NO.

③. Date Code(YWWG / R)

Y：Year Code , last digit of the year

WW：Week Code(01-53)

G/R：G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2025-04-12	Release of final version

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