IRFPC50PBF-VB Datasheet

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.7
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	2.7	
Q_{gd} (nC)	8.1	
Configuration	Single	

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current

RoHS COMPLIANT
HALOGEN FREE Available

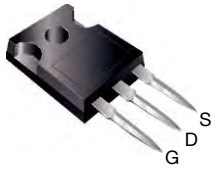
APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- Power Factor Correction

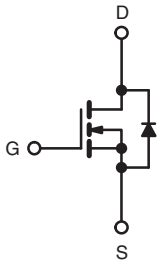
TYPICAL SMPS TOPOLOGIES

- Low Power Single Transistor Flyback

TO-247AC



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	12	A
		T_C = 100 °C		8.0	
Pulsed Drain Current[a]			I_{DM}	30	
Linear Derating Factor				0.28	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	113	mJ
Repetitive Avalanche Current[a]			I_{AR}	7.8	A
Repetitive Avalanche Energy[a]			E_{AR}	7.6	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	48	W
Peak Diode Recovery dV/dt[c]			dV/dt	3.8	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 95 mH, R_g = 25 Ω, I_{AS} = 1.4 A (see fig. 12).
c. $I_{SD} \leq$ 1.4 A, dI/dt $\leq$ 180 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		650	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.0	
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 4.8 A[b]	-	0.7	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 4.8 A		0.88	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1070	-	pF
Output Capacitance	C_{oss}			-	32.6	-	
Reverse Transfer Capacitance	C_{rss}			-	2.4	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 1.0 V, f = 1.0 MHz	-	320	-	
			V_{DS} = 480 V, f = 1.0 MHz	-	11.5	-	
Effective Output Capacitance	C_{oss} eff.		V_{DS} = 0 V to 480 V[c]	-	130	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 1.4 A, V_{DS} = 400 V, see fig. 6 and 13[b]	-	-	14	nC
Gate-Source Charge	Q_{gs}			-	-	2.7	
Gate-Drain Charge	Q_{gd}			-	-	8.1	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 1.4 A, R_g = 2.15 Ω, R_D = 178 Ω, see fig. 10[b]		-	9.8	-	ns
Rise Time	t_r			-	14	-	
Turn-Off Delay Time	$t_{d(off)}$			-	18	-	
Fall Time	t_f			-	20	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	1 1	-	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	2 5	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 1.4 A, V_{GS} = 0 V[b]		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 1.4 A, dI/dt = 100 A/μs[b]		-	290	440	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	510	760	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

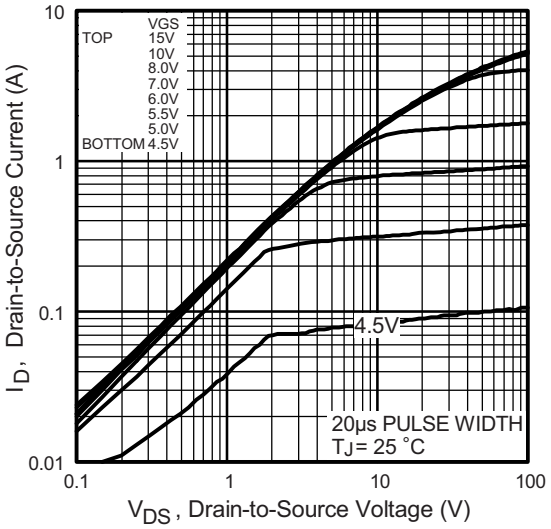


Fig. 1 - Typical Output Characteristics

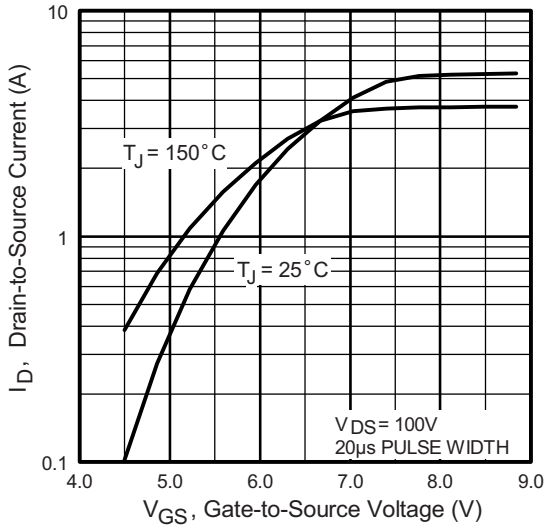


Fig. 3 - Typical Transfer Characteristics

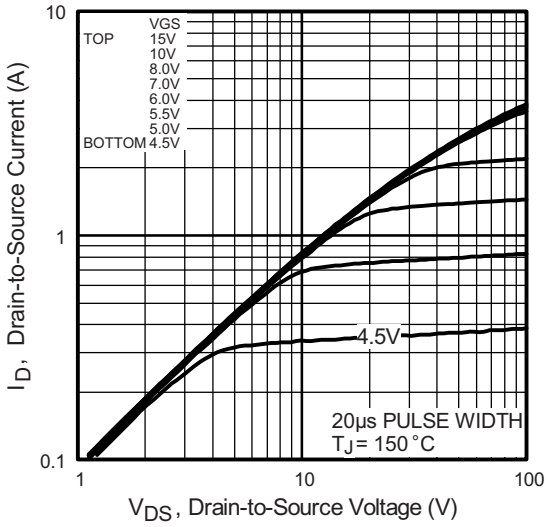


Fig. 2 - Typical Output Characteristics

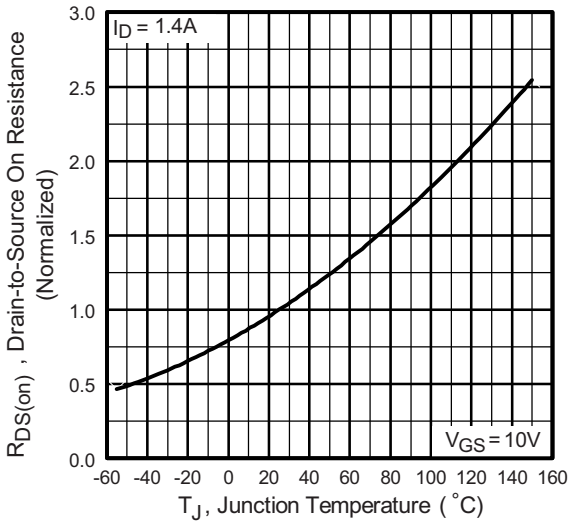


Fig. 4 - Normalized On-Resistance vs. Temperature

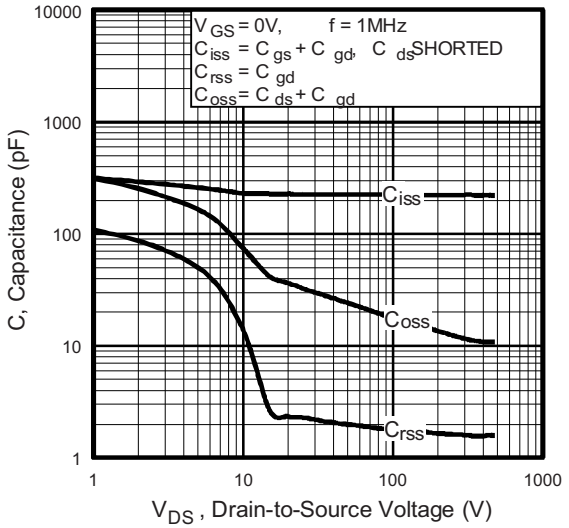


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

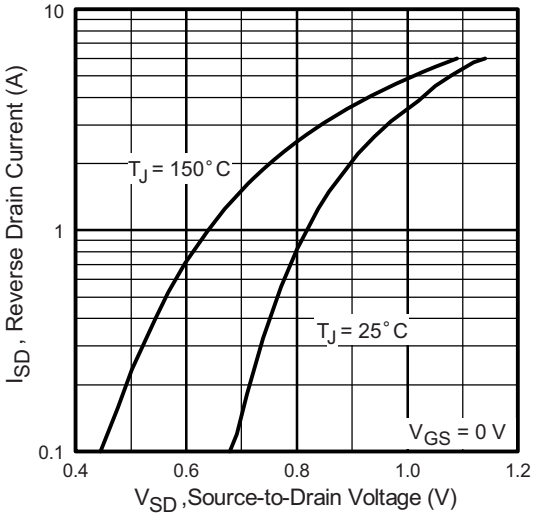


Fig. 7 - Typical Source-Drain Diode Forward Voltage

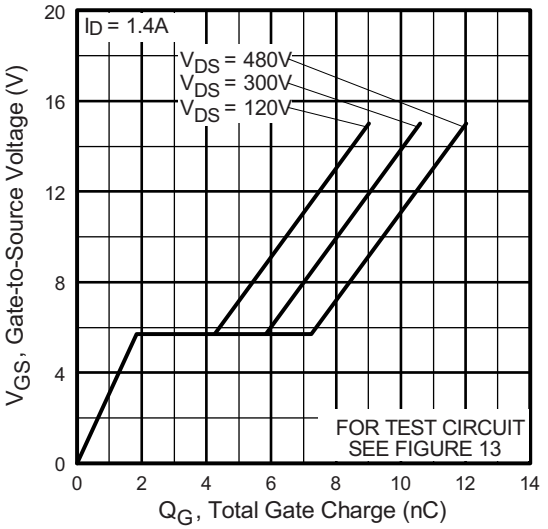


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

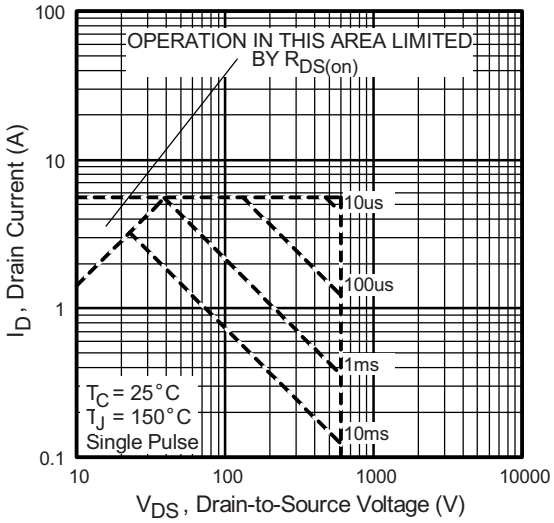


Fig. 8 - Maximum Safe Operating Area

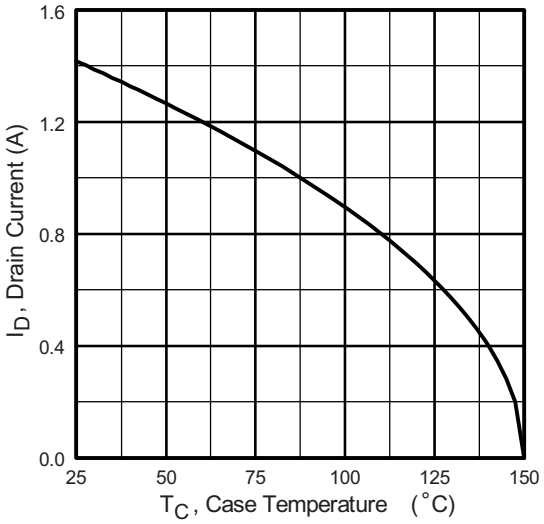


Fig. 9 - Maximum Drain Current vs. Case Temperature

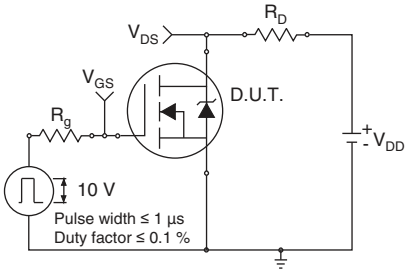


Fig. 10a - Switching Time Test Circuit

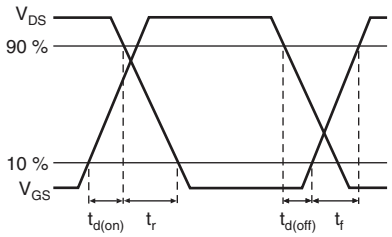


Fig. 10b - Switching Time Waveforms

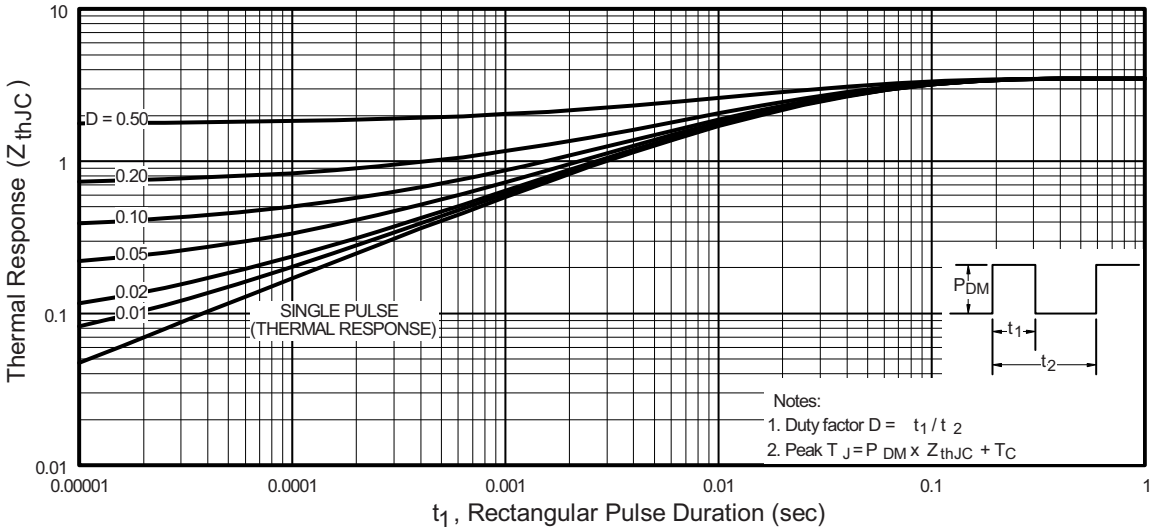


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

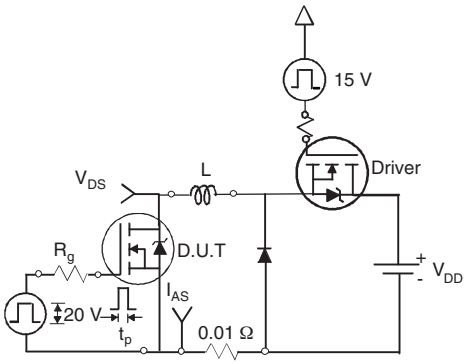


Fig. 12a - Unclamped Inductive Test Circuit

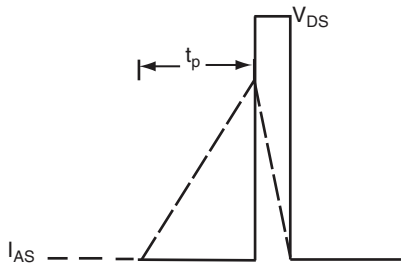


Fig. 12b - Unclamped Inductive Waveforms

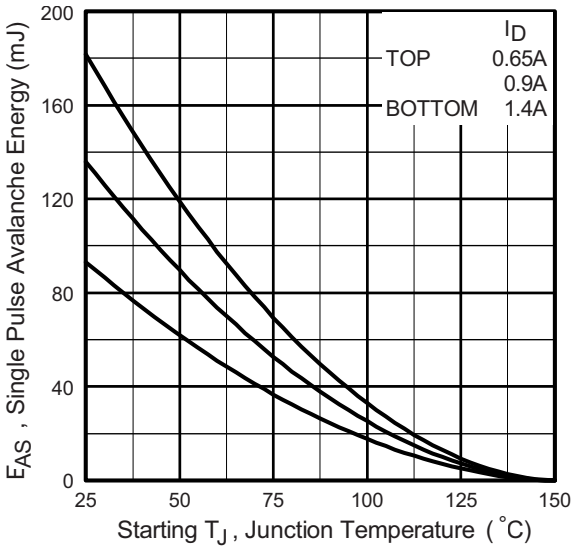


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

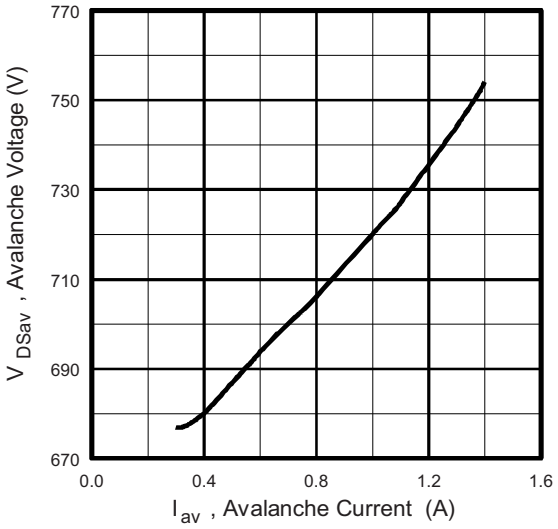


Fig. 12d - Basic Gate Charge Waveform

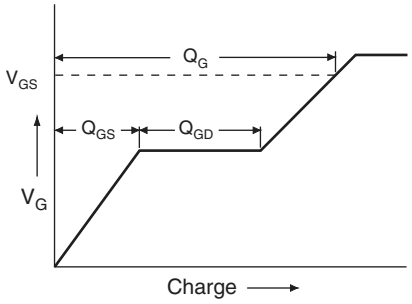


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

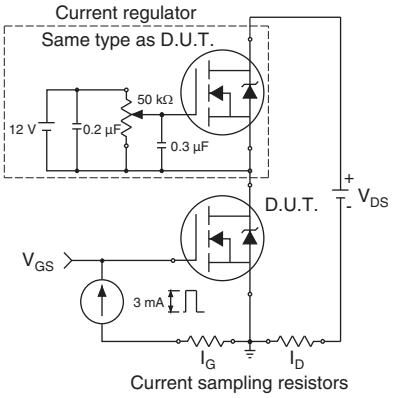
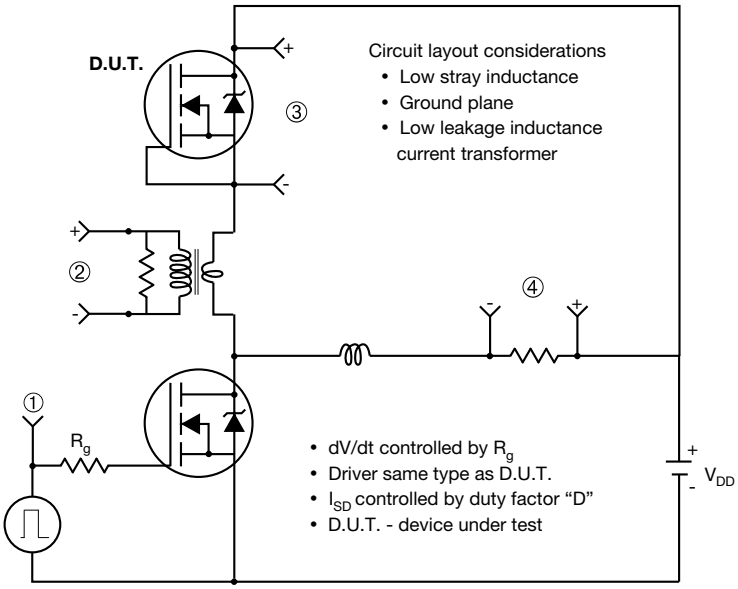
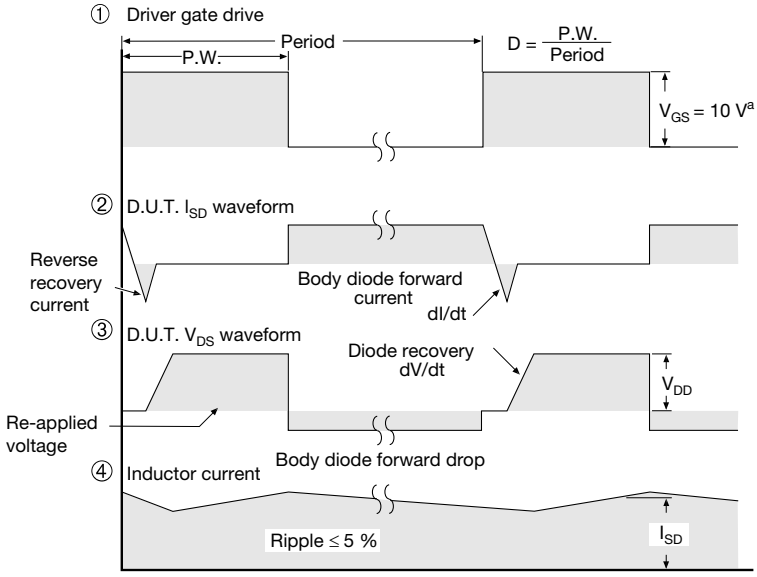


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



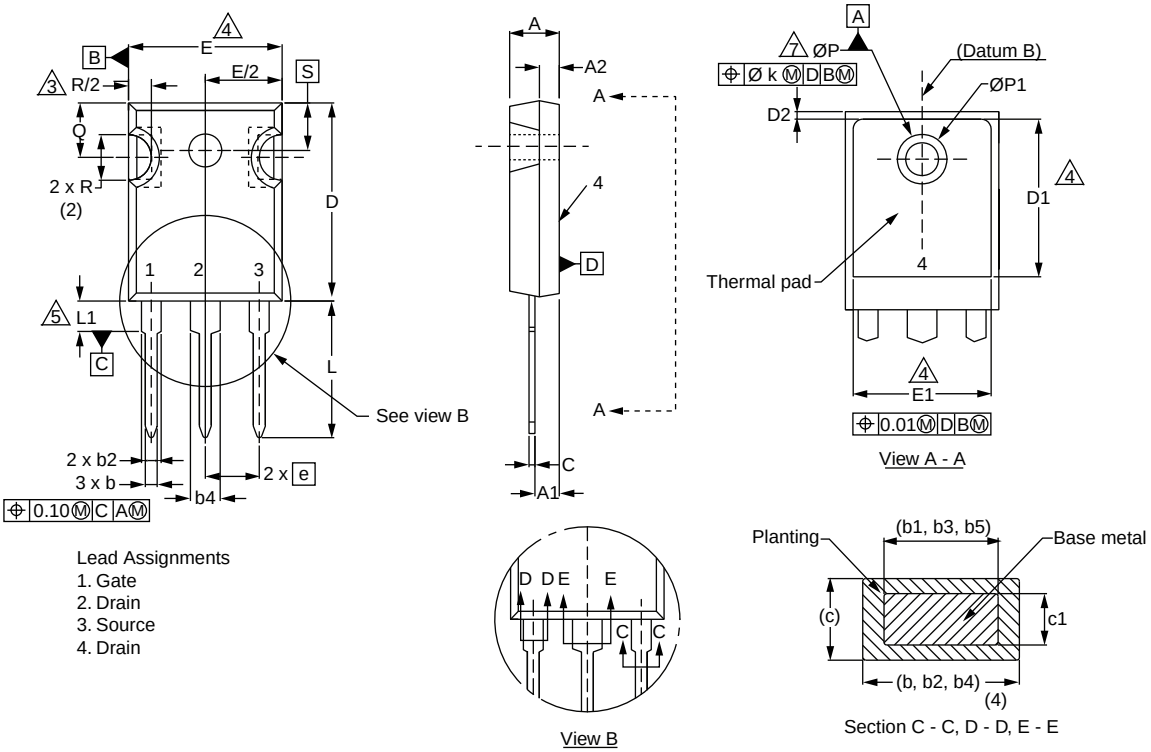


Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

TO-247AC (High Voltage)



Lead Assignments
1. Gate
2. Drain
3. Source
4. Drain

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

Taiwan VBsemi Electronics Co., Ltd., branches, agents, employees, and all persons acting on its or their representatives (collectively, the "Taiwan VBsemi"), assumes no responsibility for any errors, inaccuracies or incomplete data contained in the table or any other any disclosure of any information related to the product.(www.VBsemi.com)

Taiwan VBsemi makes no guarantee, representation or warranty on the product for any particular purpose of any goods or continuous production. To the maximum extent permitted by applicable law on Taiwan VBsemi relinquished: (1) any application and all liability arising out of or use of any products; (2) any and all liability, including but not limited to special, consequential damages or incidental ; (3) any and all implied warranties, including a particular purpose, non-infringement and merchantability guarantee.

Statement on certain types of applications are based on knowledge of the product is often used in a typical application of the general product VBsemi Taiwan demand that the Taiwan VBsemi of. Statement on whether the product is suitable for a particular application is non-binding. It is the customer's responsibility to verify specific product features in the products described in the specification is appropriate for use in a particular application. Parameter data sheets and technical specifications can be provided may vary depending on the application and performance over time. All operating parameters, including typical parameters must be made by customer's technical experts validated for each customer application. Product specifications do not expand or modify Taiwan VBsemi purchasing terms and conditions, including but not limited to warranty herein.

Unless expressly stated in writing, Taiwan VBsemi products are not intended for use in medical, life saving, or life sustaining applications or any other application. Wherein VBsemi product failure could lead to personal injury or death, use or sale of products used in Taiwan VBsemi such applications using client did not express their own risk. Contact your authorized Taiwan VBsemi people who are related to product design applications and other terms and conditions in writing.

The information provided in this document and the company's products without a license, express or implied, by estoppel or otherwise, to any intellectual property rights granted to the VBsemi act or document. Product names and trademarks referred to herein are trademarks of their respective representatives will be all.

Material Category Policy

Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be oHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.