

IRF840LCLPBF-VB Datasheet

N-Channel 650V (D-S) Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	1.3
Q_g (Max.) (nC)	210	
Q_{gs} (nC)	80	
Q_{gd} (nC)	110	
Configuration	Single	

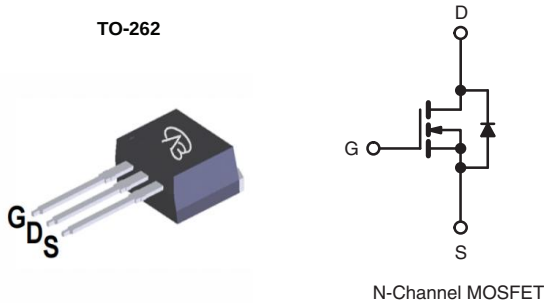
FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	21	
Linear Derating Factor		4.3	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	760	mJ
Repetitive Avalanche Current ^a	I_{AR}	50	A
Repetitive Avalanche Energy ^a	E_{AR}	51	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	530
Peak Diode Recovery dV/dt ^c	dV/dt	9.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.82\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 47\text{ A}$ (see fig. 12c).
- $I_{SD} \leq 47\text{ A}$, $dI/dt \leq 230\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.23	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	A
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.60	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 520 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 28 A ^b	-	1.3	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 28 A		23	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1400	-	pF
Output Capacitance	C _{oss}			-	960	-	
Reverse Transfer Capacitance	C _{rss}			-	120	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	270	-	
			V _{DS} = 400 V, f = 1.0 MHz	-	240	-	
Effective Output Capacitance	C _{oss eff.}		V _{DS} = 0 V to 400 V ^c	-	440	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 47 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	350	nC
Gate-Source Charge	Q _{gs}			-	-	85	
Gate-Drain Charge	Q _{gd}			-	-	180	
Turn-On Delay Time	t _{d(on)}		V _{DD} = 250 V, I _D = 47 A, R _G = 1.0 Ω, see fig. 10 ^b	-	25	-	ns
Rise Time	t _r			-	140	-	
Turn-Off Delay Time	t _{d(off)}			-	55	-	
Fall Time	t _f			-	74	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	7	A	
Pulsed Diode Forward Current ^a	I _{SM}		-	-	21		
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 47 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 47 A, dI/dt = 100 A/μs ^b		-	35	70	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	14	21	μC
Body Diode Recovery Current	I _{RRM}			-	38	-	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 400\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

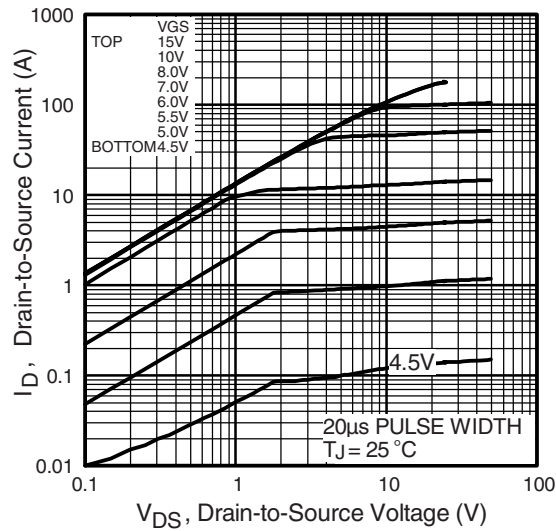


Fig. 1 - Typical Output Characteristics

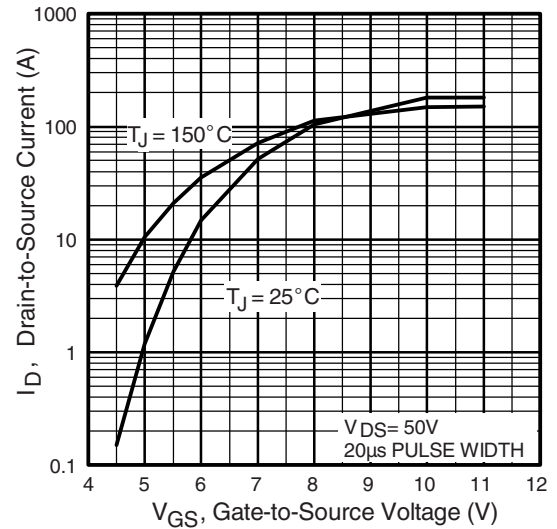


Fig. 3 - Typical Transfer Characteristics

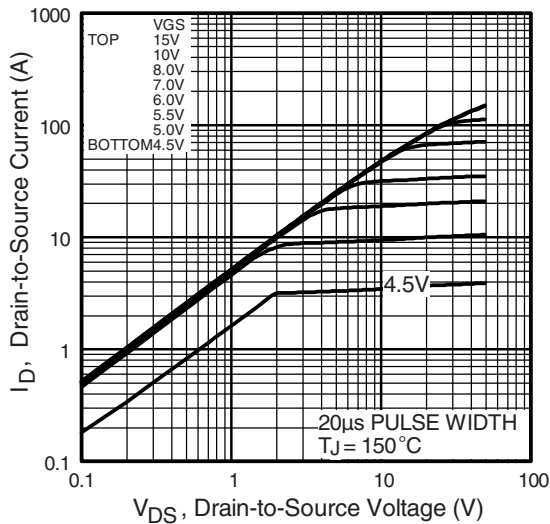


Fig. 2 - Typical Output Characteristics

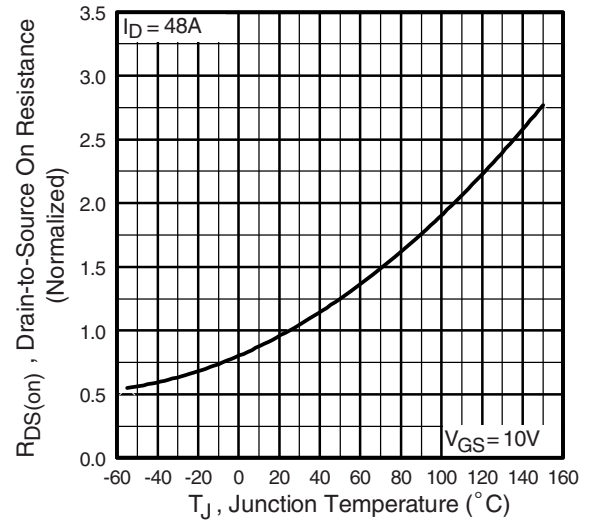


Fig. 4 - Normalized On-Resistance vs. Temperature

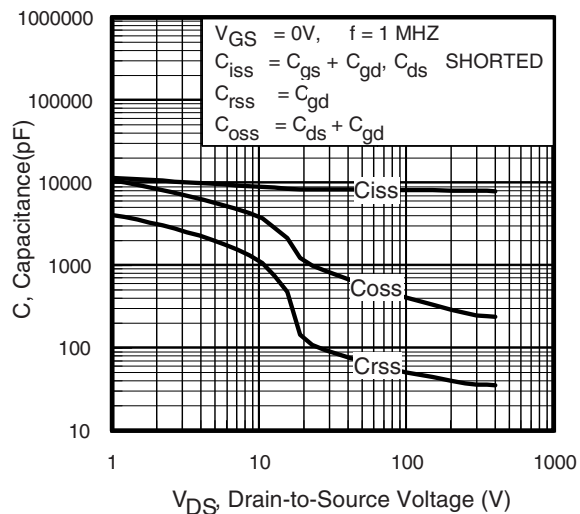


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

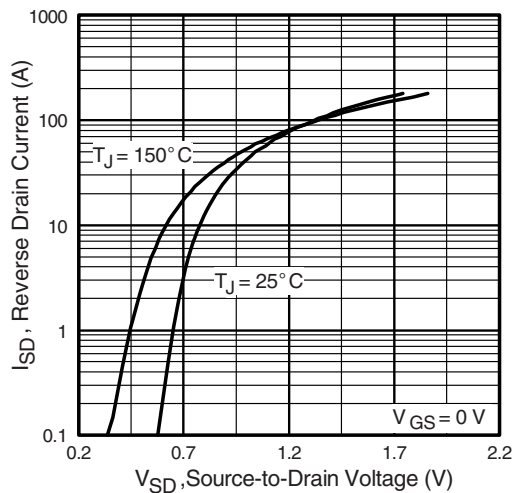


Fig. 7 - Typical Source-Drain Diode Forward Voltage

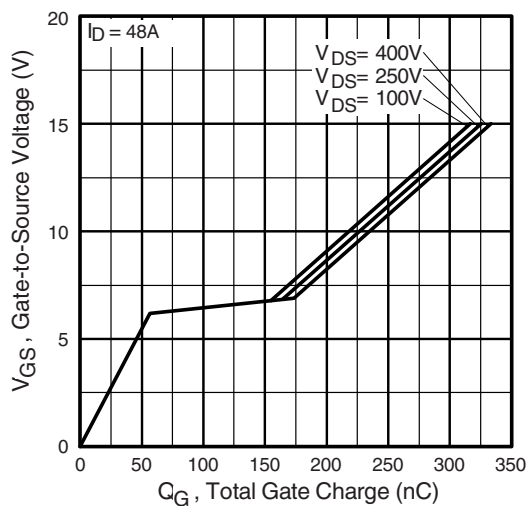


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

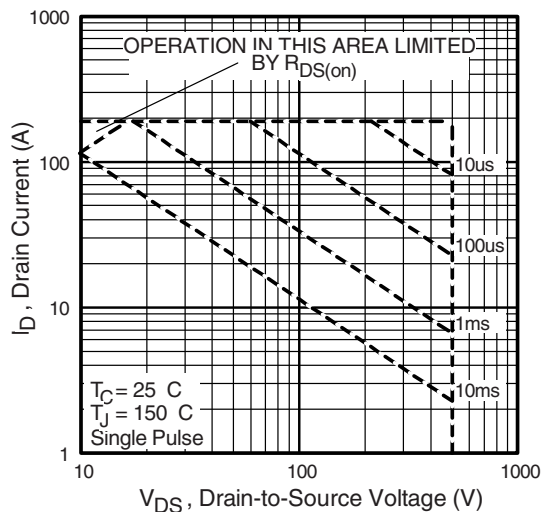


Fig. 8 - Maximum Safe Operating Area

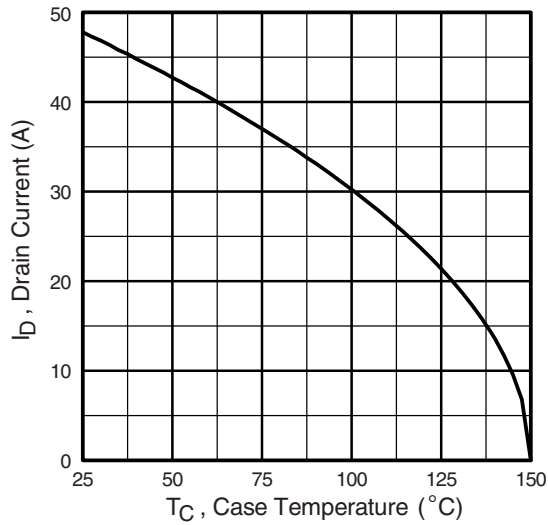


Fig. 9 - Maximum Drain Current vs. Case Temperature

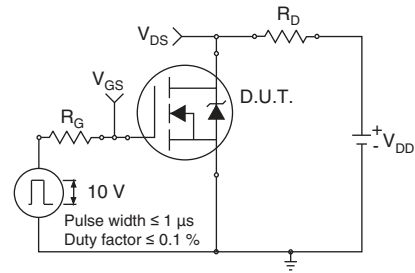


Fig. 10a - Switching Time Test Circuit

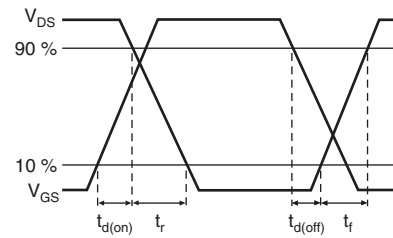


Fig. 10b - Switching Time Waveforms

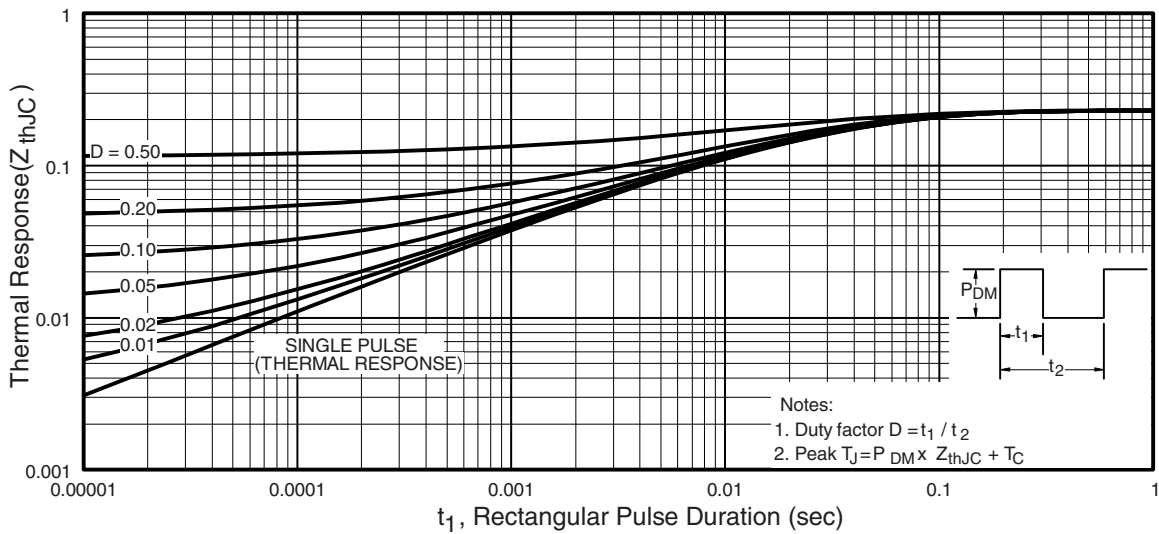


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

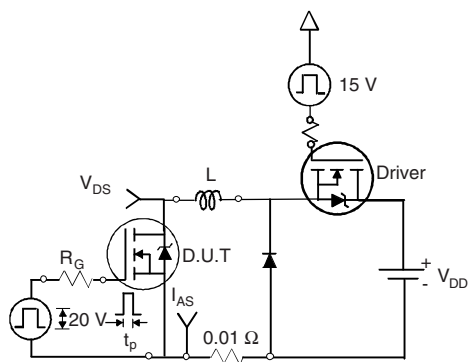


Fig. 12a - Unclamped Inductive Test Circuit

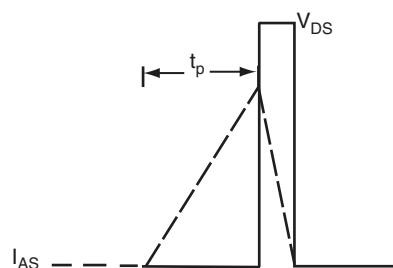


Fig. 12b - Unclamped Inductive Waveforms

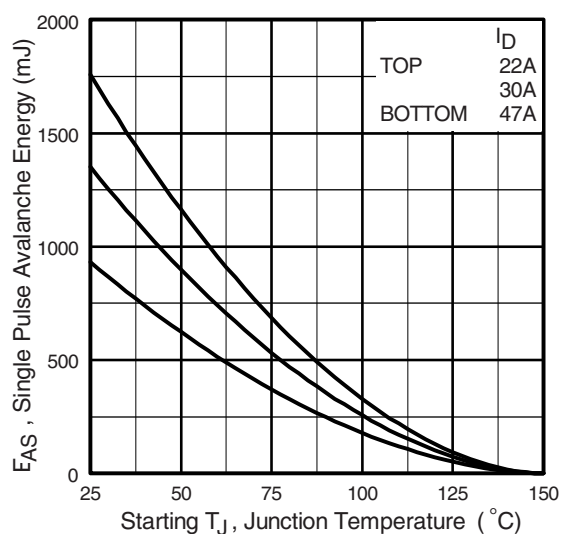


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

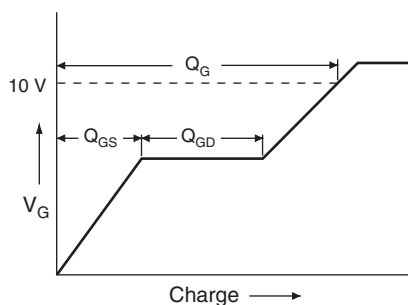


Fig. 13a - Basic Gate Charge Waveform

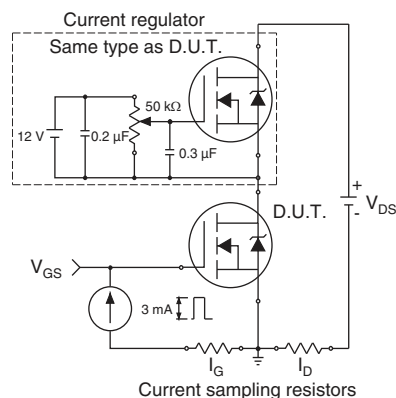
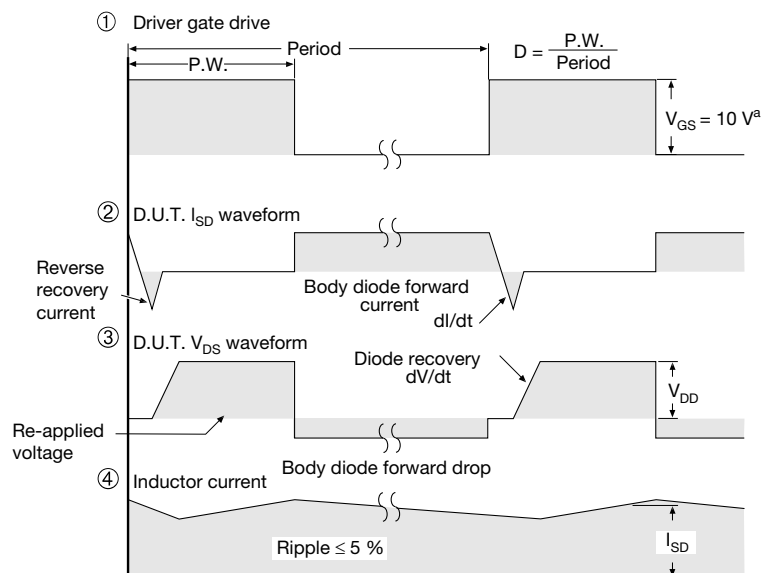
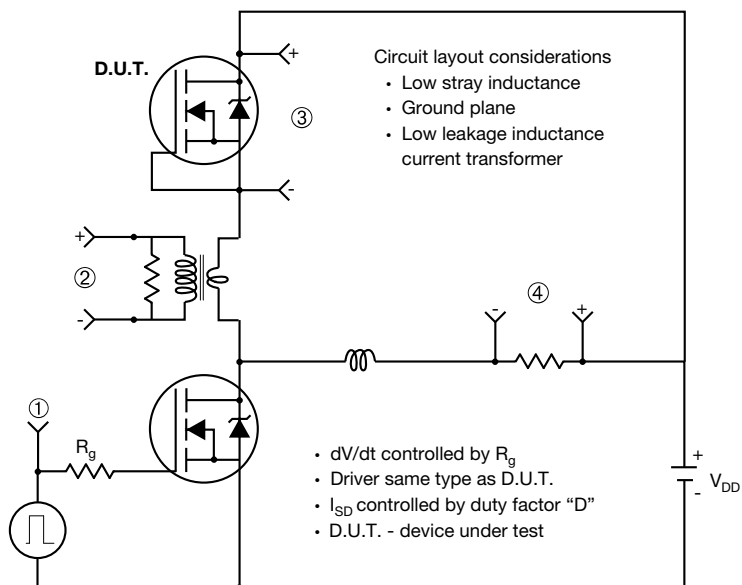


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

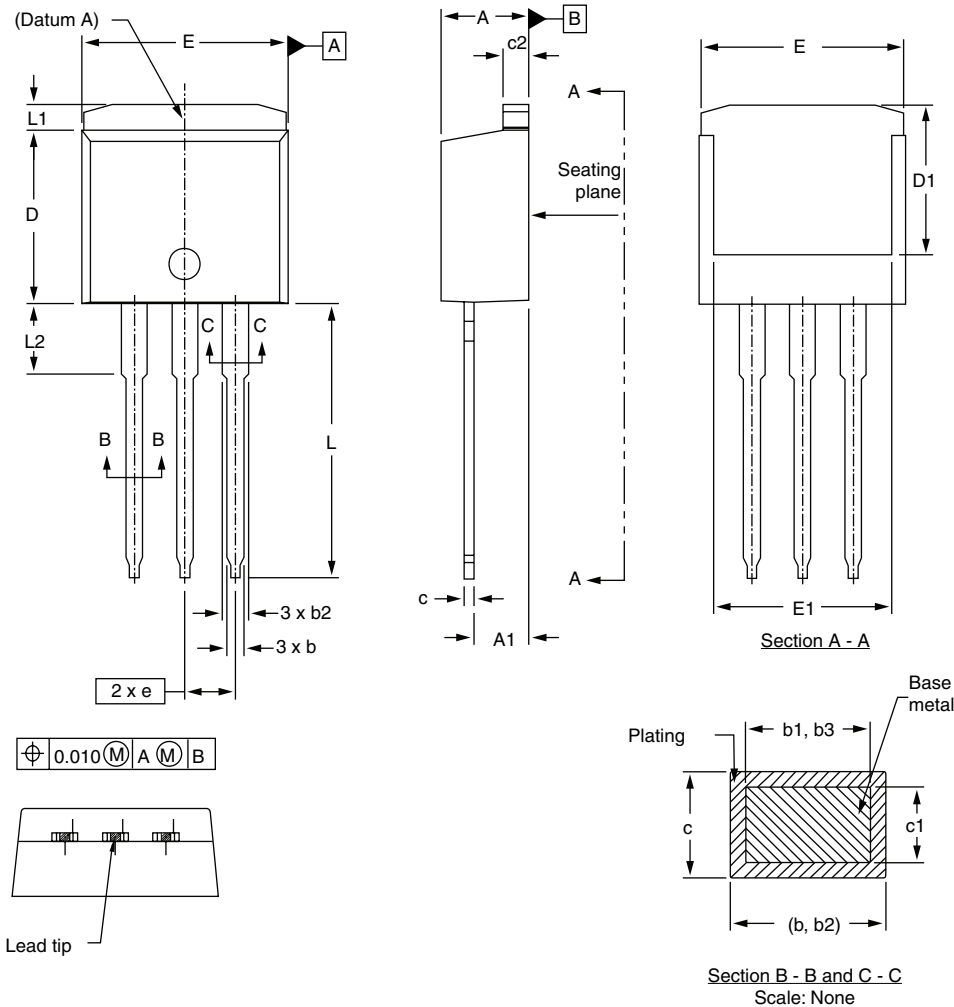


Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

I²PAK (TO-262)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

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