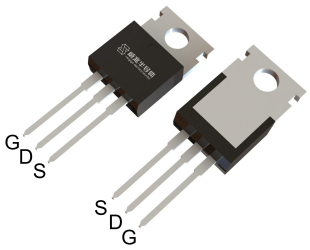
Features

V_{DS}	85	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	1.8	mΩ
$I_{D(Wire\ bond\ limited)}$	195	A

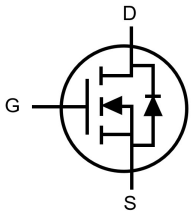
- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® Ⅱ Technology
- 100% Avalanche tested,100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TO-220AB



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS8801GTH	TO-220AB	8801GTH	50pcs/Tube



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		85	V
V_{GS}	Gate-source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	T_C=25°C	195	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	195	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 100°C	195	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	1240	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	24	A
		T_A=70°C	20	A
EAS	Maximum avalanche energy, single pulsed ②		1332	mJ
P_D	Maximum power dissipation ③	T_C=25°C	577	W
		T_C=100°C	288	W
P_{DSM}	Maximum power dissipation ④	T_A=25°C	2.5	W
		T_A=70°C	1.8	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 175	°C

Thermal characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.22	0.26	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250μA	85	95	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=85V,V_{GS}=0V	--	--	1	μA
	Zero gate voltage drain current(Tj=125℃)⑦	V_{DS}=85V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=250μA	2.6	3.1	3.6	V
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=10V, I_D=80A	--	1.8	2.3	mΩ
		Tj=100℃ ⑦	--	2.6	--	mΩ
G_{FS}	Forward transconductance	V_{DS}=5V, I_D=40A	--	94	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑦	V_{DS}=40V,V_{GS}=0V, f=100kHz	--	11385	--	pF
Coss	Output capacitance ⑦		--	2255	--	pF
Crss	Reverse transfer capacitance ⑦		--	80	--	pF
Rg	Gate resistance	f=1MHz	--	2.3	--	Ω
Qg	Total gate charge ⑦	V_{DS}=40V,I_D=80A, V_{GS}=10V	--	171	--	nC
Qgs	Gate-source charge ⑦		--	54	--	nC
Qgd	Gate-drain charge ⑦		--	40	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on delay Time	V_{DD}=40V, I_D=80A, R_G=3Ω, V_{GS}=10V	--	32	--	ns
Tr	Turn-on rise Time		--	131	--	ns
Td(off)	Turn-off delay Time		--	93	--	ns
Tf	Turn-off fall Time		--	81	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=80A,V_{GS}=0V	--	0.87	1	V
Trr	Reverse recovery time ⑦	V_{DD}=60V I_{sd}=80A, V_{GS}=0V di/dt=100A/μs	--	95	--	ns
Qrr	Reverse recovery charge ⑦		--	168	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 73A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 50A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

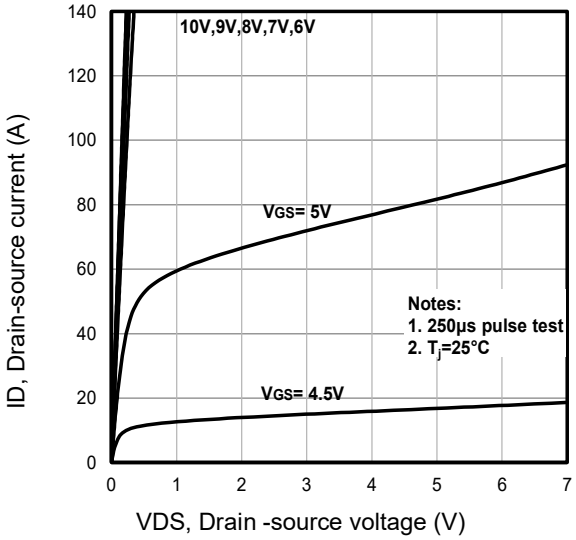


Fig1. Typical output characteristics

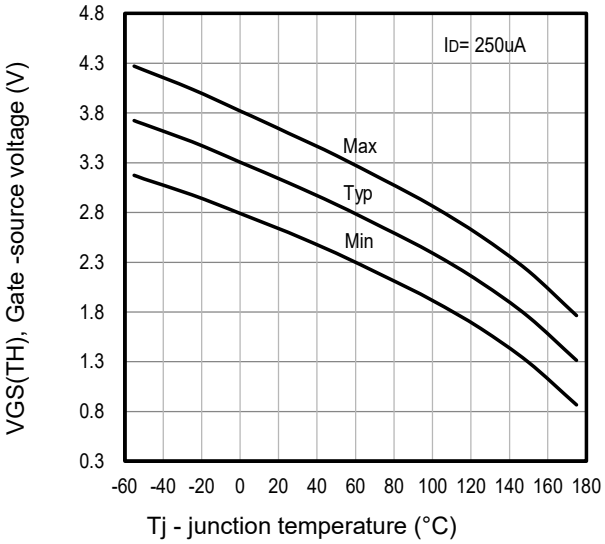


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

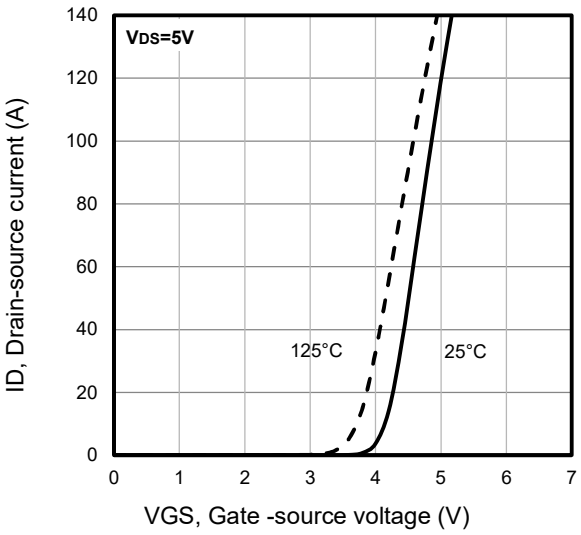


Fig3. Typical transfer characteristics

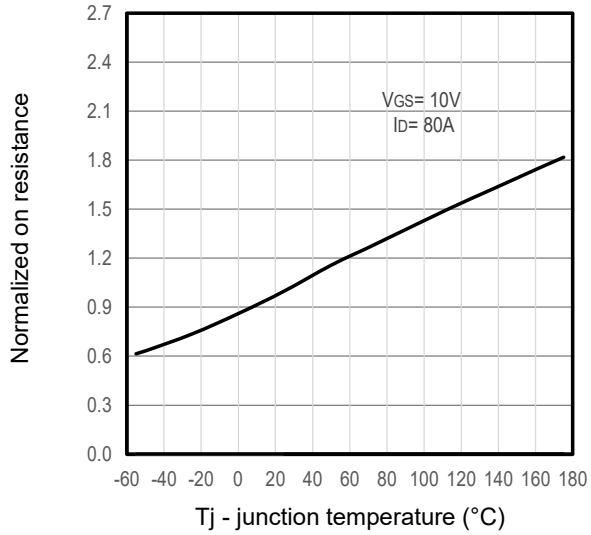


Fig4. Typical normalized on-resistance Vs. Tj

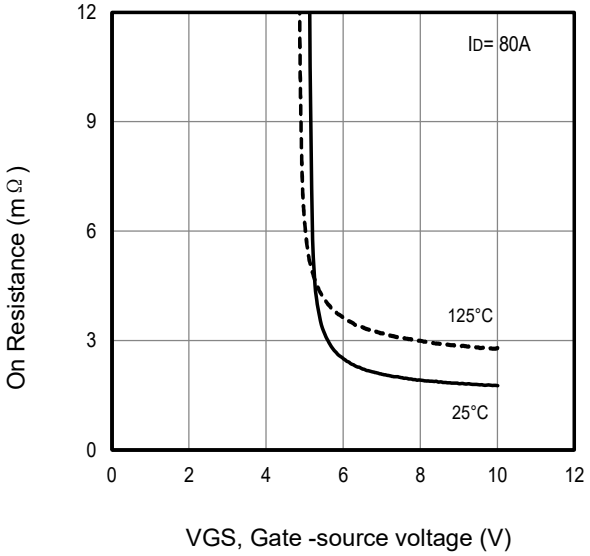


Fig5. Typical on resistance Vs gate -source voltage

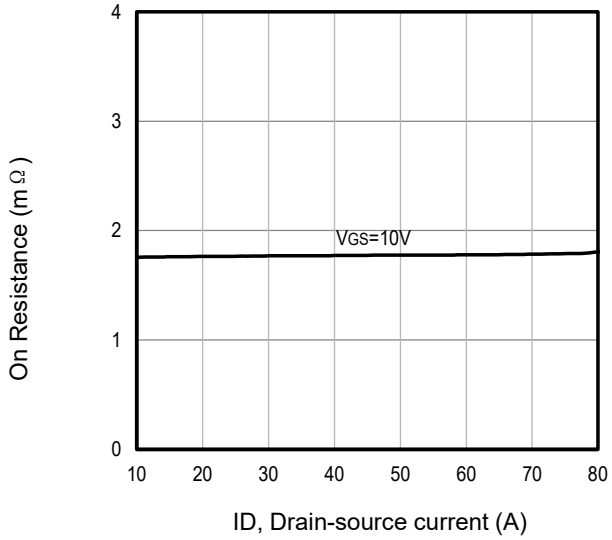


Fig6. Typical on resistance Vs drain current

Typical Characteristics

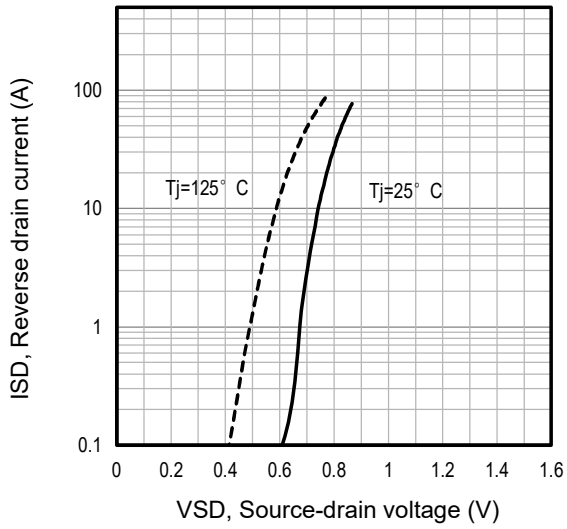


Fig7. Typical source-drain diode forward voltage

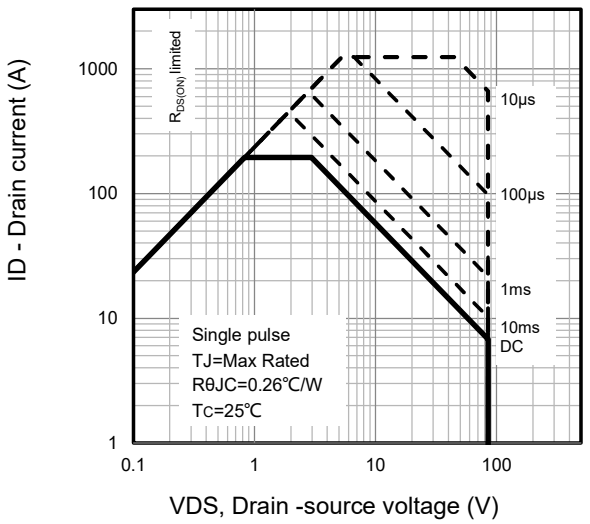


Fig8. Maximum safe operating area

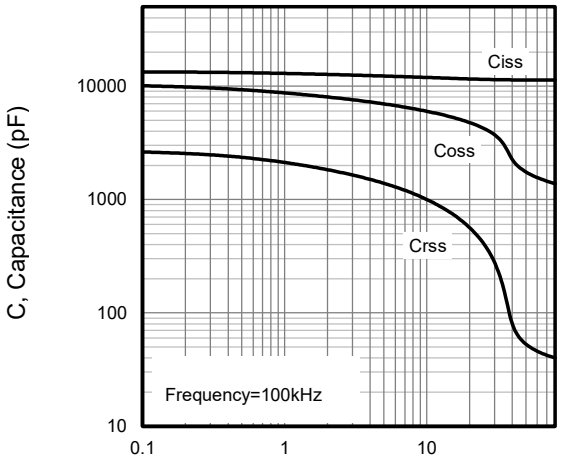


Fig9. Typical capacitance Vs. drain-source voltage

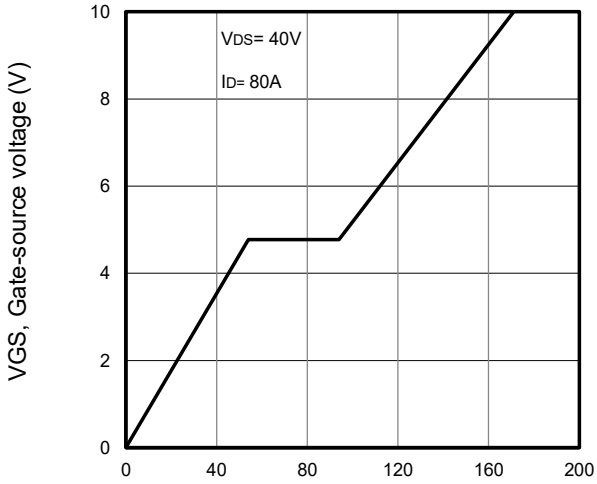


Fig10. Typical gate charge Vs. gate-source voltage

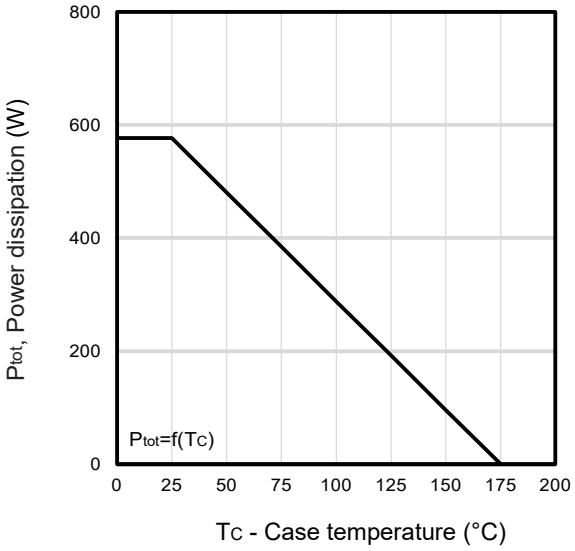


Fig11. Power dissipation Vs. case temperature

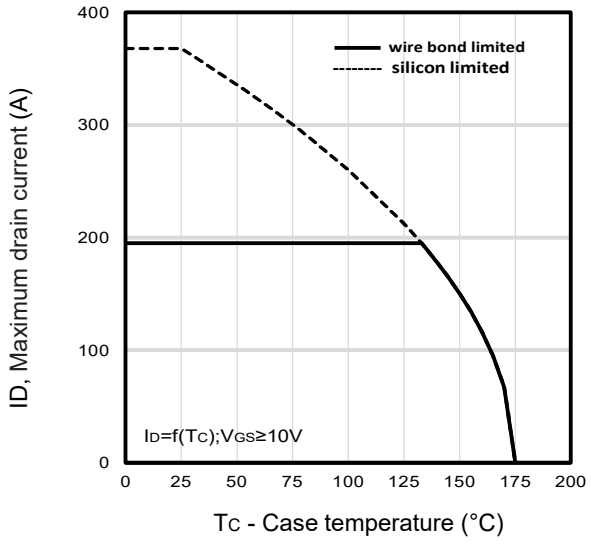


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

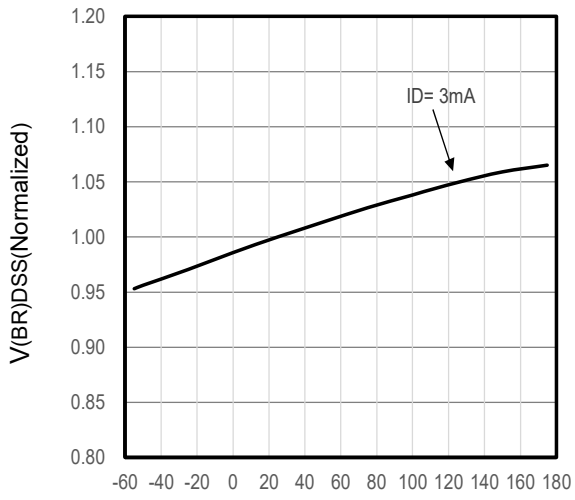


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

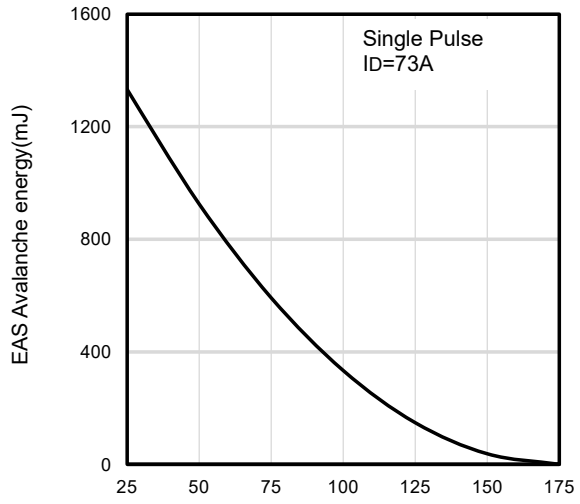


Fig14. Maximum avalanche energy vs temperature (°C)

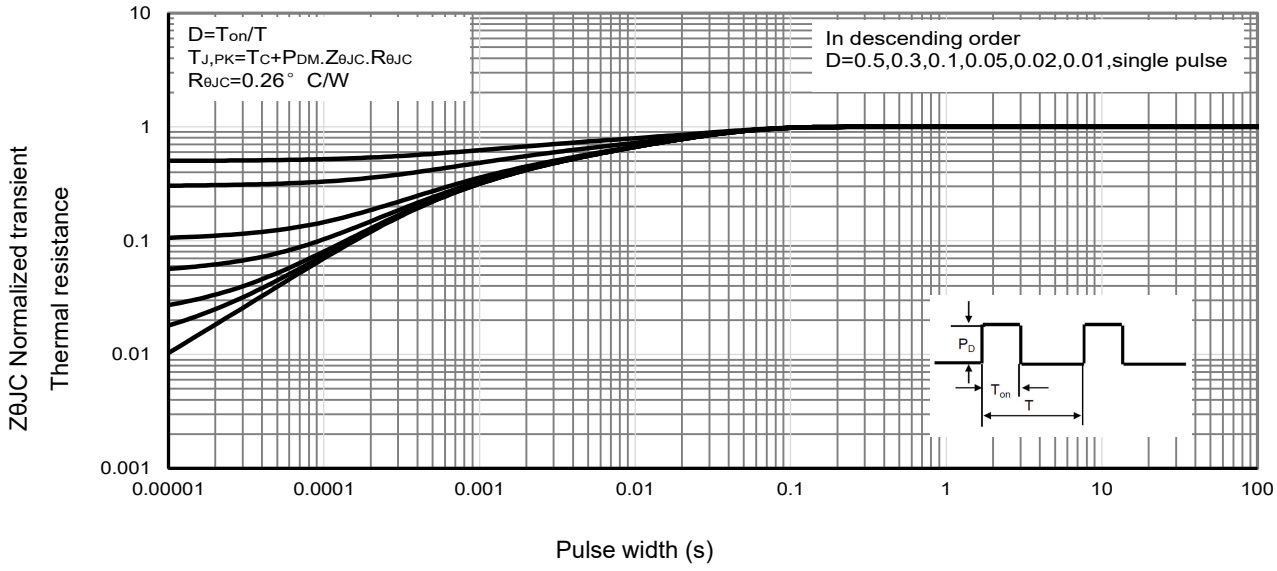


Fig15 . Normalized maximum transient thermal impedance

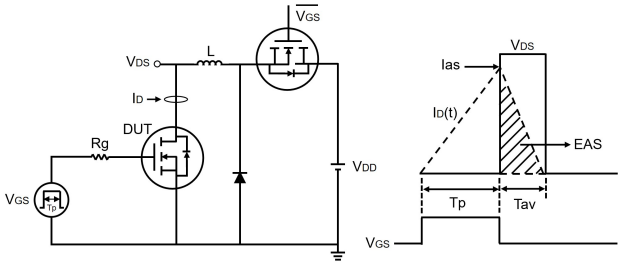


Fig16. Unclamped inductive test circuit and waveforms

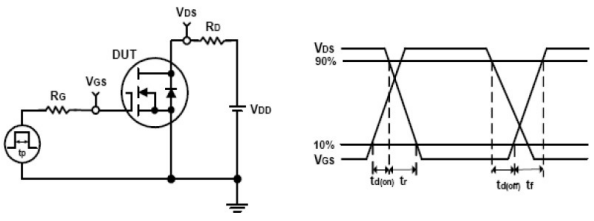
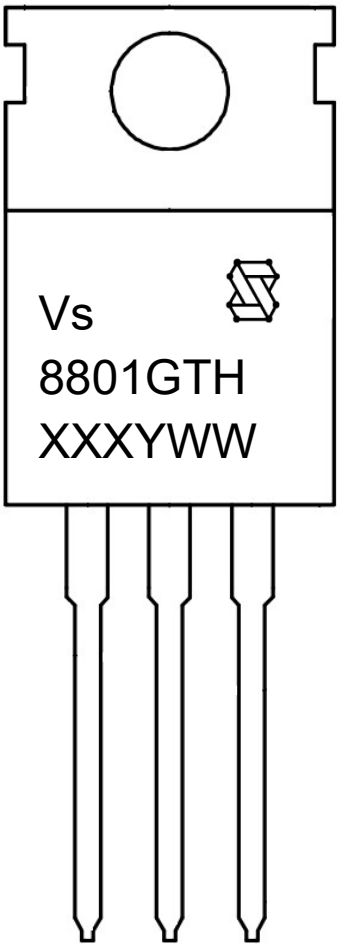


Fig17. Switching time test circuit and waveforms

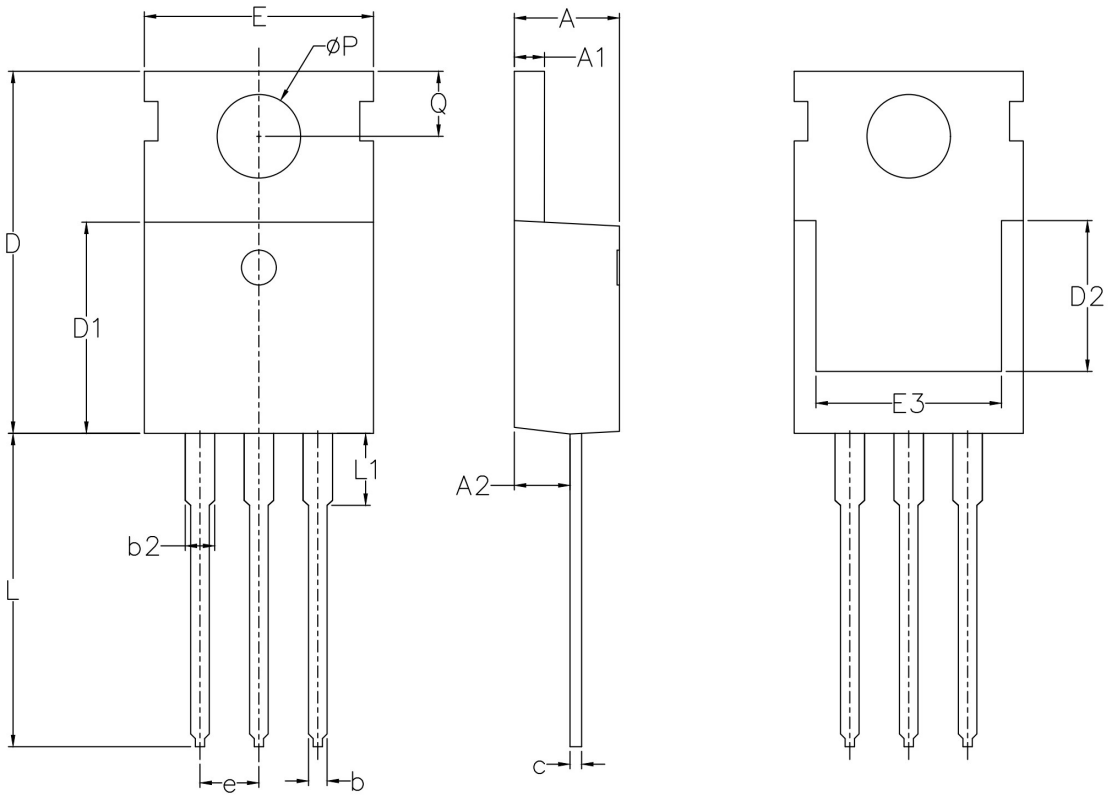
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（8801GTH）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.35	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.27	1.47
c	0.45	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	--	--
E	9.70	10.00	10.30
E3	7.00	--	--
e	2.54 BSC		
L	12.75	13.50	13.85
L1	--	3.10	3.40
Q	2.60	2.80	3.00
ΦP	3.40	3.60	3.80

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.