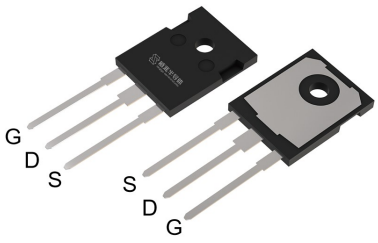
Features

V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	1.8	mΩ
$I_{D(Wire\ bond\ Limited)}$	260	A

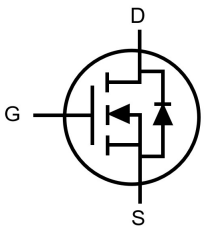
- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested,100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TO-247



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS1891GUH	TO-247	1891GUH	30pcs/Tube



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	T_C = 25°C	260	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	260	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	211	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	844	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	26	A
		T_A = 70°C	21	A
EAS	Maximum Avalanche energy, single pulsed ②		1406	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	441	W
		T_C = 100°C	221	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	3.3	W
		T_A = 70°C	2.1	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.28	0.34	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	32	38	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)⑦	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3.0	3.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=80A	--	1.8	2.4	mΩ
		Tj=100℃ ⑦	--	2.7	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=50V,V_{GS}=0V, f=100KHz	--	12375	--	pF
Coss	Output Capacitance ⑦		--	1785	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	40	--	pF
Rg	Gate Resistance	f=1MHz	--	2.1	--	Ω
Qg	Total Gate Charge ⑦	V_{DS}=50V,I_D=80A, V_{GS}=10V	--	196	--	nC
Qgs	Gate-Source Charge ⑦		--	57	--	nC
Qgd	Gate-Drain Charge ⑦		--	47	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=50V, I_D=80A, R_G=3Ω, V_{GS}=10V	--	37	--	ns
Tr	Turn-on Rise Time		--	133	--	ns
Td(off)	Turn-Off Delay Time		--	110	--	ns
Tf	Turn-Off Fall Time		--	102	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=80A,V_{GS}=0V	--	0.85	1	V
Trr	Reverse Recovery Time ⑦	V_{DD}=60V, I_{sd}=80A, V_{GS}=0V di/dt=100A/μs	--	95	--	ns
Qrr	Reverse Recovery Charge ⑦		--	194	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 52A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

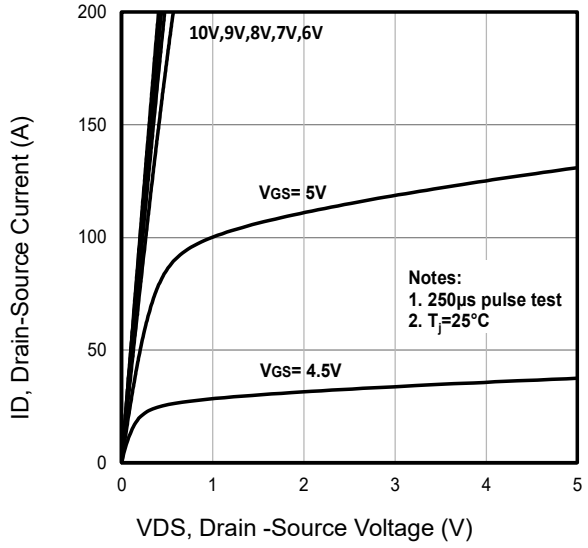


Fig1. Typical Output Characteristics

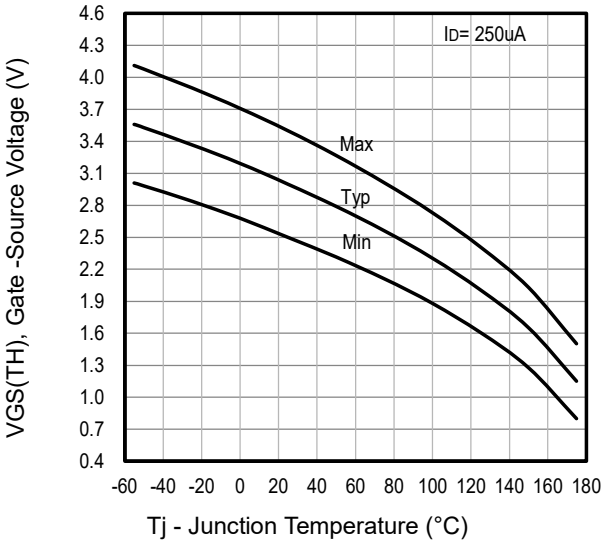


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

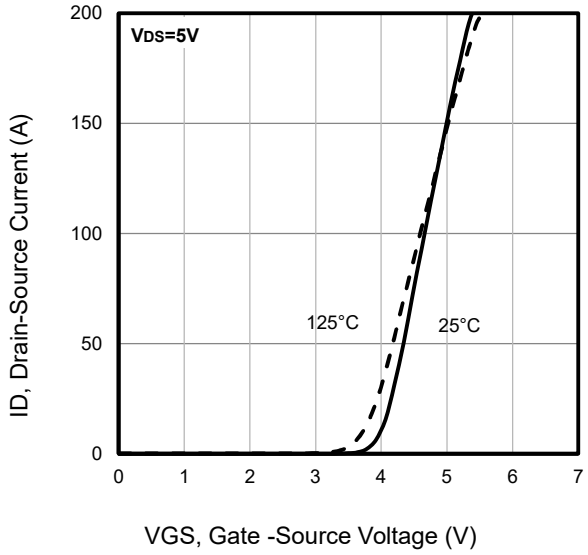


Fig3. Typical Transfer Characteristics

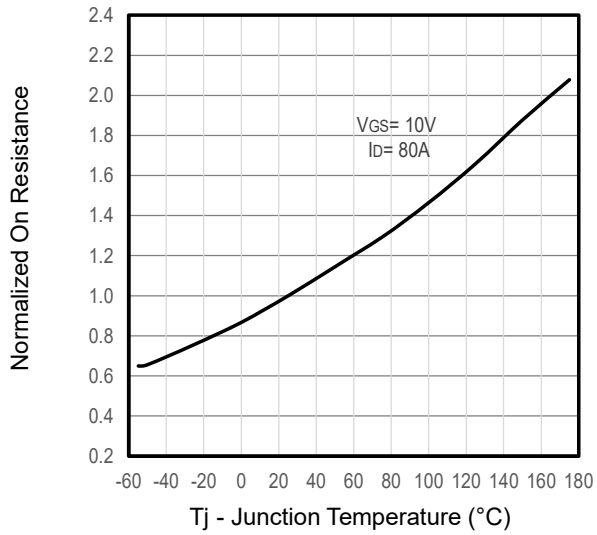


Fig4. Typical Normalized On-Resistance Vs. Tj

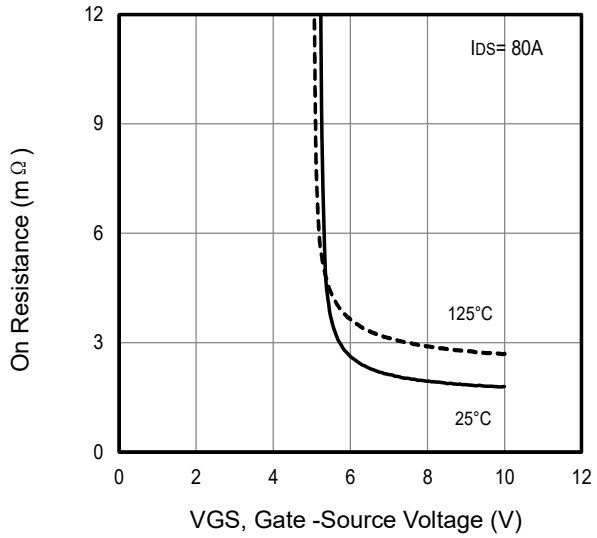


Fig5. Typical On Resistance Vs Gate -Source Voltage

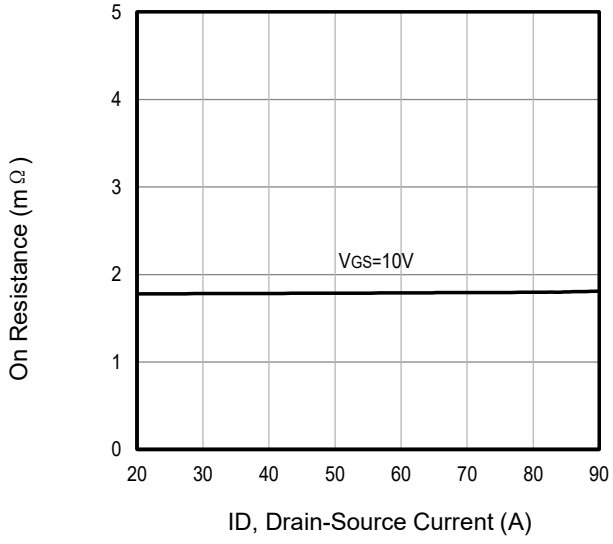


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

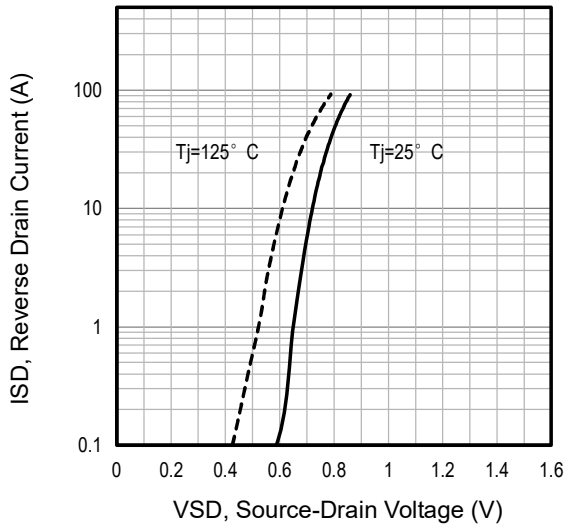


Fig7. Typical Source-Drain Diode Forward Voltage

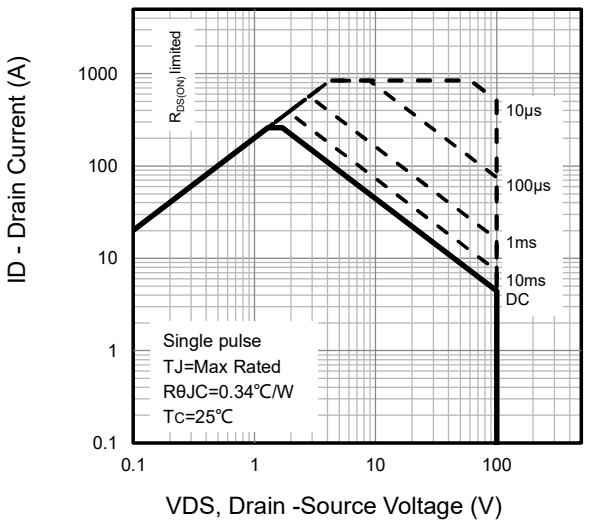


Fig8. Maximum Safe Operating Area

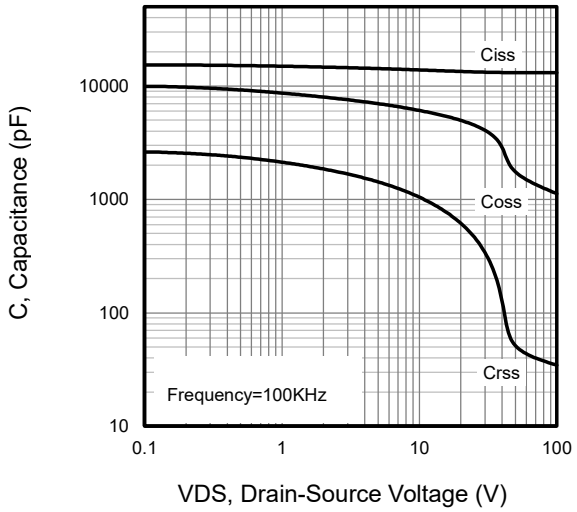


Fig9. Typical Capacitance Vs. Drain-Source Voltage

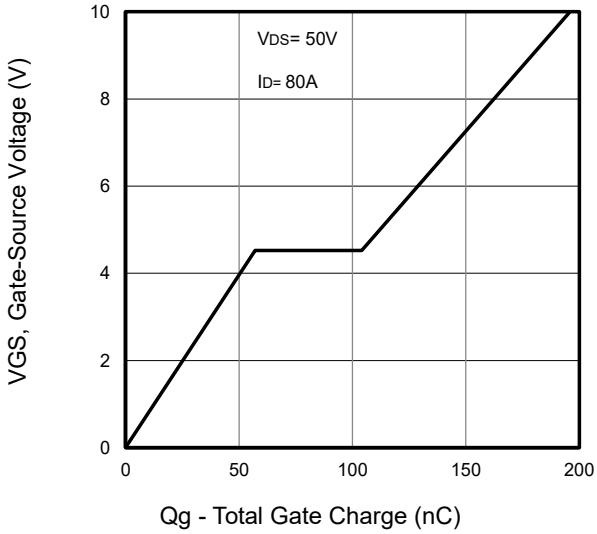


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

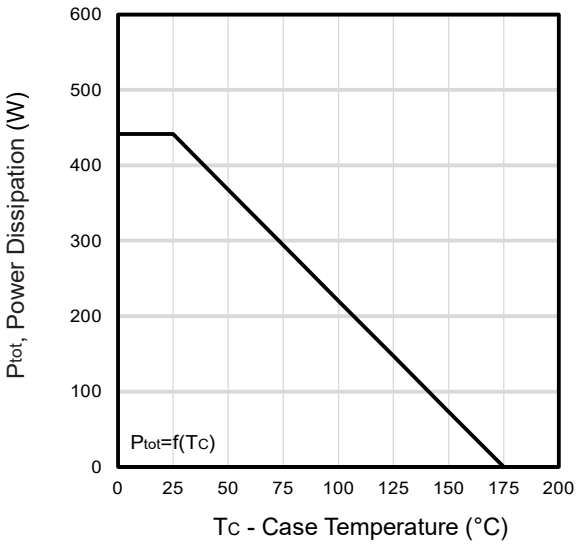


Fig11. Power Dissipation Vs. Case Temperature

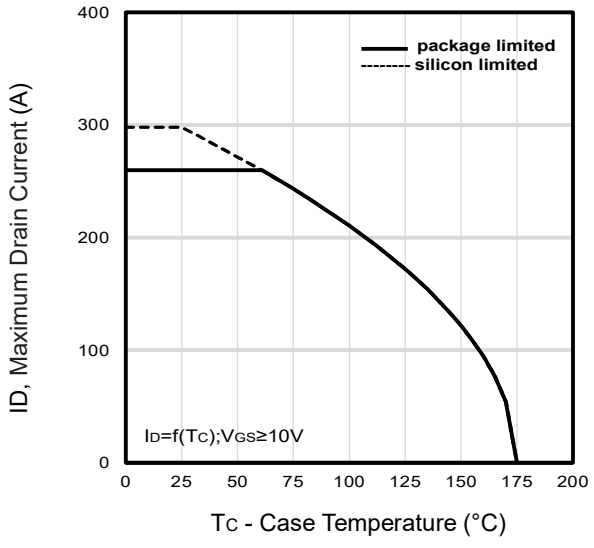


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

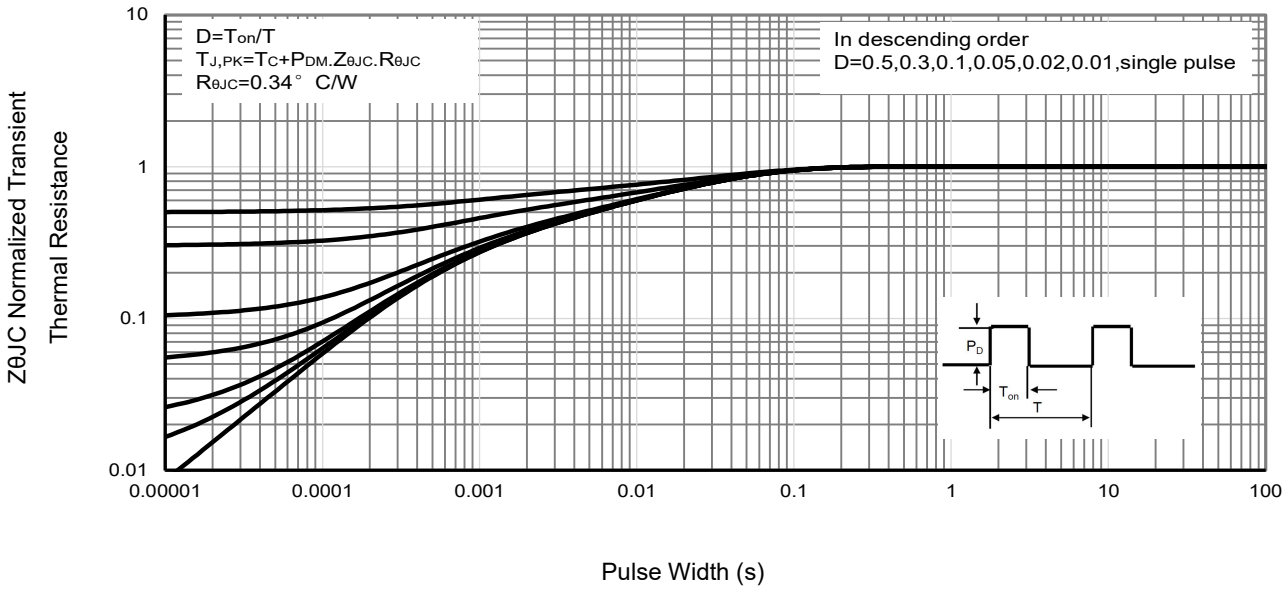


Fig13 . Normalized Maximum Transient Thermal Impedance

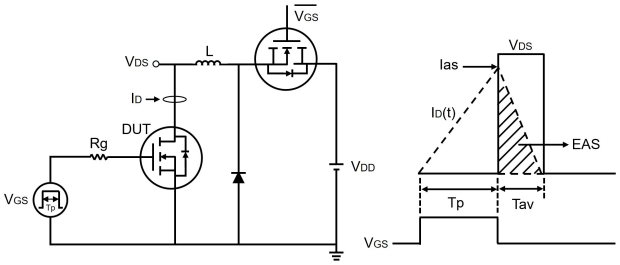


Fig14. Unclamped Inductive Test Circuit and waveforms

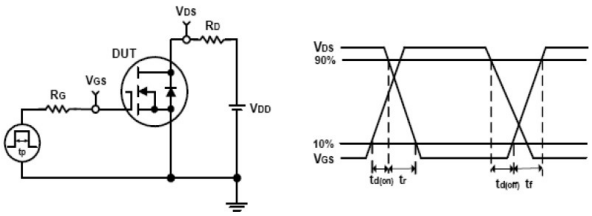
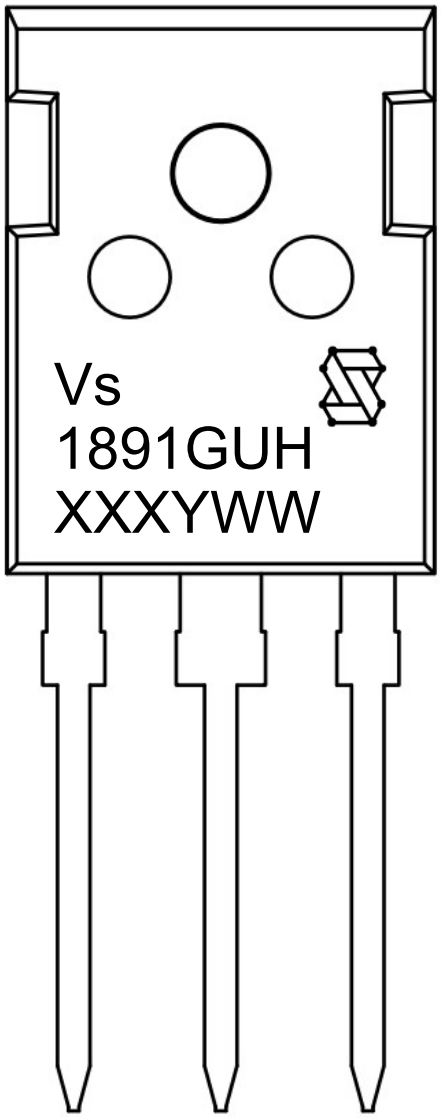


Fig15. Switching Time Test Circuit and waveforms

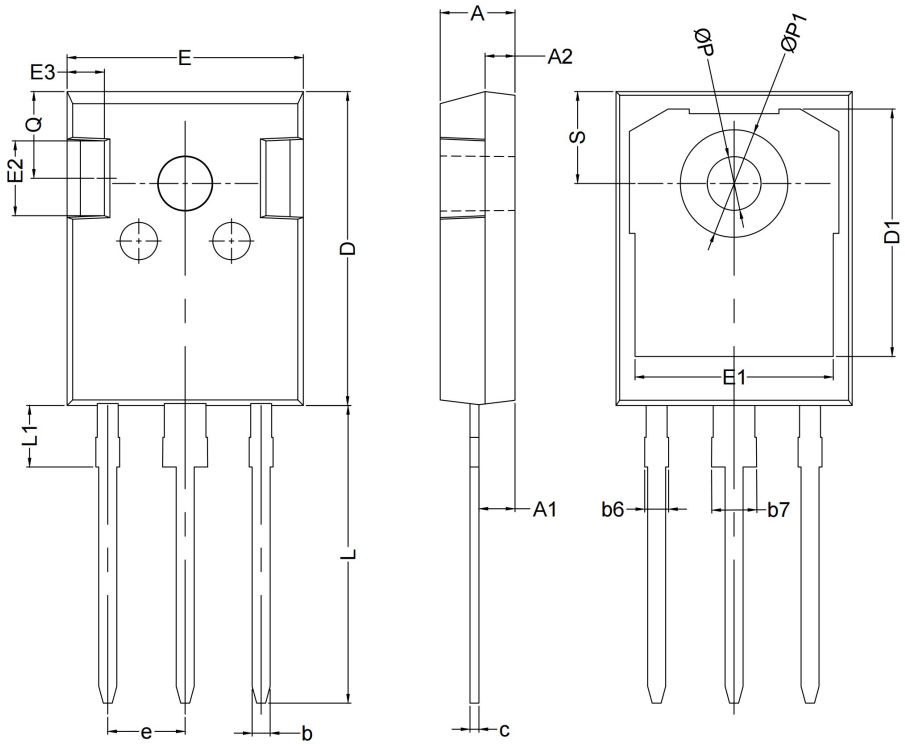
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（1891GUH）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-247 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Nom	Max
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16	--	1.26
b6	--	--	2.25
b7	--	--	3.25
c	0.59	--	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.40	4.50	4.60
E3	1.50	1.60	1.70
e	5.44 BSC		
L	19.80	19.92	20.10
L1	--	--	4.30
ΦP	3.40	3.50	3.60
ΦP1	7.00	--	7.40
Q	5.60	--	6.00
S	6.05	6.15	6.25

Notes:

1. Package Reference: JEDEC TO-247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.