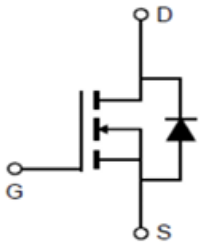
General Description:

The LWN6045AL uses trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT23-3L, which accords with the ROHS standard and Halogen Free standard.

V_{DSS}	60	V
I_D	5.5	A
P_D	2.0	W
$R_{DS(ON)\ TYPE}$	33	mΩ

Marking and Pin Assignment

Inner Equivalent Principium Chart



Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Applications:

- DC-DC Converter
- Portable Equipment
- Power Management

RoHS HF

Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
6045A	LWN6045AL	SOT23-3L	Reel	3000 Pcs

Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		60	V
I_D	Continuous Drain Current	T_A=25℃	5.5	A
	Continuous Drain Current	T_A=100℃	3.4	A
I_{DM}[a1]	Pulsed Drain Current		22	A
V_{GS}	Gate-to-Source Voltage		±20	V
P_D	Power Dissipation		2.0	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JA}$[a2]	Thermal Resistance, Junction-to-Ambient	62.5	℃/W

Electrical Characteristic (T_J = 25 °C, unless otherwise specified):

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=60V, V_{GS}=0V	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V, V_{DS}=0V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V, V_{DS}=0V	--	--	-100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.1	1.6	2.1	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=10V, I_D=5.0A	--	33	45	mΩ
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=4.5V, I_D=3.0A	--	38	55	mΩ

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} =0V V_{DS} =30V f =1.0MHz	--	971	--	pF
C_{oss}	Output Capacitance		--	40	--	
C_{rss}	Reverse Transfer Capacitance		--	37	--	
R_G	Gate resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	--	1.4	--	Ω

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =5.0A V_{DS} =30V V_{GS} =10V R_G =3.0Ω	--	8.0	--	ns
t_r	Rise Time		--	3.6	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	19.2	--	
t_f	Fall Time		--	3.2	--	
Q_g	Total Gate Charge	V_{GS} =10V V_{DS} =30V I_D =5.0A	--	23	--	nC
Q_{gs}	Gate to Source Charge		--	2.7	--	
Q_{gd}	Gate to Drain Charge		--	5.0	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_A =25 °C	--	--	5.5	A
I_{SM}	Diode Pluse Current		--	--	22	A
V_{SD}	Diode Forward Voltage	I_S=5.0A, V_{GS}=0V	--	--	1.2	V

a1：Repetitive rating; pulse width limited by maximum junction temperature

a2：Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection.

Characteristics Curve：

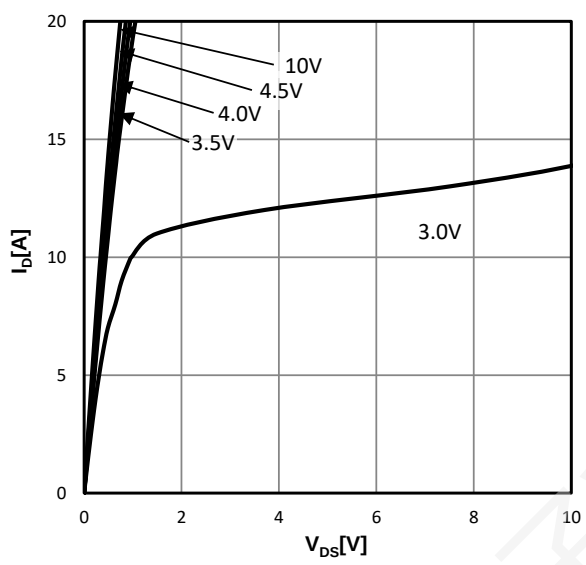
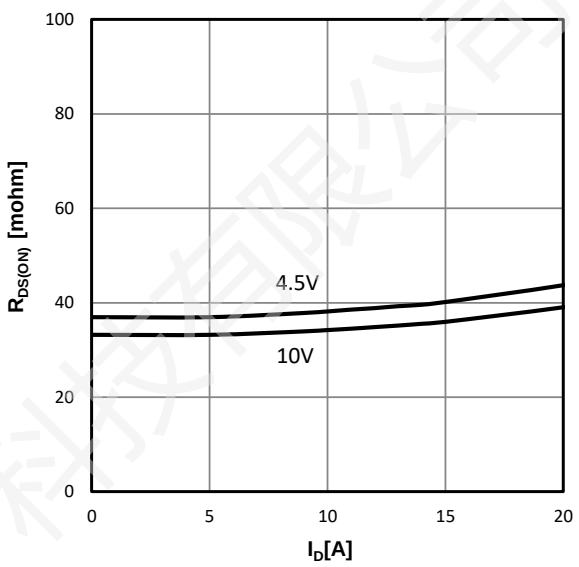
Figure 1: Typ. output characteristics	Figure 2: Typ. drain-source on resistance
	
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

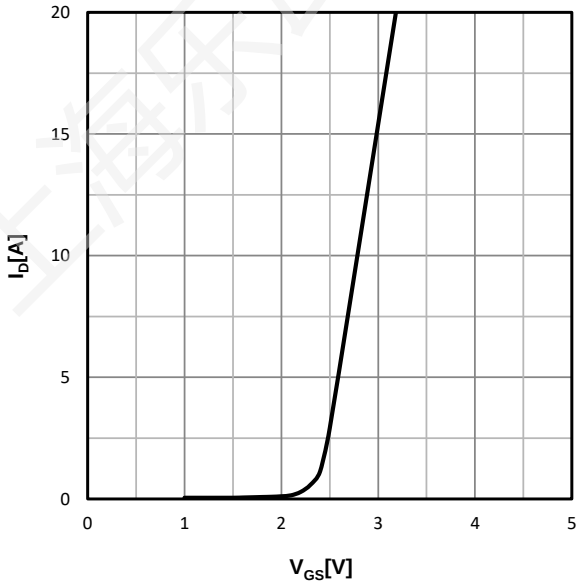
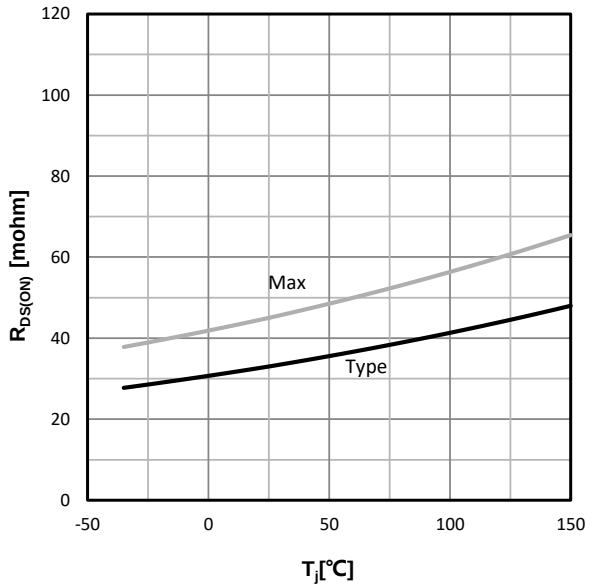
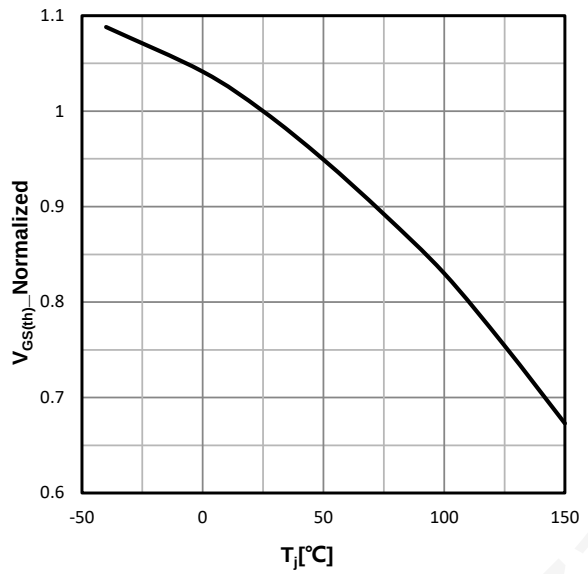
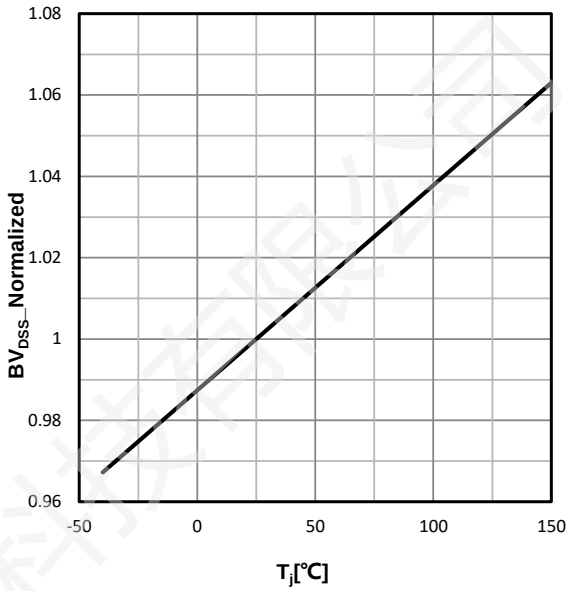
Figure 3: Typ. transfer characteristics	Figure 4: drain-source on resistance
	
$I_D=f(V_{GS})$, $\|V_{DS}\|>2\|I_D\|R_{DS}(on)max$;	$R_{DS(on)}=f(T_j)$, I_D=5.0A, V_{GS}=10V;

Figure 5: Typ. gate threshold voltage



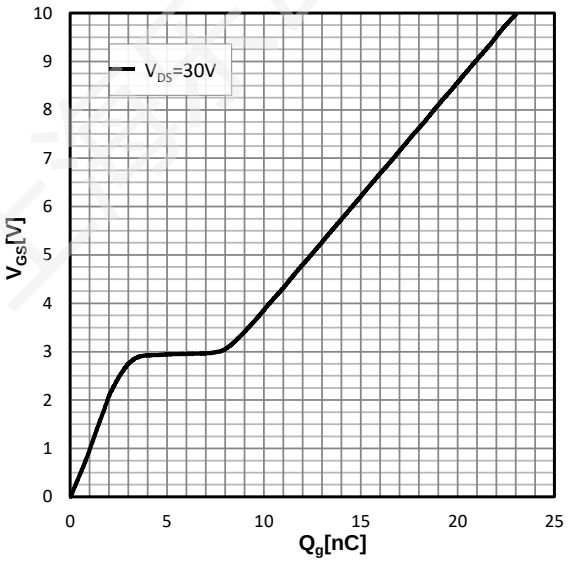
$V_{GS}=f(T_j)$,I $V_{GS}=V_{DS,}I_D=250\mu A$;

Figure 6: Drain-source breakdown voltage



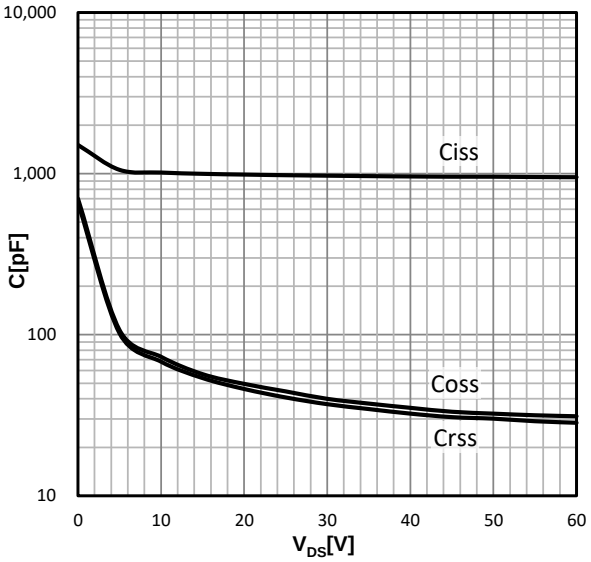
$V_{BR(DSS)}=f(T_j)$; $I_D=250\mu A$;

Figure 7: Typ. gate charge



$V_{GS}=f(Q_g)$, $I_D=5.0A$, $T_j=25$ °C; parameter: V_{DS}

Figure 8: Typ. Capacitances



$C=f(V_{DS})$; $V_{GS}=0V$; f=1.0 MHz;

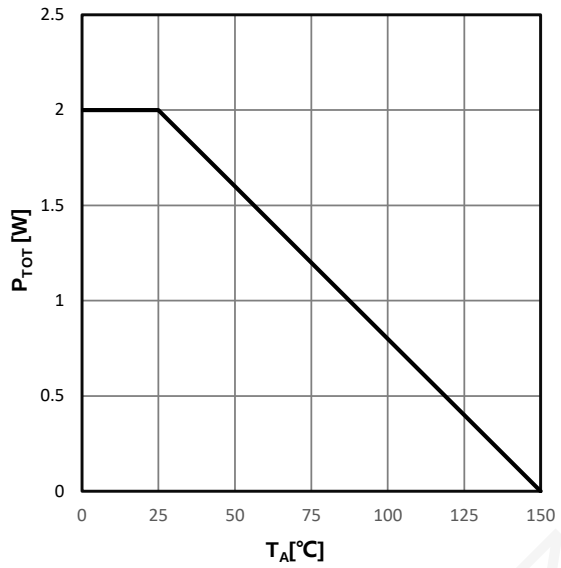
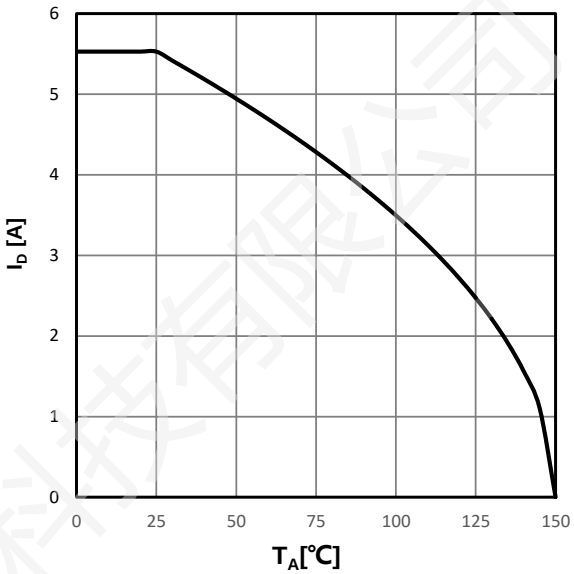
Figure 9: Power dissipation	Figure 10:Drain current
	
$P_{tot}=f(T_A)$;	$I_D=f(T_A)$;

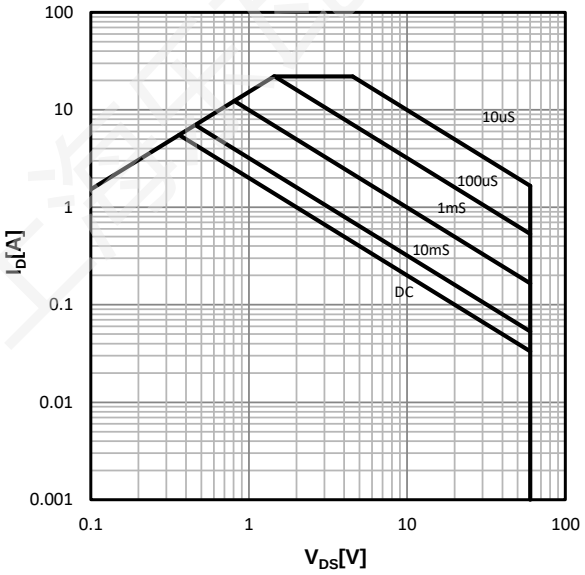
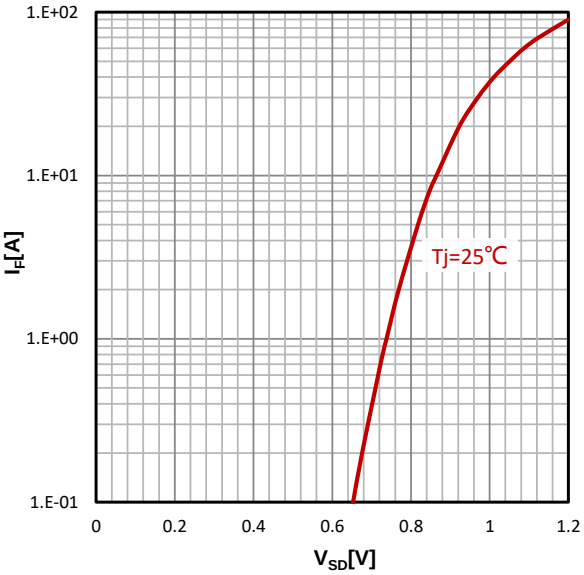
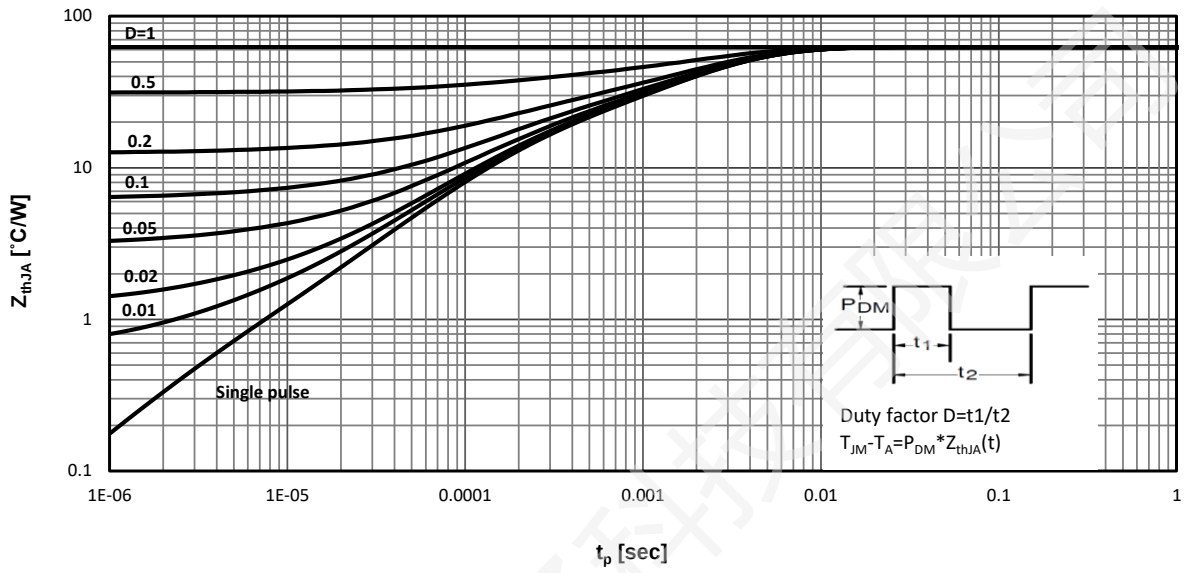
Figure 11: Safe operating area	Figure 12: Typ. forward characteristics
	
$I_D=f(V_{DS})$; T_A=25 °C; D=0; parameter: tp	$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJA}=f(t_p)$; parameter: D

Test Circuit & Waveform:

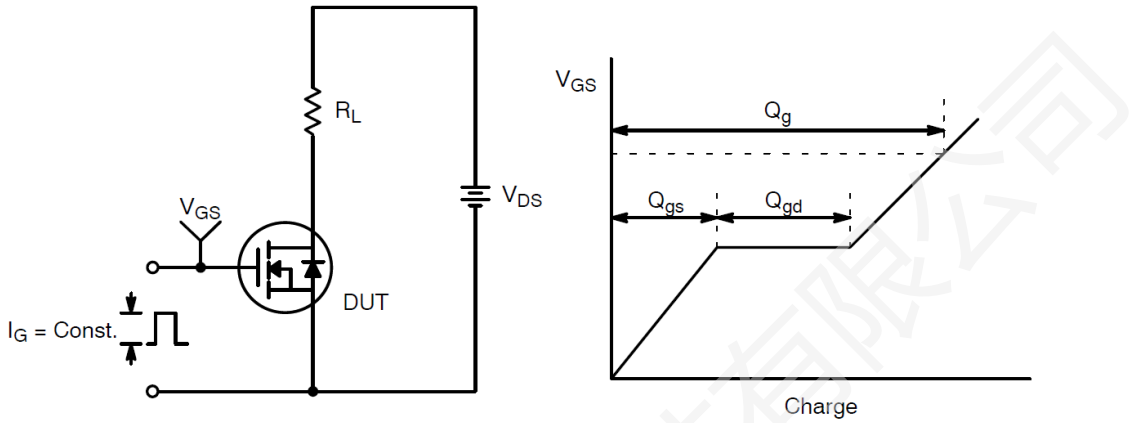


Figure 14: Gate Charge Test Circuit & Waveform

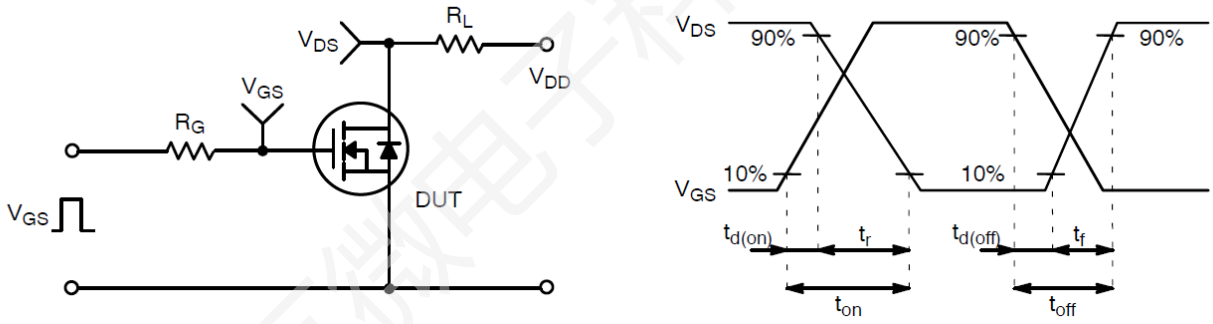


Figure 15: Resistive Switching Test Circuit & Waveforms

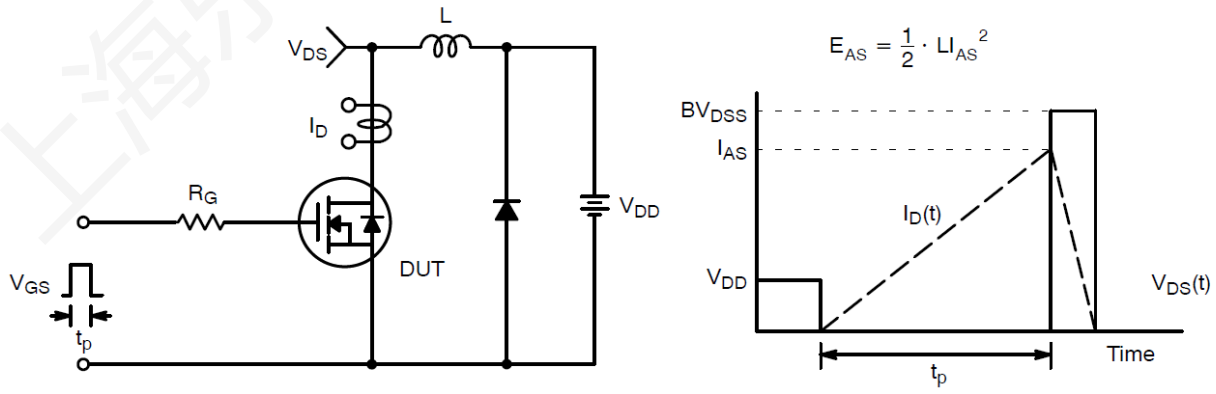
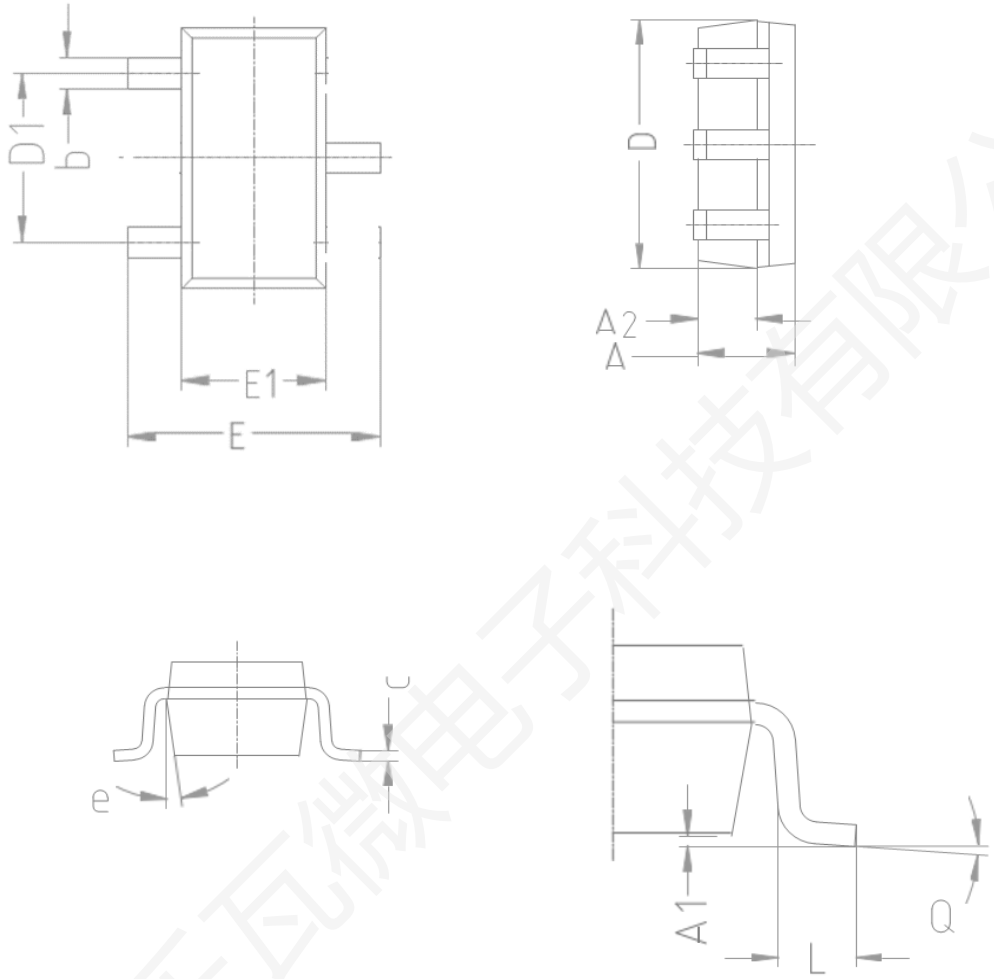


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:



COMMON DIMENSION (MM)			
PKG	SOT23-3L		
Symbol	**MIN**	**NOM**	**MAX**
A	1.050	1.100	1.150
A1	0.010	0.060	0.150
A2	0.640	0.670	0.700
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.925	2.980
D1	1.800	1.900	2.000
E	2.650	2.825	3.000
E1	1.550	1.610	1.670
L	0.300	0.450	0.600
e	8°		
Q	0°	4°	8°

Revision History:

Revison	Date	Descriptions
Rev 1.0	July.2025	Initial Version

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