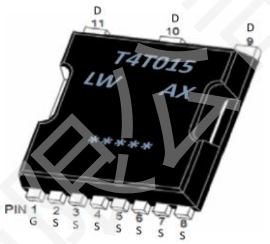
General Description:

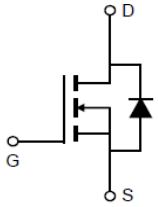
The LWT4T015AX uses SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is TOLL, which accords with the ROHS standard and Halogen Free standard.

V_{DSS}	40	V
I_D	200	A
P_D	167	W
$R_{DS(ON)\ TYPE}$	1.1	mΩ

Marking and Pin Assignment



Inner Equivalent Principium Chart



Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Applications:

- DC-DC Converter
- Portable Equipment
- Power Management

100% DVDS Tested

100% Avalanche Tested

Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
T4T015/LW AX/D.C.	LWT4T015AX	TOLL	Reel	2000 Pcs

Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		40	V
I_D	Continuous Drain Current	T_C=25℃	200	A
	Continuous Drain Current	T_C=100℃	127	A
I_{DM}[a1]	Pulsed Drain Current		800	A
E_{AS}[a2]	Single pulse avalanche energy		400	mJ
V_{GS}	Gate-to-Source Voltage		±20	V
P_D	Power Dissipation		167	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.75	℃/W
$R_{\theta JA}$[a3]	Thermal Resistance, Junction-to-Ambient	40	℃/W

Electrical Characteristic (T_J = 25 °C, unless otherwise specified):

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=40V, V_{GS}=0V	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V, V_{DS}=0V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V, V_{DS}=0V	--	--	-100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.3	1.7	2.1	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=10V, I_D=20A	--	1.1	1.5	mΩ
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=4.5V, I_D=15A	--	1.5	2.0	mΩ
g_{FS}	Forward Transconductance	V_{DS}=10V,I_D=20A	--	100	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} =0V V_{DS} =20V f =1.0MHz	--	5842	--	pF
C_{oss}	Output Capacitance		--	1859	--	
C_{rss}	Reverse Transfer Capacitance		--	210	--	
R_G	Gate resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	--	2.3	--	Ω

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =20A V_{DS} =20V V_{GS} =10V R_G =1.6Ω	--	15	--	ns
t_r	Rise Time		--	36	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	68	--	
t_f	Fall Time		--	35	--	
Q_g	Total Gate Charge	V_{GS} =10V V_{DS} =20V I_D =20A	--	100	--	nC
Q_{gs}	Gate to Source Charge		--	16	--	
Q_{gd}	Gate to Drain Charge		--	18	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_C =25 °C	--	--	200	A
V_{SD}	Diode Forward Voltage	I_S=20A, V_{GS}=0V	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_S=20A, V_{DD}=20V dI/dt=100A/μs	--	48	--	ns
Q_{rr}	Reverse Recovery Charge		--	39	--	nC

a1：Repetitive rating; pulse width limited by maximum junction temperature

a2：V_{DD}=30V, L=0.1mH, R_G=25Ω, Starting T_J=25 ℃

a3：Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection.

Characteristics Curve：

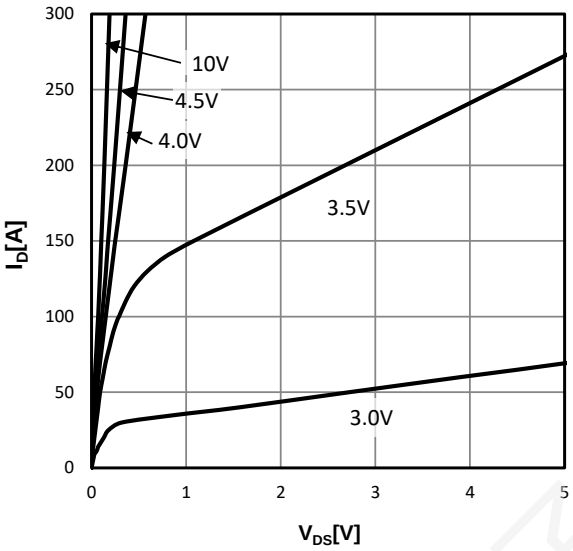
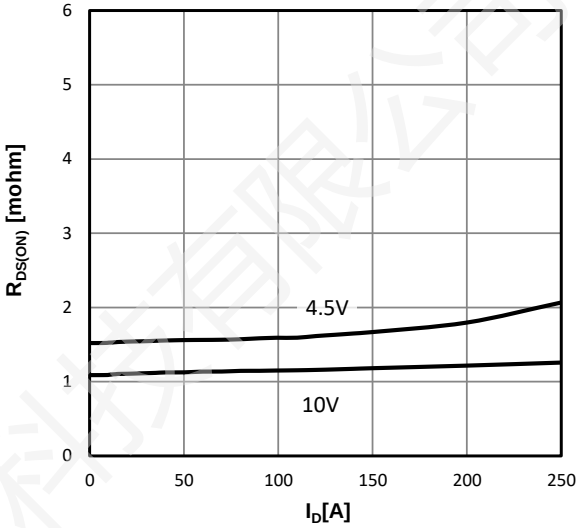
Figure 1: Typ. output characteristics	Figure 2: Typ. drain-source on resistance
	
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

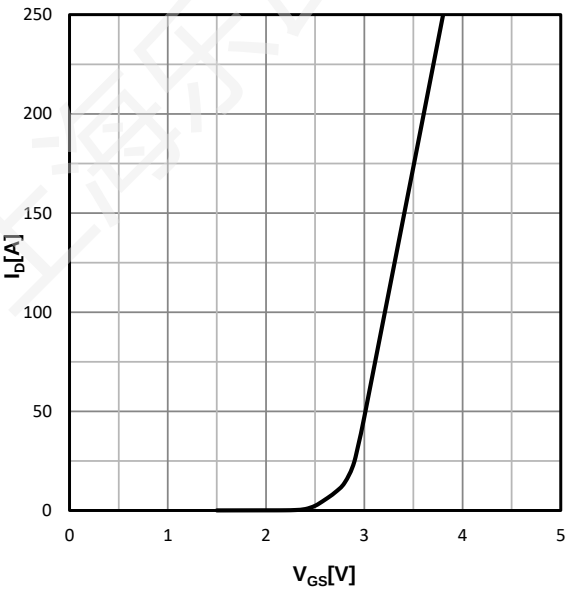
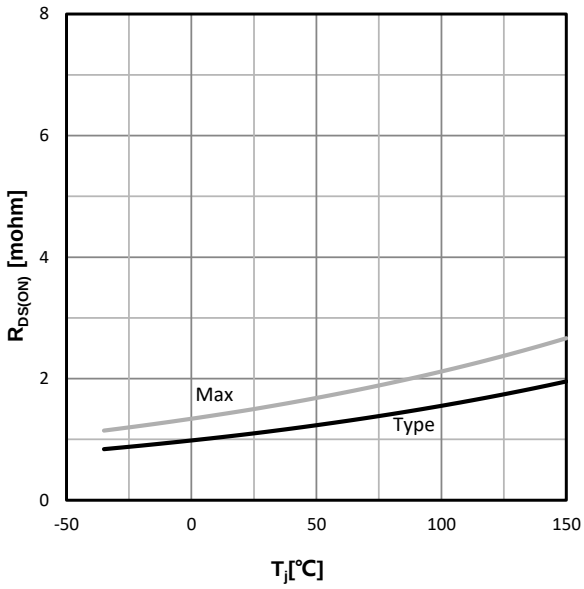
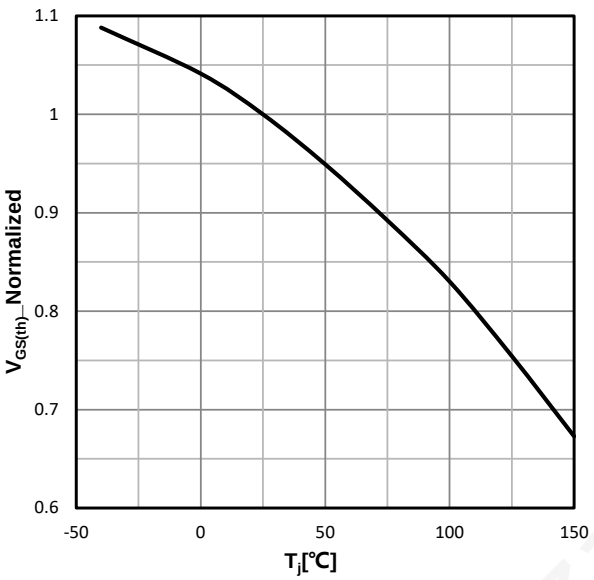
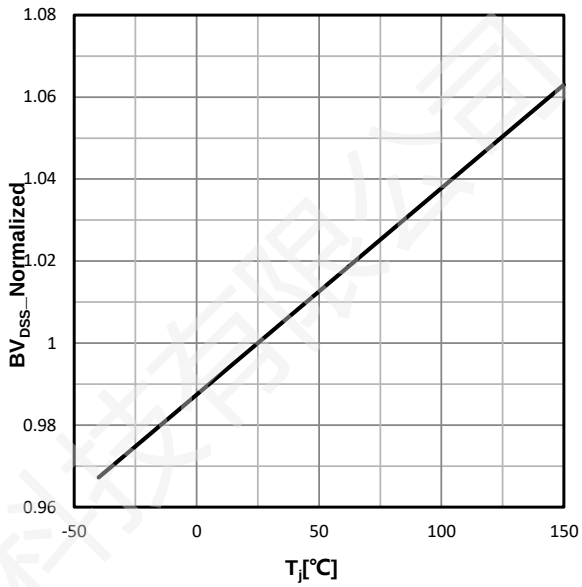
Figure 3: Typ. transfer characteristics	Figure 4: drain-source on resistance
	
$I_D=f(V_{GS})$, $\|V_{DS}\|>2\|I_D\|R_{DS}(on)max$;	$R_{DS(on)}=f(T_j)$, I_D=20A, V_{GS}=10V;

Figure 5: Typ. gate threshold voltage



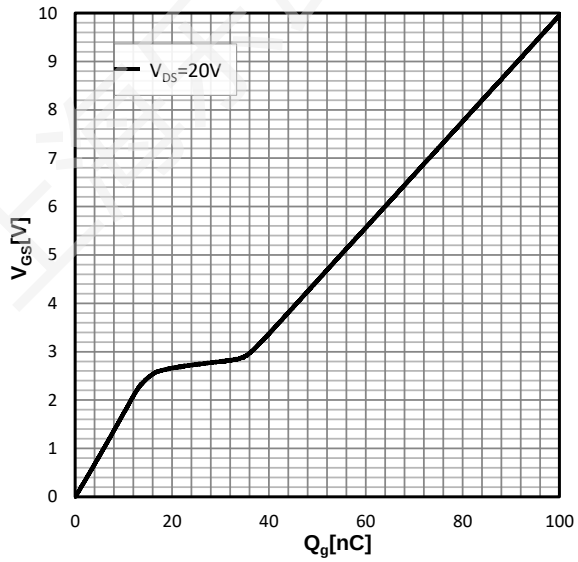
$V_{GS}=f(T_j)$,I $V_{GS}=V_{DS,}I_D=250\mu A$;

Figure 6: Drain-source breakdown voltage



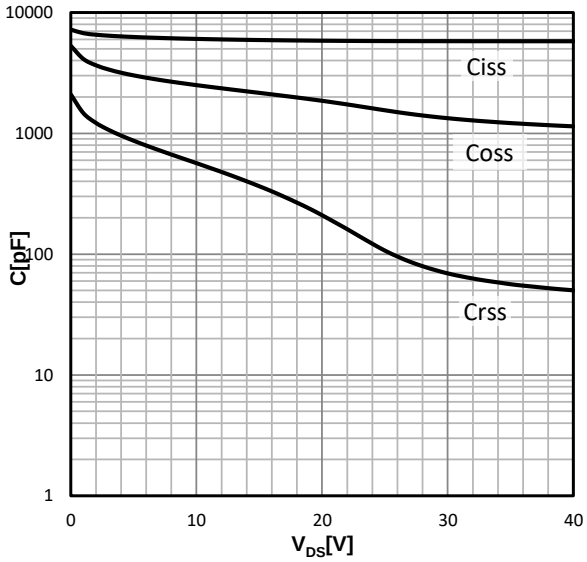
$V_{BR(DSS)}=f(T_j)$; $I_D=250\mu A$;

Figure 7: Typ. gate charge



$V_{GS}=f(Q_g)$, $I_D=20A$, $T_j=25$ °C; parameter: V_{DS}

Figure 8: Typ. Capacitances



$C=f(V_{DS})$; $V_{GS}=0V$; f=1.0 MHz;

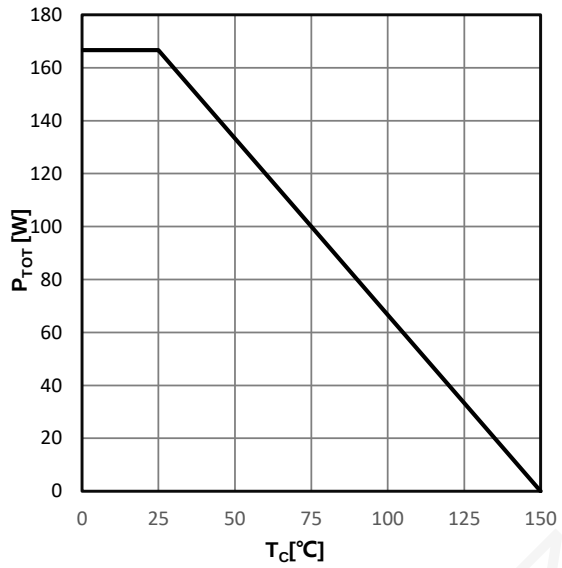
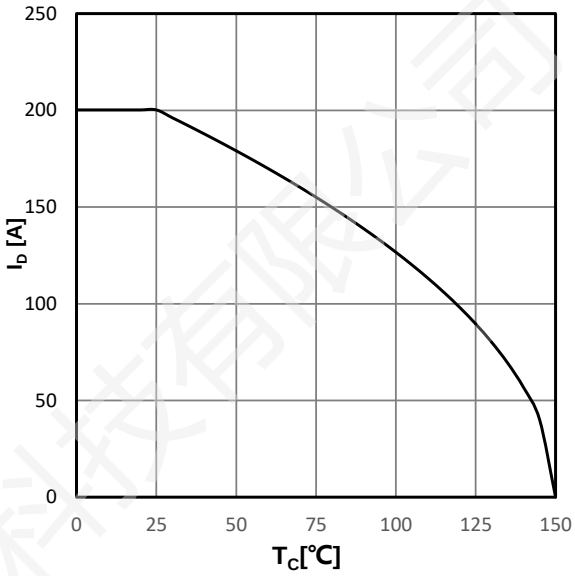
Figure 9: Power dissipation	Figure 10:Drain current
	
$P_{tot}=f(T_C)$;	$I_D=f(T_C)$;

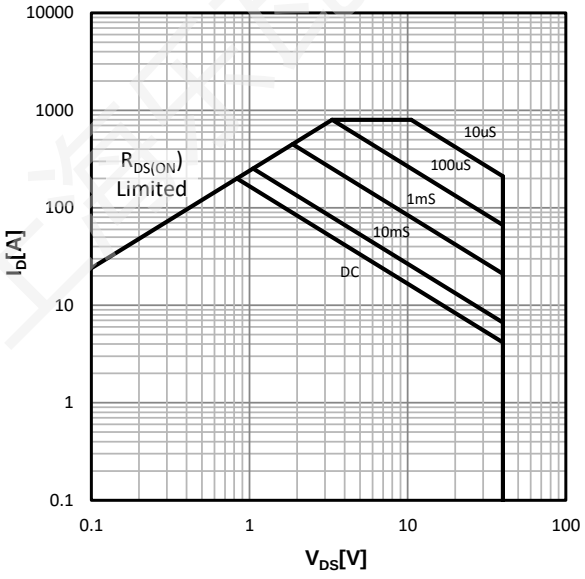
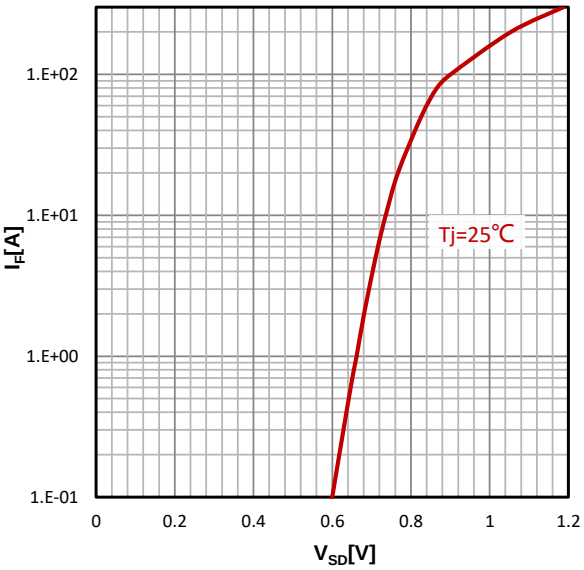
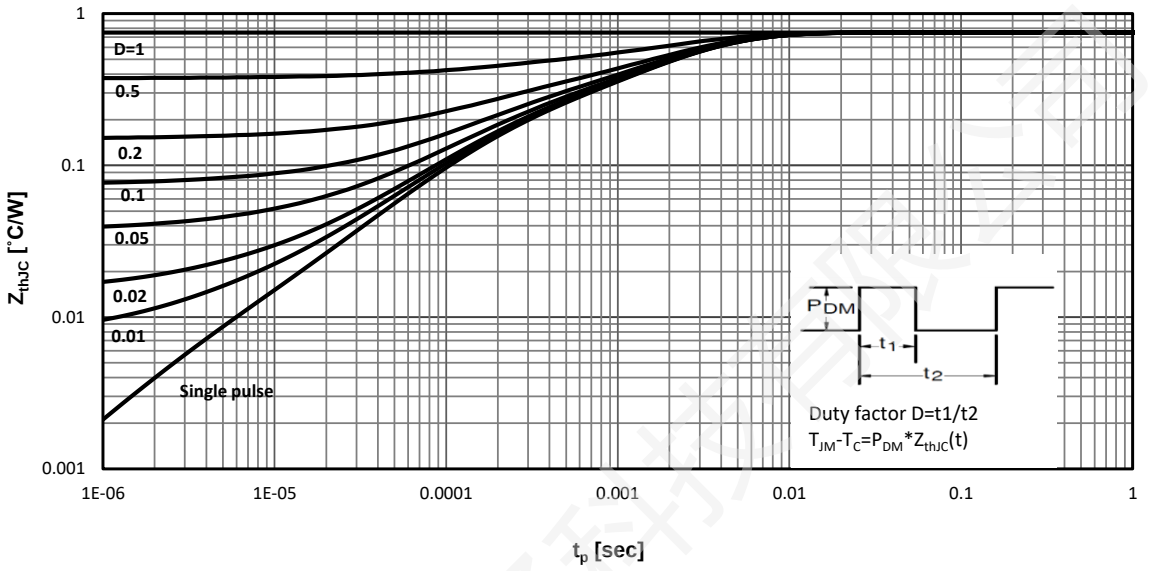
Figure 11: Safe operating area	Figure 12: Typ. forward characteristics
	
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: tp	$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJC}=f(t_p)$; parameter: D

Test Circuit & Waveform:

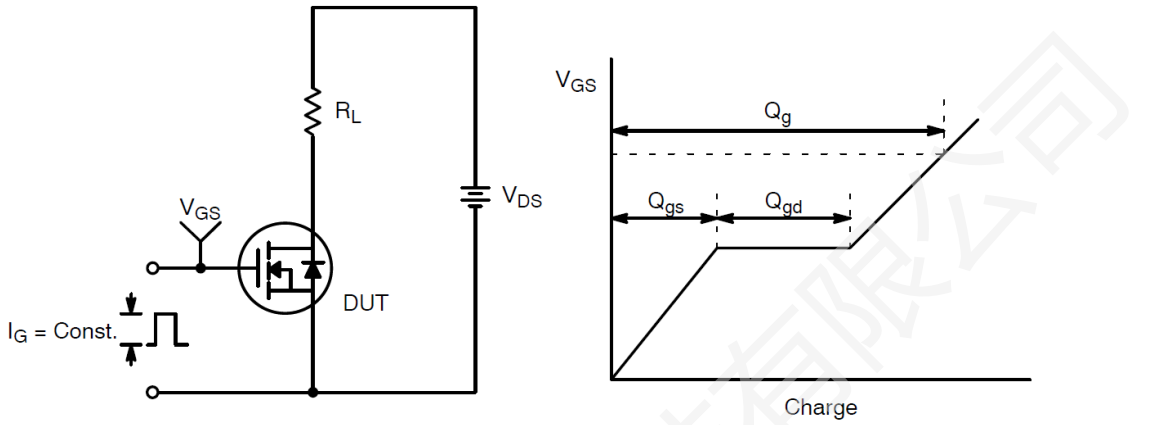


Figure 14: Gate Charge Test Circuit & Waveform

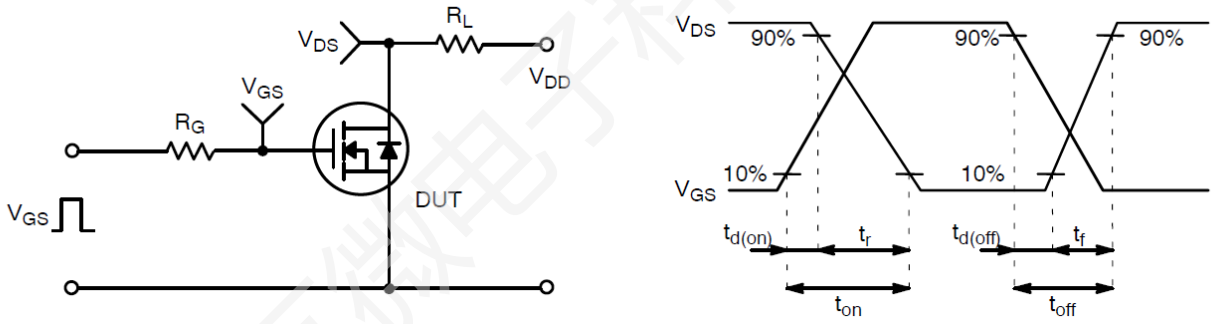


Figure 15: Resistive Switching Test Circuit & Waveforms

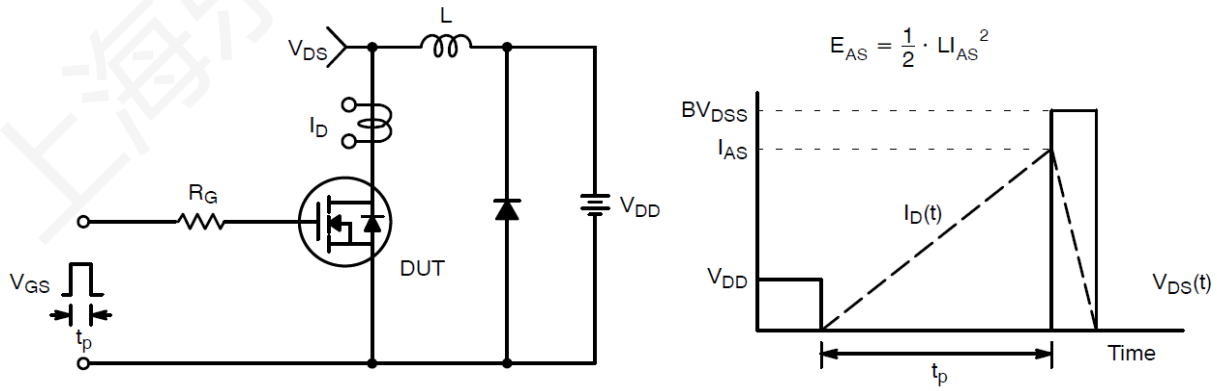
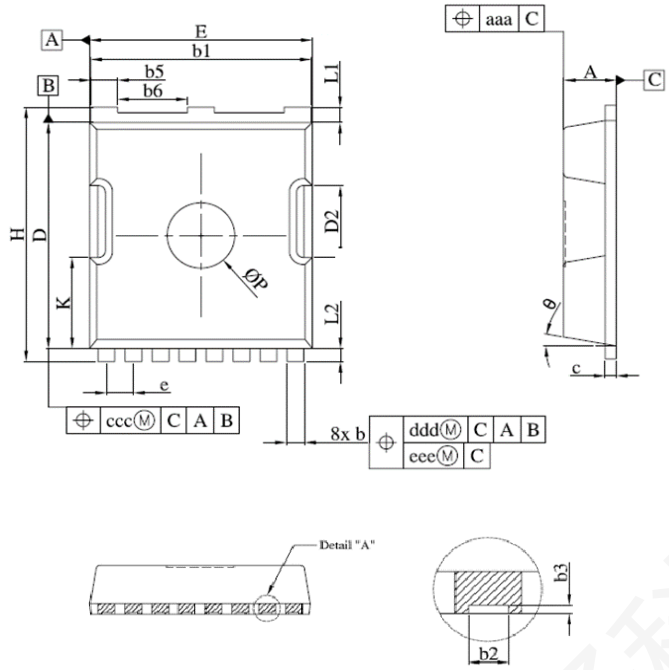


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:



SYMBOL	COMMON		
	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.45	0.55
b3	0.05	0.10	0.35
b4	0.30	0.40	0.50
b5	1.10	1.20	1.30
b6	3.00	3.10	3.20
c	0.40	0.50	0.60
D	10.28	10.38	10.55
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	7.00	7.15	7.30
D4	3.44	3.59	3.74
e	1.10	1.20	1.30
E	9.80	9.90	10.00
E1	8.20	8.30	8.40
E2	8.35	8.50	8.65
H	11.50	11.68	11.85
K	4.08	4.18	4.28
K1	2.45	-	-
L	1.60	1.90	2.10
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.30
L4	0.13	0.23	0.33
P	2.85	3.00	3.15
θ	10°REF		
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.20		

Revision History:

Revison	Date	Descriptions
Rev 1.0	May.2025	Initial Version

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