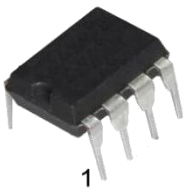
LM2660 Switched Capacitor Voltage Converter

Features

- Inverts or Doubles Input Supply Voltage
- Narrow SOP-8 Packages
- 8-Ω Typical Output Resistance
- 88% Typical Conversion Efficiency at 100 mA
- Selectable Oscillator Frequency: 10 kHz/80 kHz
- Optional External Oscillator Input



DIP-8

SOP-8

MSOP-8

DFN-8 3*3

Applications

- Laptop Computers
- Cellular Phones
- Medical Instruments
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
LM2660N/HG	DIP-8	LM2660	TUBE	2000pcs/reel
LM2660M/TR-HG	SOP-8	LM2660	REEL	2500pcs/reel
LM2660MM/TR-HG	MSOP-8	LM2660,2660	REEL	3000pcs/reel
LM2660DQ3/TR-HG	DFN-8 3*3	LM2660,2660	REEL	5000pcs/reel

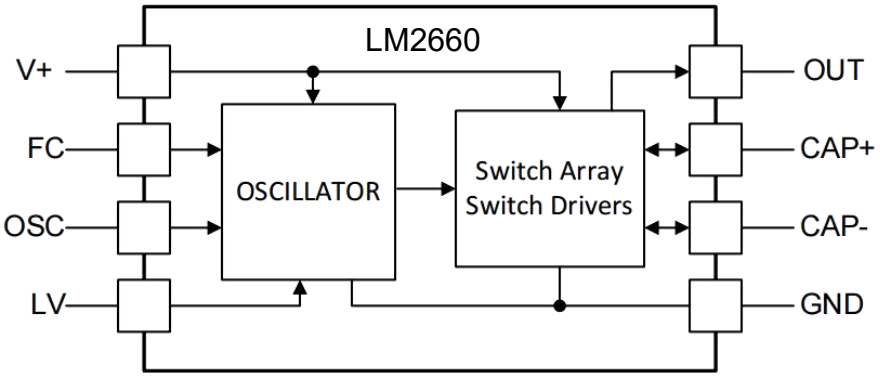
Description

The LM2660 CMOS charge-pump voltage converter is a versatile unregulated switched capacitor inverter or doubler. Operating from a wide 1.5V to 5.5V supply voltage, the LM2660 uses two low-cost capacitors to provide 100 mA of output current without the cost,size and EMI related to inductor- based converters. With an operating current of only120 μA and operating efficiency greater than 90% at most loads, the LM2660 provides ideal performance for battery-powered systems. LM2660 devices can be operated directly in parallel to lower output impedance, thus providing more current at a given voltage.

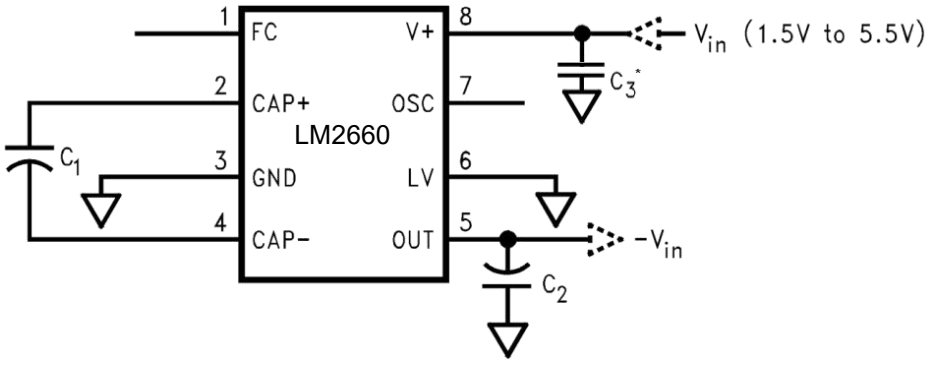
The FC (frequency control) pin selects between a nominal10kHz or 80kHz oscillator frequency.The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2660 with an external clock up to 150kHz. Through these methods, output ripple frequency and harmonics may be controlled.

Additionally, the LM2660 may be configured to divide a positive input voltage precisely in half. In this mode, input voltages as high as 11 V may be used.

Functional Block Diagram

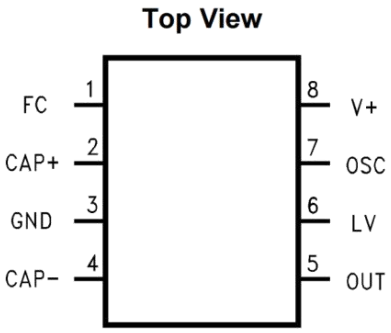


Simplified Schematic

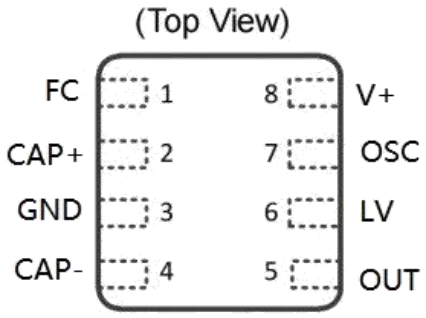


* When Iout>100ma FC=Vdd, the C_3 capacitance should be greater than 0.1uf.

Pin Configuration and Functions



DIP-8/SOP-8/MSOP-8



DFN-8 3*3

Pin Functions

PIN		TYPE	DESCRIPTION	
NUMBER	NAME		VOLTAGE INVERTER	VOLTAGE DOUBLER
1	FC	Input	Frequency control for internal oscillator: FC = open, f_{OSC} = 10 kHz (typ); FC = V+, f_{OSC} = 80 kHz (typ); FC has no effect when OSC pin is driven externally.	Same as inverter.
2	CAP+	Power	Connect this pin to the positive terminal of charge- pump capacitor.	Same as inverter.
3	GND	Ground	Power supply ground input.	Power supply positive voltage input.
4	CAP−	Power	Connect this pin to the negative terminal of charge-pump capacitor.	Same as inverter.
5	OUT	Power	Negative voltage output.	Power supply ground input.
6	LV	Input	Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5V. Above 3.5V, LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND.	LV must be tied to OUT.
7	OSC	Input	Oscillator control input. OSC is connected to an internal 15-pF apacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC.	Same as inverter except that OSC cannot be driven by an external clock.
8	V+	Power	Power supply positive voltage input.	Positive voltage output.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or GND to OUT)		7.5	V
LV	OUT − 0.3 V	GND + 3 V	V
FC, OSC	The least negative of (OUT − 0.3 V) or (V+ − 6 V) to (V+ + 0.3 V)		V
V+ and OUT continuous output current		120	mA
Output short-circuit duration to GND (2)		1	second
Power dissipation SOIC (D)(3)		735	mW
Power dissipation VSSOP (DGK)(3)		500	mW
Lead temperature (soldering, 10 seconds)		260	°C
Operating junction temperature	–40	85	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.

(3) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - TA)/R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and RθJA is the junction-to-ambient thermal resistance of the specified package.

Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000		V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V+ (supply voltage)	Inverter, LV = Open	3.5	5.5	V
	Inverter, LV = GND	1.5	5.5	
	Doubler, LV = OUT	2.5	5.5	
Junction temperature (T_J)		–40	85	°C

Thermal Information

THERMAL METRIC(1)	LM2660 SOP-8	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	170	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Electrical Characteristics

Limits in for typical (TYP) values are for T_J = 25°C, and limits in for minimum (MIN) and maximum (MAX) values apply over the full operating temperature range; V+ = 5V, FC = Open, C_1 = C_2 = 150 µF, unless otherwise specified in the Test Conditions.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_+	Supply voltage	R_L = 1k	Inverter, LV = Open	3.5		5.5	V
			Inverter, LV = GND	1.5		5.5	
			Doubler, LV = OUT	2.5		5.5	
I_Q	Supply current	No Load	FC = Open		0.12	0.5	mA
		LV = Open	FC = V+		1	3	
I_L	Output current	T_A≤ 85°C, OUT ≤ −4 V		100			mA
		T_A > 85°C, OUT ≤ −3.8 V		100			
R_{OUT}	Output resistance(2)(4)	I_L = 100 mA	T_A ≤ 85°C		8	12	Ω
			T_A > 85°C			14	
f_{OSC}	Oscillator frequency	OSC = Open	FC = Open	5	10		kHz
			FC = V+	40	80		
f_{SW}	Switching frequency(3)	OSC = Open	FC = Open	2.5	5		kHz
			FC = V+	20	40		
I_{OSC}	OSC input current	FC = Open			±2		µA
		FC = V+			±16		
P_{EFF}	Power efficiency	R_L (1k) between V^+ and OUT		96%	98%		
		R_L (500) between GND and OUT		92%	96%		
		IL = 100 mA to GND			88%		
VO_{EFF}	Voltage conversion efficiency	No Load		99%	99.96%		

(1) In the test circuit, capacitors C_1 and C_2 are 0.2-Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

(2) Specified output resistance includes internal switch resistance and capacitor ESR.

(3) The output switches operate at one half of the oscillator frequency, f_{OSC} = $2f_{SW}$

(4)When Iout>100ma FC=Vdd, the capacitance should be greater than 0.1uf.

Typical Characteristics

(Circuit of Figure 12)

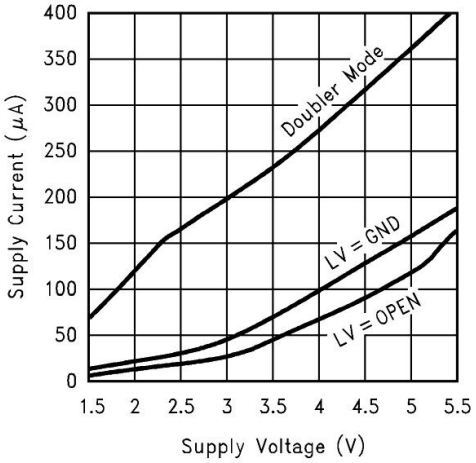


Figure 1. Supply Current vs Supply Voltage

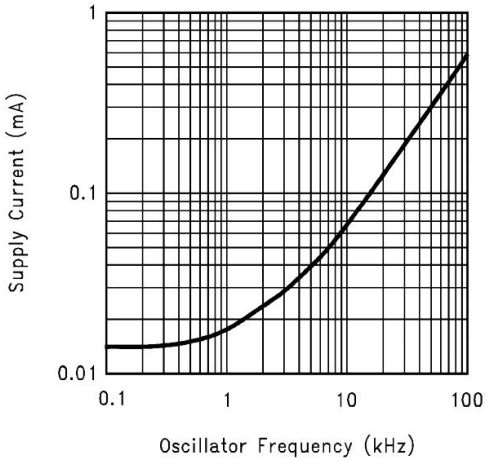


Figure 2. Supply Current vs Oscillator Frequency

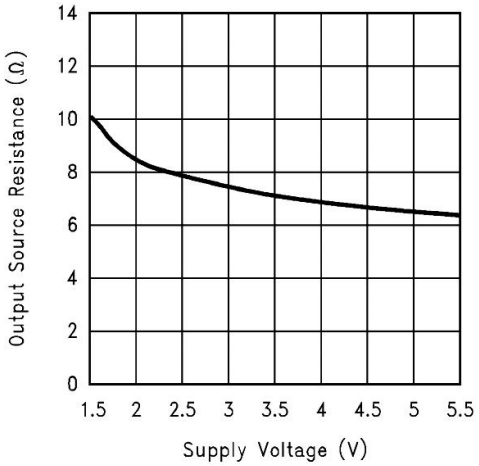


Figure 3. Output Source Resistance vs Supply Voltage

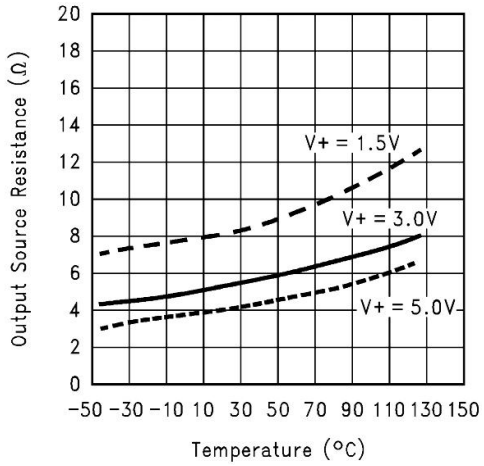


Figure 4. Output Source Resistance vs Temperature

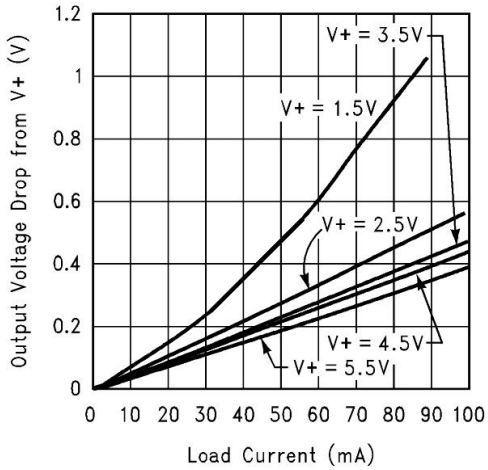


Figure 5. Output Voltage Drop vs Load Current

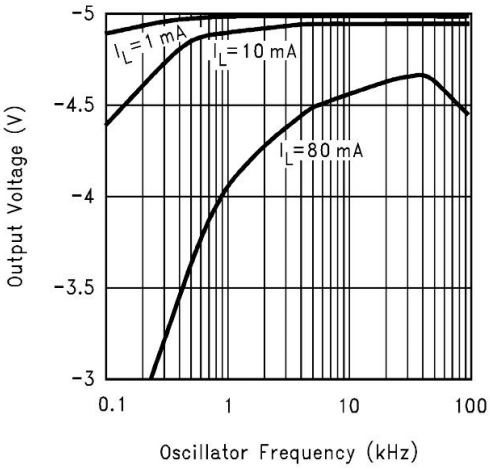
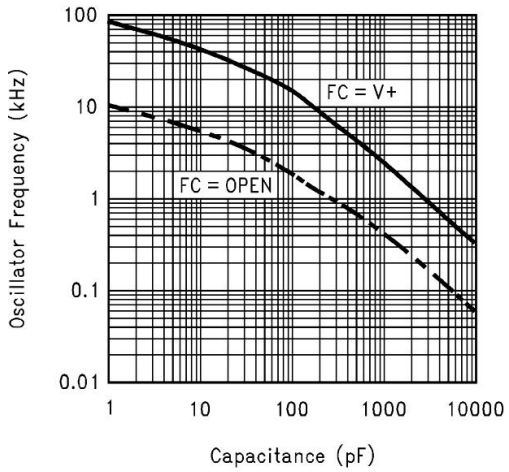


Figure 6. Output Voltage vs Oscillator Frequency



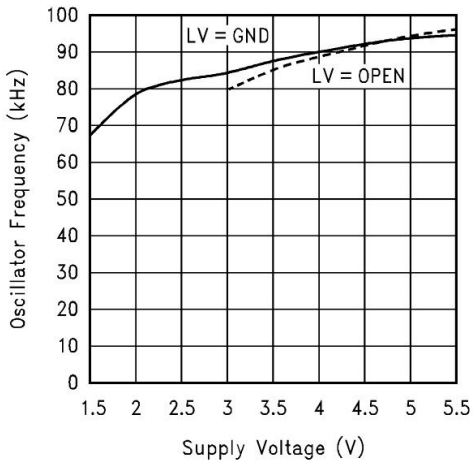


Figure 7. Oscillator Frequency vs External Capacitance Figure 8. Oscillator Frequency vs Supply Voltage(Fc = V+)

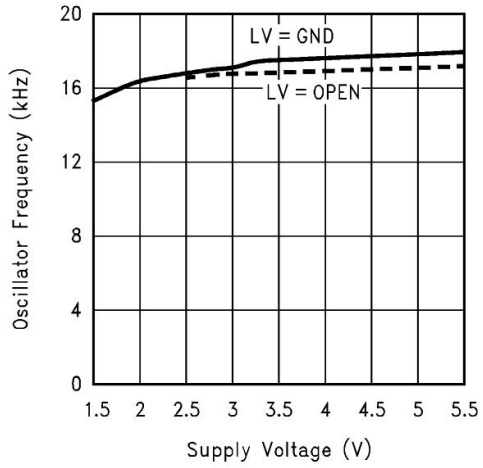


Figure 9. Oscillator Frequency vs Supply Voltage (Fc = Open)

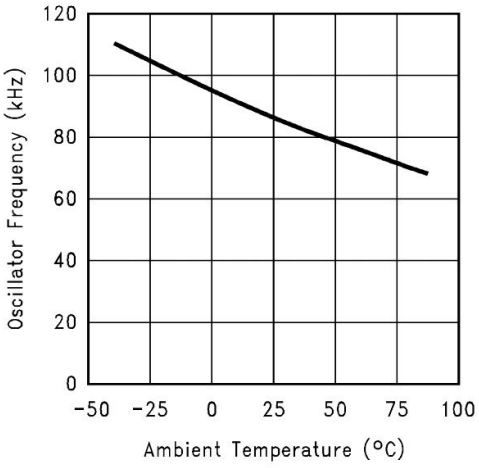


Figure 10. Oscillator Frequency vs Temperature (Fc = V+)

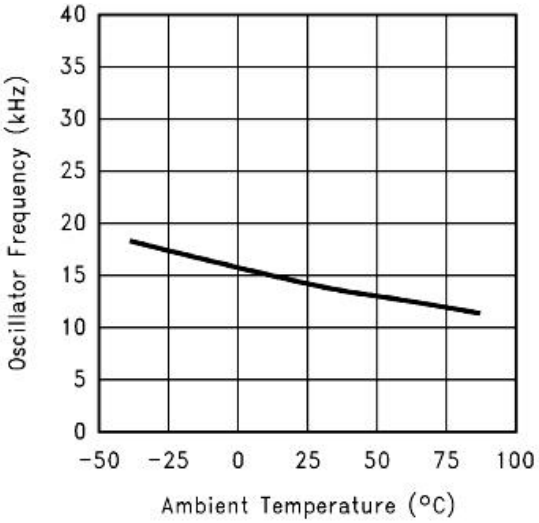
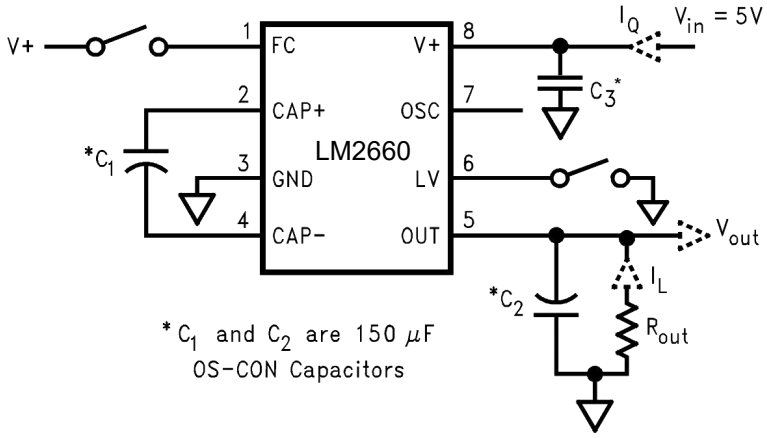


Figure 11. Oscillator Frequency vs Temperature (Fc = Open)

Parameter Measurement Information

Test Circuits



* When Iout>100ma FC=Vdd, the C_3 capacitance should be greater than 0.1uf.

Figure 12. LM2660 Test Circuit

Detailed Description

Overview

The LM2660 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 13 illustrates the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V+. During this time interval switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open and S_2 and S_4 are closed, C_1 is charging C_2 . After a number of cycles, the voltage across C_2 will be pumped to V+. Since the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(V+) assuming no load on C_2 , no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.

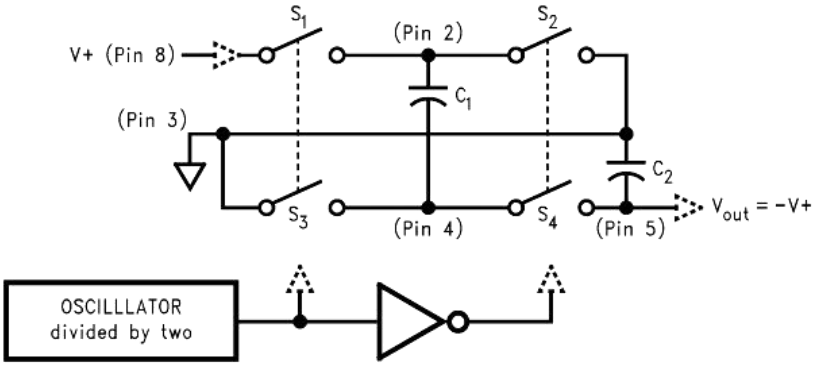


Figure 13. Voltage Inverting Principle

Feature Description

Changing Oscillator Frequency

The internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 10 kHz; when FC is connected to V+, the frequency increases to 80 kHz. A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.12 mA to 1 mA.

The oscillator frequency can be lowered by adding an external capacitor between OSC and GND. (See Typical Characteristics.) Also, in the inverter mode, an external clock that swings within 100 mV of V+ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency.

NOTE OSC cannot be driven by an external clock in the voltage-doubling mode.

Feature Description (continued)

Table 1. LM2660 Oscillator Frequency Selection

FC	OSC	OSCILLATOR
Open	Open	10 kHz
V+	Open	80 kHz
Open or V+	External Capacitor	See Typical Characteristics
N/A	External Clock	External Clock
	(inverter mode only)	Frequency

Device Functional Modes

When V+ is applied to the LM2660, the device becomes enabled and will operate in which ever configuration the device is placed (inverter, doubler, etc.).

Application Information

The LM2660 CMOS charge-pump voltage converter is a versatile unregulated switched capacitor inverter or doubler. Operating from a wide 1.5 V to 5.5 V supply voltage, the LM2660 uses two low-cost capacitors to provide 100 mA of output current without the cost, size and EMI related to inductor-based converters. With an operating current of only 120 μA and operating efficiency greater than 90% at most loads, the LM2660 provides ideal performance for battery-powered systems. LM2660 devices can be operated directly in parallel to lower output impedance, thus providing more current at a given voltage.

Typical Applications

Voltage Inverter

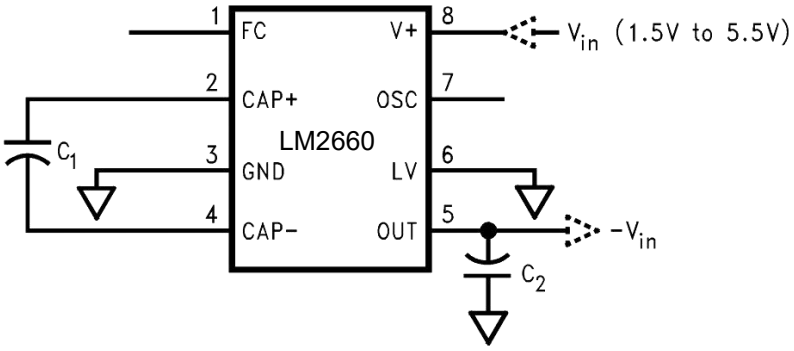


Figure 14. LM2660 Voltage Inverter

Design Requirements

The main application of LM2660 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Figure 14. The range of the input supply voltage is 1.5 V to 5.5 V. For a supply voltage less than 3.5V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5 V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the LM2660 for the LMC7660 Switched Capacitor Voltage Converter.

Detailed Design Procedure

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals −(V+). The output resistance Rout is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C1 and C2 . A good approximation is:

$$R_{out} \cong 2R_{SW} + \frac{2}{f_{osc} \times C_1} + 4\,ESR_{C1} + ESR_{C2}$$

where

- RSW is the sum of the ON resistance of the internal MOS switches shown in Figure 13. (1)

High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the $2/(f_{osc} \times C1)$ term. Once this term is trivial compared with R_{SW} and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C2 :

$$V_{ripple} = \frac{I_L}{f_{osc} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

Again, using a low ESR capacitor will result in lower ripple.

Typical Applications (continued)

Capacitor Selection

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{out} + I_Q(V+)}$$

where

- $I_Q(V+)$ is the quiescent power loss of the IC device, and
- $I_L{}^2 R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs (3)

Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. However, the ESR of C_2 directly affects the output voltage ripple. Therefore, low ESR capacitors (Table 2) are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, C_1 and C_2 are usually chosen to be the same.

The output resistance varies with the oscillator frequency and the capacitors. In Figure 15, the output resistance vs. oscillator frequency curves are drawn for three different tantalum capacitors. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 20 kHz for the 150 µF capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. For lower ESR, use ceramic capacitors.

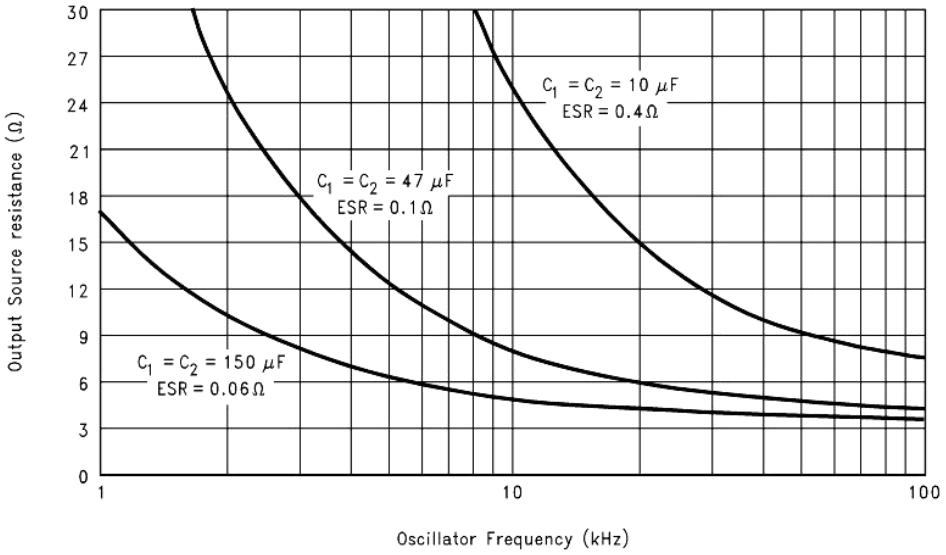


Figure 15. Output Source Resistance vs Oscillator Frequency

Table 2. Low ESR Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE
Nichicon Corp.	PL, PF series, through-hole aluminum electrolytic
AVX Corp.	TPS series, surface-mount tantalum
Sprague	593D, 594D, 595D series, surface-mount tantalum
Sanyo	OS-CON series, through-hole aluminum electrolytic

Paralleling Devices

Any number of LM2660s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C_1 , while only one output capacitor C_{out} is needed as shown in Figure 16. The composite output resistance is:

$$R_{out} = \frac{R_{out}\ of\ each\ LM2660}{Number\ of\ Devices} \quad (4)$$

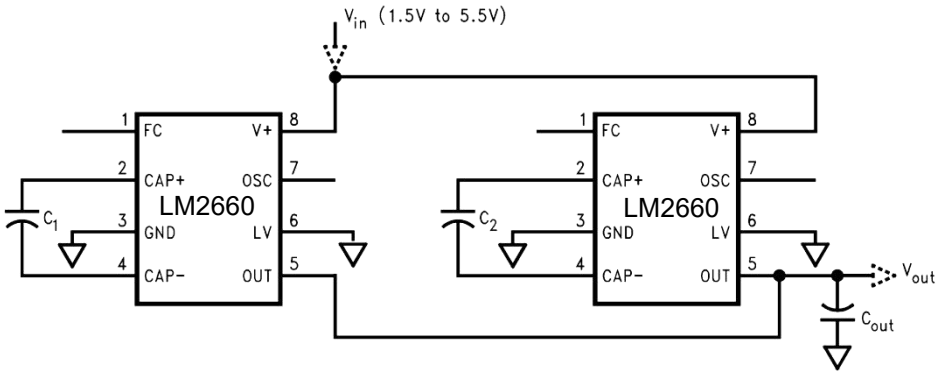


Figure 16. Lowering Output Resistance By Paralleling Devices

Cascading Devices

Cascading the LM2660s is an easy way to produce a greater negative voltage (as shown in Figure 17). If n is the integer representing the number of devices cascaded, the unloaded output voltage V_{out} is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + \frac{n}{2}R_{out\_2} + \ldots + R_{out\_n} \quad (5)$$

A three-stage cascade circuit shown in Figure 18 generates −3 V_{in}, from V_{in}.

Cascading is also possible when devices are operating in doubling mode. In Figure 19, two devices are cascaded to generate 3 V_{in}.

An example of using the circuit in Figure 18 or Figure 19 is generating +15 V or −15 V from a +5 V input.

Note that, the number of n is practically limited since the increasing of n significantly reduces the efficiency and increases the output resistance and output voltage ripple.

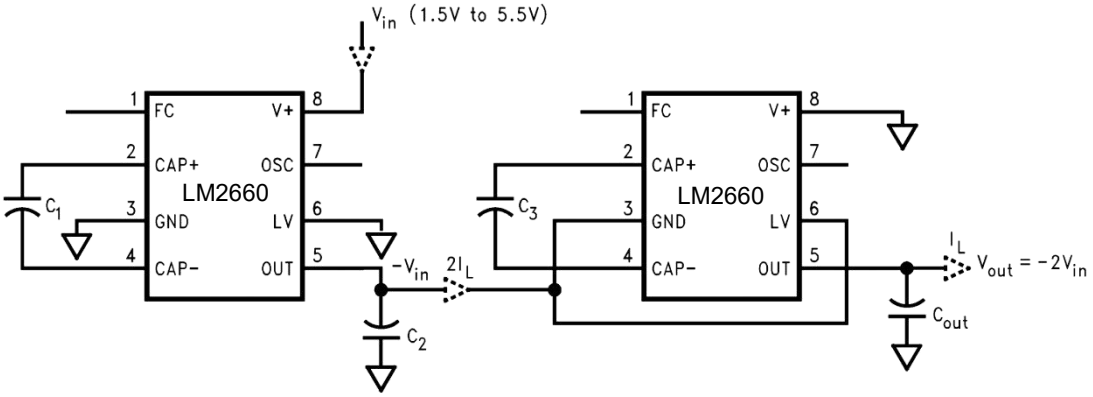


Figure 17. Increasing Output Voltage by Cascading Devices

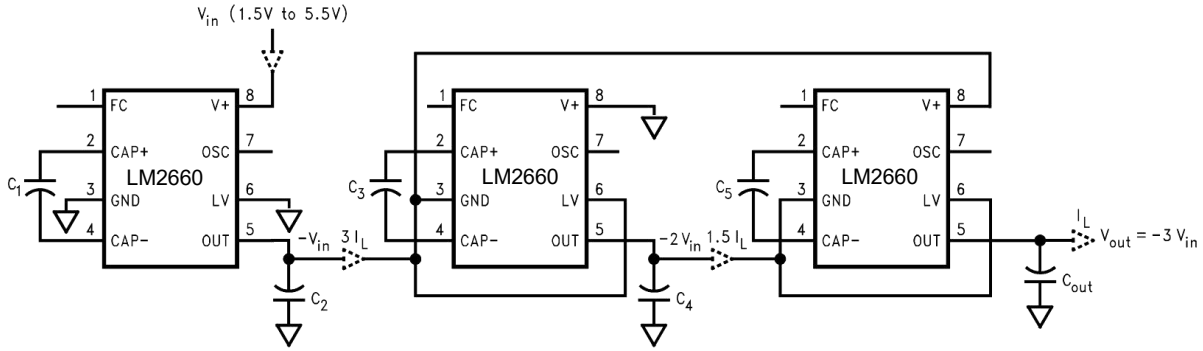


Figure 18. Generating −3V$_{IN}$ from +V$_{IN}$

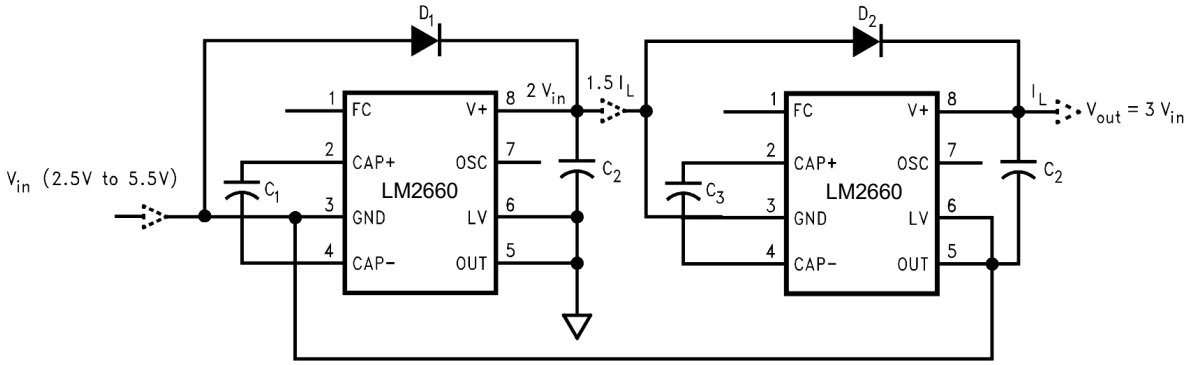


Figure 19. Generating +3V$_{IN}$ from +V$_{IN}$

Regulating VOUT

It is possible to regulate the output of the LM2660 by use of a low dropout regulator (such as LP2951). The whole converter is depicted in Figure 20. This converter can give a regulated output from −1.5 V to −5.5 V by choosing the proper resistor ratio:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

where

- V_{ref} = 1.235 V (6)

The error flag on pin 5 of the LP2951 goes low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shutdown by taking pin 3 high.

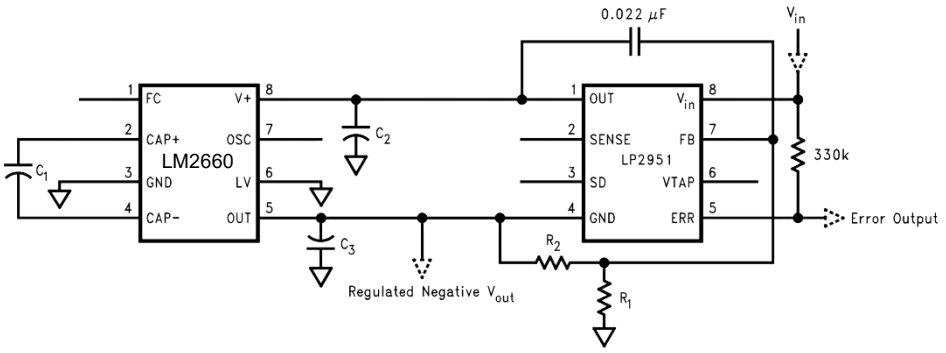


Figure 20. Combining LM2660 With LP2951 to Make a Negative Adjustable Regulator

Also, as shown in Figure 21 by operating LM2660 in voltage doubling mode and adding a linear regulator (such as LP2981) at the output, we can get +5 V output from an input as low as +3 V.

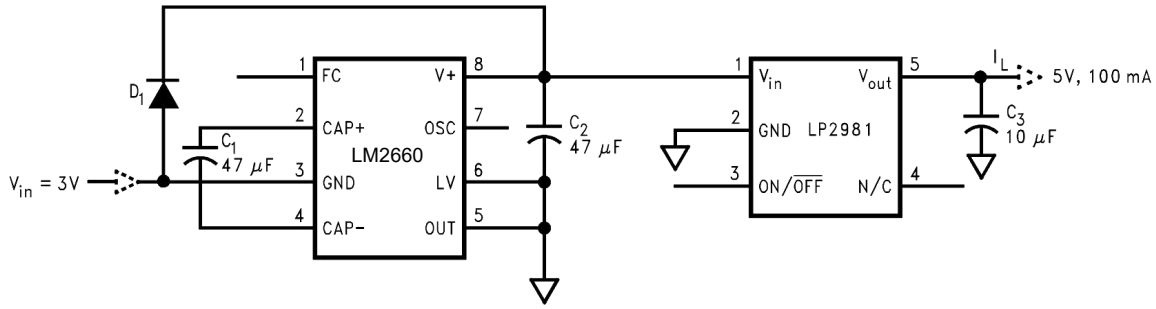


Figure 21. Generating +5 V from +3 V Input Voltage

Application Curves

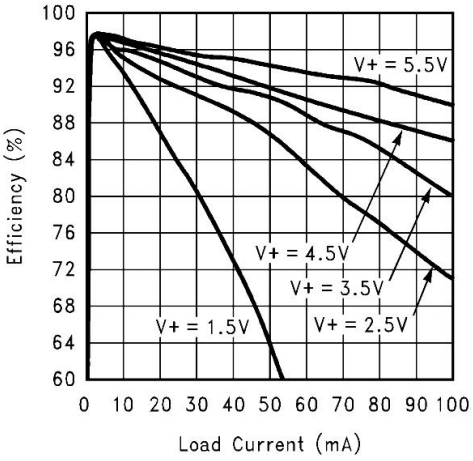


Figure 22. Efficiency vs Load Current

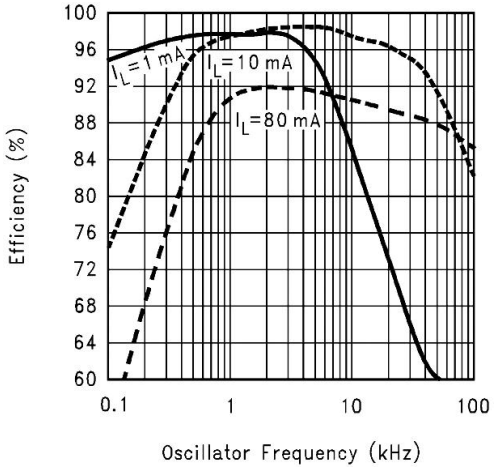


Figure 23. Efficiency vs Oscillator Frequency

Positive Voltage Doubler

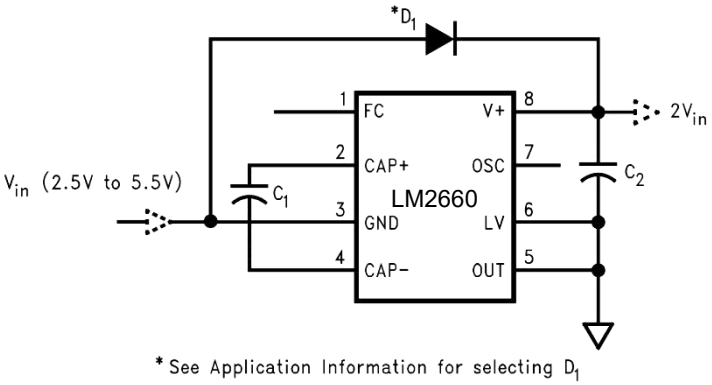


Figure 24. LM2660 Voltage Doubler

Design Requirements

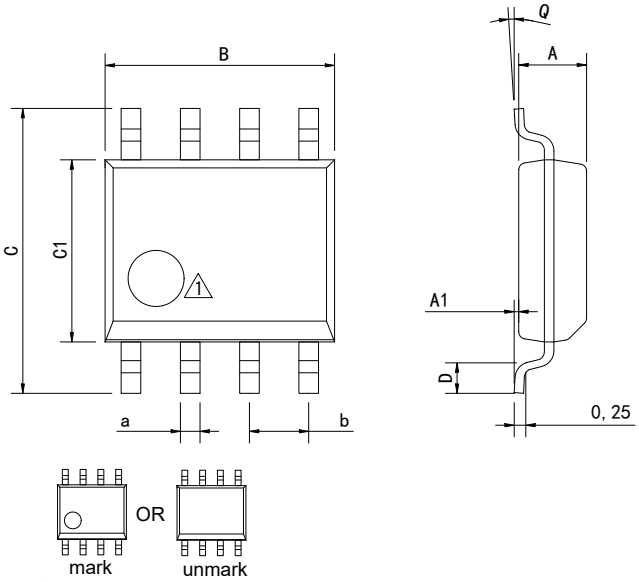
The LM2660 can operate as a positive voltage doubler (as shown in the Figure 24). The doubling function is achieved by reversing some of the connections to the device. The input voltage is applied to the GND pin with an allowable voltage from 2.5 V to 5.5 V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode D1 's forward drop.

Detailed Design Procedure

The Schottky diode D1 is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5 V to insure the operation of the oscillator. During start-up, D1 is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode D1 should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

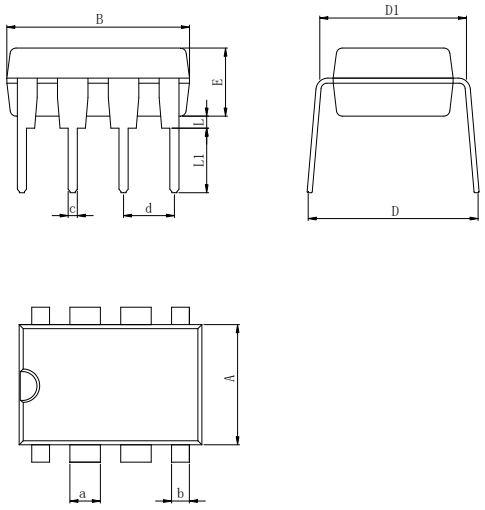
Physical Dimensions

SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

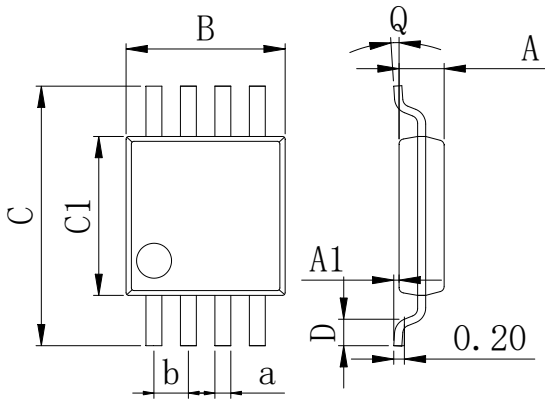
DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	**A**	**B**	**D**	**D1**	**E**	**L**	**L1**	**a**	**b**	**c**	**d**
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.75	1.20	0.50	

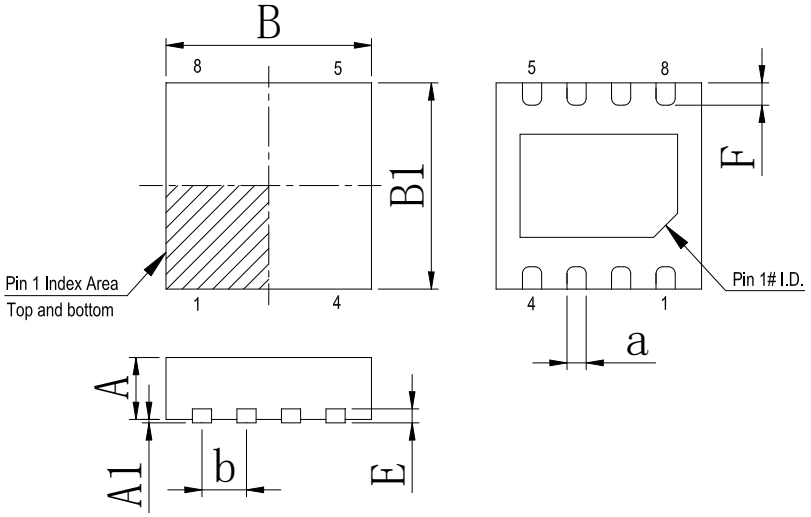
Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

DFN-8 3*3_0.65 Pin spacing



Dimensions In Millimeters(DFN-8 3*3)								
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**a**	**b**
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65 BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2016-11	New	1-18
V1.1	2025-10	Document Reformatting	1-18
V1.2	2025-12	Add DIP-8、MSOP-8 and DFN-8 package model	1

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