



QNHCHIP

QNM7421AY

Product Specification

QNM7421AY

18V P-Channel MOSFET



Description

- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge

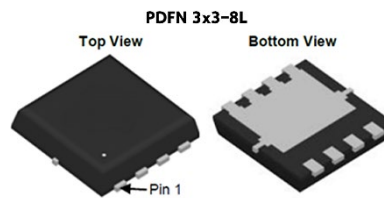
FEATURES

- $V_{DS} = -18V$, $I_D = -55A$
 $R_{DS(ON)} < 9.1m\Omega$ @ $V_{GS} = -4.5V$
 $R_{DS(ON)} < 13.0m\Omega$ @ $V_{GS} = -2.5V$

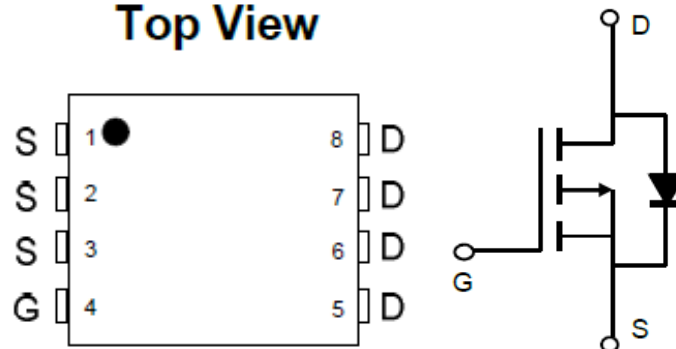
Applications

- PWM Applications
- Load Switch

Pin Description



Top View



| NO. | Symbol | Description |
|-----|--------|-------------|
| 1 | S | SOURCE |
| 2 | S | SOURCE |
| 3 | S | SOURCE |
| 4 | G | GATE |
| 5 | D | DRAIN |
| 6 | D | DRAIN |
| 7 | D | DRAIN |
| 8 | D | DRAIN |



Absolute Maximum Ratings

(@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Max. | Units |
|-----------------|-----------------------------------------------|---------------------------|---------------------------|
| V_{DSS} | Drain-Source Voltage | -18 | V |
| V_{GSS} | Gate-Source Voltage | ± 12 | V |
| I_D | Continuous Drain Current | $T_C = 25^\circ\text{C}$ | A |
| | | $T_C = 100^\circ\text{C}$ | |
| I_{DM} | Pulsed Drain Current ⁽¹⁾ | -220 | A |
| E_{AS} | Single Pulsed Avalanche Energy ⁽²⁾ | 90 | mJ |
| P_D | Power Dissipation | 66 | W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.9 | $^\circ\text{C}/\text{W}$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |



Electrical Characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---------------------------------------------------------------|----------------------------------------------------------|-------------------------------------------------------------------|------|-------|-----------|------------|
| Off Characteristic | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=-250\mu A$ | -18 | - | - | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=-18V, V_{GS}=0V,$ | - | - | -1 | μA |
| I_{GSS} | Gate to Body Leakage Current | $V_{DS}=0V, V_{GS}=\pm 12V$ | - | - | ± 100 | nA |
| On Characteristics | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=-250\mu A$ | -0.4 | -0.55 | -1.0 | V |
| $R_{DS(on)}$ | Static Drain-Source on-Resistance ⁽³⁾ | $V_{GS}=-4.5V, I_D=-15A$ | - | 6.4 | 9.1 | m Ω |
| | | $V_{GS}=-2.5V, I_D=-12A$ | - | 9.4 | 13.0 | |
| Dynamic Characteristics | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$ | - | 1935 | - | pF |
| C_{oss} | Output Capacitance | | - | 407 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | | - | 368 | - | pF |
| Q_g | Total Gate Charge | $V_{DS}=-10V, I_D=-15A,$ $V_{GS}=-4.5V$ | - | 56 | - | nC |
| Q_{gs} | Gate-Source Charge | | - | 8 | - | nC |
| Q_{gd} | Gate-Drain("Miller") Charge | | - | 16 | - | nC |
| Switching Characteristics | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}=-10V, I_D=-13A,$ $R_{GEN}=2.7\Omega,$ $V_{GS}=-10V$ | - | 11 | - | ns |
| t_r | Turn-on Rise Time | | - | 110 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | | - | 157 | - | ns |
| t_f | Turn-off Fall Time | | - | 160 | - | ns |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| I_S | Maximum Continuous Drain to Source Diode Forward Current | | - | - | -55 | A |
| I_{SM} | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | -220 | A |
| V_{SD} | Drain to Source Diode Forward Voltage | $V_{GS}=0V, I_S=-30A$ | - | - | -0.7 | V |
| t_{rr} | Reverse Recovery Time | $T_J=25^\circ\text{C}, I_S=-15A,$ $di/dt=-100A/\mu s$ | - | 23 | - | ns |
| Q_{rr} | Reverse Recovery Charge | | - | 14 | - | nC |

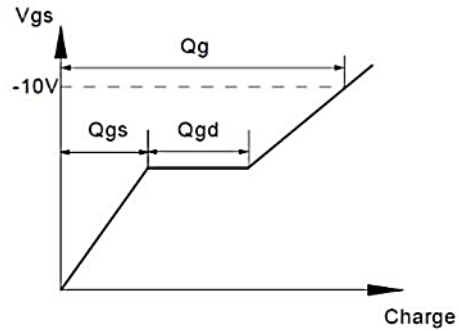
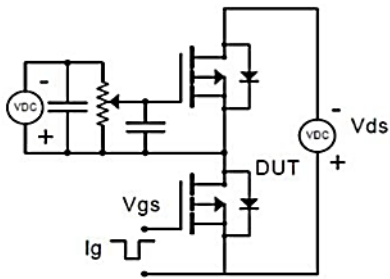
Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. E_{AS} condition: $T_J=25^\circ\text{C}, V_{DD}=-10V, V_G=-10V, R_G=25\Omega, L=0.5mH, I_{AS}=-19A$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

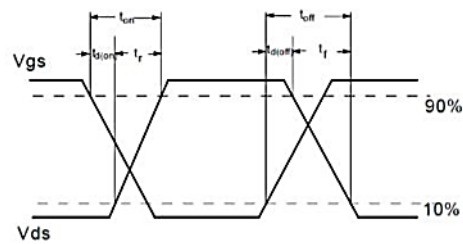
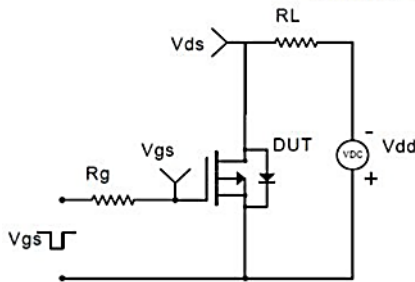


Test Circuit

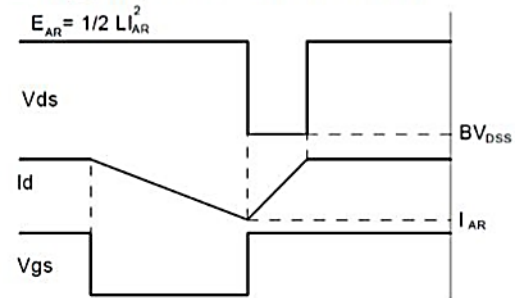
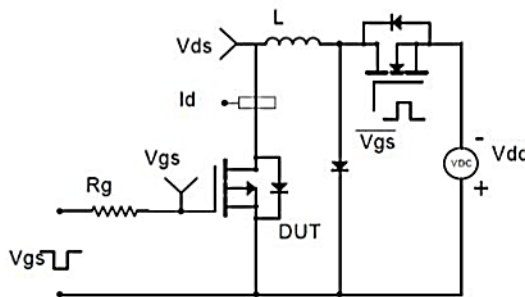
Gate Charge Test Circuit & Waveform



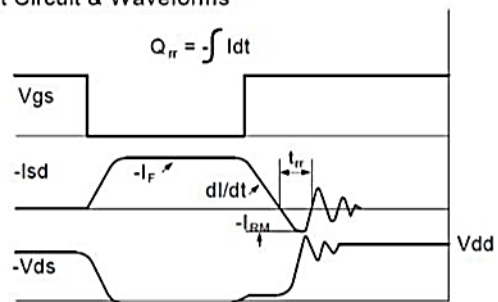
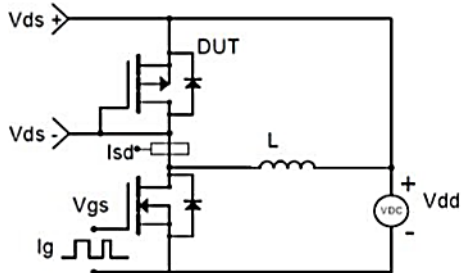
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

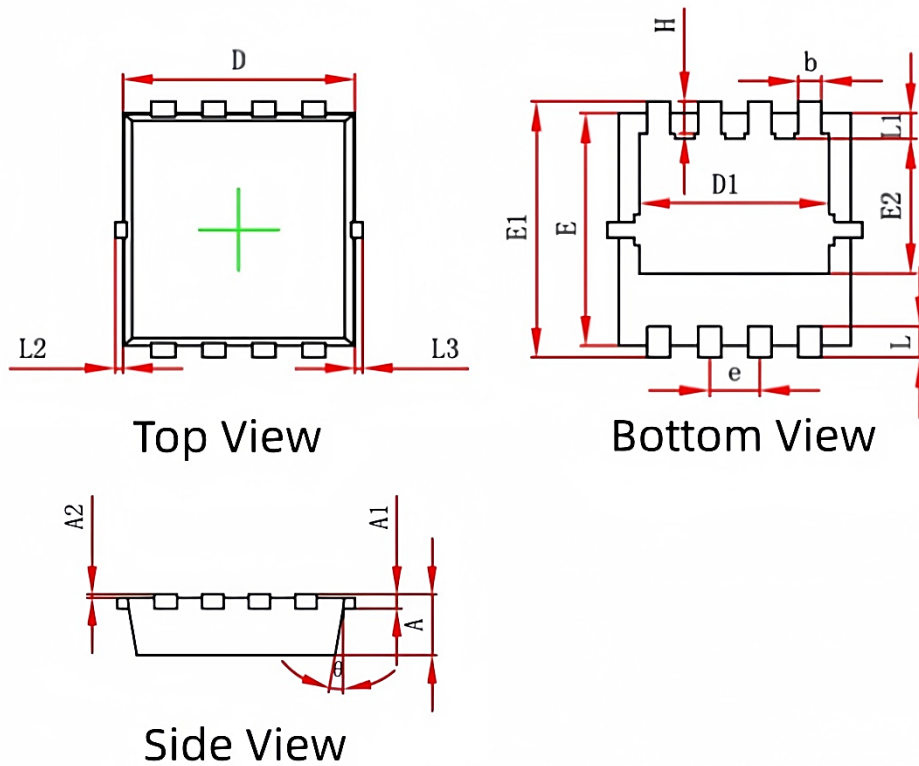


Diode Recovery Test Circuit & Waveforms

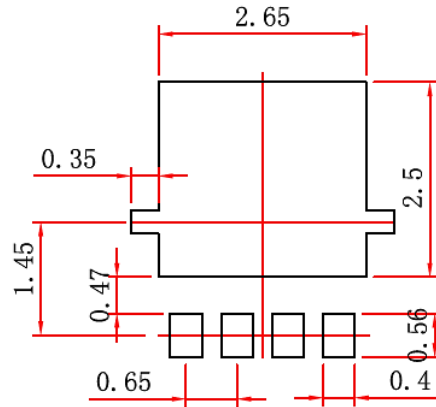




Package Mechanical Data(PDFN 3x3-8)



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|----------|---------------------------|-------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 0.650 | 0.850 | 0.026 | 0.033 |
| A1 | 0.152 REF. | | 0.006 REF. | |
| A2 | 0~0.05 | | 0~0.002 | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.300 | 2.600 | 0.091 | 0.102 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 3.150 | 3.450 | 0.124 | 0.136 |
| E2 | 1.535 | 1.935 | 0.060 | 0.076 |
| b | 0.200 | 0.400 | 0.008 | 0.016 |
| e | 0.550 | 0.750 | 0.022 | 0.030 |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| L1 | 0.180 | 0.480 | 0.007 | 0.019 |
| L2 | 0~0.100 | | 0~0.004 | |
| L3 | 0~0.100 | | 0~0.004 | |
| H | 0.315 | 0.515 | 0.012 | 0.020 |
| θ | 9° | 13° | 9° | 13° |



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

Ordering information

| Order Code | Package | $V_{DS}(V)$ | $I_D(A)$ | $R_{DS(ON)}(m\Omega)$ | |
|------------|------------|-------------|----------|-----------------------|--------|
| QNM7421AY | PDFN 3x3-8 | -18 | -55 | $V_{GS}=-4.5V$ | < 9.1 |
| | | | | $V_{GS}=-2.5V$ | < 13.0 |