

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Features

- 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation
- Max Data Rate:
  - 420 Mbps at Translation from 3.3 V to 5 V
  - 210 Mbps at Translation to 3.3 V
  - 140 Mbps at Translation to 2.5 V
  - 75 Mbps at Translation to 1.8 V
- Voltage-Level Translation between:
  - $V_{CCA}$  Range: 1.65 V to 5.5 V
  - $V_{CCB}$  Range: 1.65 V to 5.5 V
- $I_{off}$  Supports Partial Power-down Mode
- No Power Up Sequence Required for  $V_{CCA}$  and  $V_{CCB}$
- ESD Protection:
  - A Port  $\pm 8000$ -V Human-Body Model
  - B Port  $\pm 8000$ -V Human-Body Model
  - $\pm 1000$ -V Charged-Device Model

### Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

### Description

The T74L8T245 device is an 8-bit level shifter that supports only Push-Pull mode, which operates with an enable ( $\overline{OE}$ ) input. It can work within the  $V_{CCA}$  range from 1.65 V to 5.5 V and the  $V_{CCB}$  range from 1.65 V to 5.5 V.

The T74L8T245 enables asynchronous communication between data buses. Depending on the logic level of the direction control ( $DIR_n$ ) input, this device transmits data either from the A bus to the B bus or from the B bus to the A bus. The output enable ( $\overline{OE}$ ) pin can be used to disable the outputs, effectively isolating the buses.

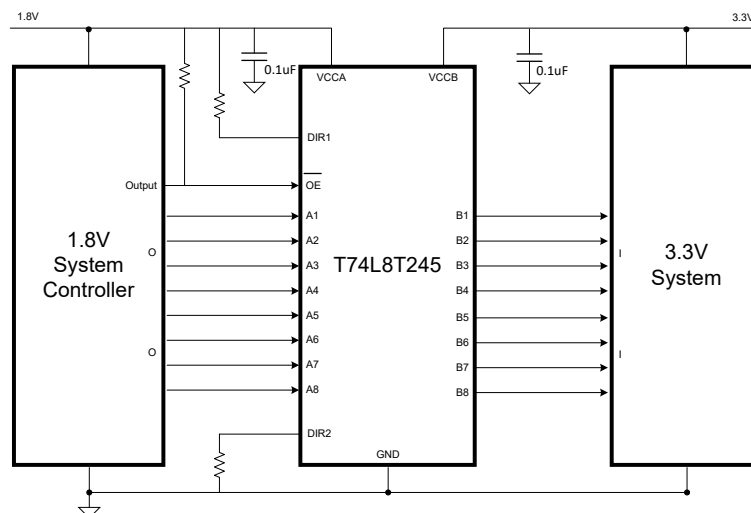
The enable control pin ( $\overline{OE}$ ) and direction control pin ( $DIR_n$ ) of the T74L8T245 are powered by  $V_{CCA}$ .

The T74L8T245 fully complies with the specifications for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging backflow current through the device when it is powered down.

For high-impedance operation during power-up/power-down conditions, the output enable ( $\overline{OE}$ ) pin must be tied to  $V_{CCA}$  via a pull-up resistor. The minimum resistor value depends on the sink current capability of the driver.

The T74L8T245 is available in the TSSOP-24 package and is characterized from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Typical Application



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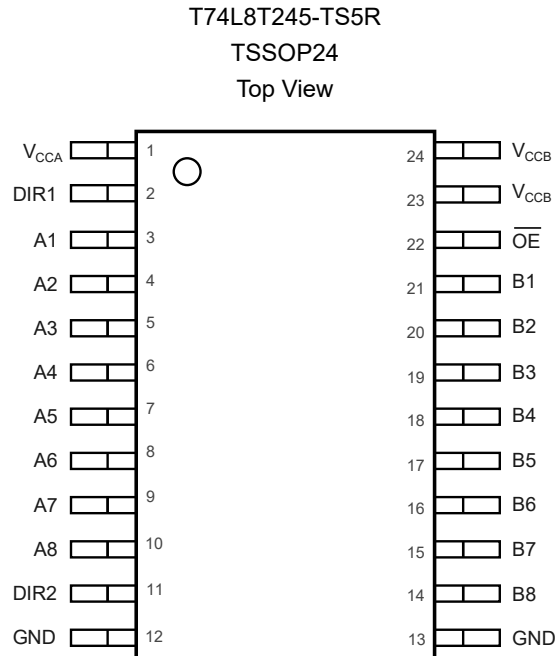
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**8-bit Dual Supply Translating Transceiver with Configurable  
Voltage Translation****Revision History**

Date	Revision	Notes
2025-05-15	Rev.P.0	Initial version
2026-01-21	Rev.A.0	Released version

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Pin Configuration and Functions



**Table 1. Pin Functions: T74L8T245-TS5R**

Pin		I/O	Description
No.	Name		
1	V <sub>CCA</sub>	Power	Side-A Supply Voltage
2	DIR1	I	Direction-control '1'. Referenced to V <sub>CCA</sub>
3	A1	I/O	Input/output A1. Referenced to V <sub>CCA</sub>
4	A2	I/O	Input/output A2. Referenced to V <sub>CCA</sub>
5	A3	I/O	Input/output A3. Referenced to V <sub>CCA</sub>
6	A4	I/O	Input/output A4. Referenced to V <sub>CCA</sub>
7	A5	I/O	Input/output A5. Referenced to V <sub>CCA</sub>
8	A6	I/O	Input/output A6. Referenced to V <sub>CCA</sub>
9	A7	I/O	Input/output A7. Referenced to V <sub>CCA</sub>
10	A8	I/O	Input/output A8. Referenced to V <sub>CCA</sub>
11	DIR2	I	Direction-control '2'. Referenced to V <sub>CCA</sub>
12	GND	Power	Supply Ground
13	GND	Power	Supply Ground
14	B8	I/O	Input/output B8. Referenced to V <sub>CCB</sub>
15	B7	I/O	Input/output B7. Referenced to V <sub>CCB</sub>
16	B6	I/O	Input/output B6. Referenced to V <sub>CCB</sub>
17	B5	I/O	Input/output B5. Referenced to V <sub>CCB</sub>

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**8-bit Dual Supply Translating Transceiver with Configurable  
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Pin		I/O	Description
No.	Name		
18	B4	I/O	Input/output B4. Referenced to $V_{CCB}$
19	B3	I/O	Input/output B3. Referenced to $V_{CCB}$
20	B2	I/O	Input/output B2. Referenced to $V_{CCB}$
21	B1	I/O	Input/output B1. Referenced to $V_{CCB}$
22	$\overline{OE}$	I	Active-low Enable Input, Reference to $V_{CCA}$
23	$V_{CCB}$	Power	Side-B Supply Voltage
24	$V_{CCB}$	Power	Side-B Supply Voltage

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Specifications

#### Absolute Maximum Ratings <sup>(1)</sup>

Parameter		Min	Max	Unit
V <sub>CCA</sub>	DC Reference Voltage Range, Side-A	-0.5	6.5	V
V <sub>CCB</sub>	DC Reference Voltage Range, Side-B	-0.5	6.5	V
I <sub>IK</sub>	Input Clamp Current, V <sub>I</sub> < 0	-50		mA
V <sub>I</sub> <sup>(2)</sup>	Input Voltage Range, Side-A	-0.5	6.5	V
	Input Voltage Range, Side-B	-0.5	6.5	V
I <sub>OK</sub>	Output Clamp Current, V <sub>IO</sub> < 0	-50		mA
V <sub>O</sub>	Output Voltage, Active Mode	-0.5	V <sub>CCO</sub> +0.5	V
	Output Voltage, Suspend or 3-state Mode	-0.5	6.5	V
I <sub>O</sub>	Continuous Output Current	-50	50	mA
I <sub>CC</sub>	Continuous Current through Each V <sub>CCA</sub> , V <sub>CCB</sub> , or GND	-100	100	mA
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The values of V<sub>CCA</sub> and V<sub>CCB</sub> are provided in the recommended operating conditions table.

(4) V<sub>CCO</sub> is the supply voltage of the output side-A or side-B port.

#### ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD, Side-A Ports	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4	kV
	Human Body Model ESD, Side-B Ports	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4	kV
CDM	Charged Device Model ESD, Side-A and Side-B Ports	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1	kV
LU	Latch Up	LU, per JESD78, All Pins	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Recommended Operating Conditions

Parameter		Conditions	Min	Typ	Max	Unit
V <sub>CCA</sub>	Supply Voltage Side-A		1.65		5.5	V
V <sub>CCB</sub>	Supply Voltage Side-B		1.65		5.5	V
V <sub>I</sub>	Input Voltage		0		5.5	V
V <sub>O</sub>	Output Voltage	Active Mode	0		V <sub>CCO</sub>	V
		Suspend or 3-state Mode	0		5.5	V
T <sub>amb</sub>	Ambient Temperature		-40		125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V <sub>CCI</sub> = 1.65 V to 1.95 V			20	ns/V
		V <sub>CCI</sub> = 2.3 V to 2.7 V			20	ns/V
		V <sub>CCI</sub> = 3 V to 3.6 V			10	ns/V
		V <sub>CCI</sub> = 4.5 V to 5.5 V			5	ns/V

(1) V<sub>CCO</sub> is the supply voltage of the output side-A or side-B port, V<sub>CCI</sub> is the supply of the input side-A or side-B port.

### Thermal Information

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
TSSOP-24	90.1	51.8	°C/W

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Electrical Characteristics

All test conditions:  $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ ,  $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ , unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-level Output Voltage	$V_I = V_{IL}$				
		$I_O = 100\ \mu\text{A}$ , $V_{CCA} = 1.65\text{ V to }4.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }4.5\text{ V}$			0.1	V
		$I_O = 4\ \text{mA}$ , $V_{CCA} = 1.65\text{ V}$ , $V_{CCB} = 1.65\text{ V}$			0.45	V
		$I_O = 8\ \text{mA}$ , $V_{CCA} = 2.3\text{ V}$ , $V_{CCB} = 2.3\text{ V}$			0.3	V
		$I_O = 24\ \text{mA}$ , $V_{CCA} = 3\text{ V}$ , $V_{CCB} = 3\text{ V}$			0.55	V
		$I_O = 32\ \text{mA}$ , $V_{CCA} = 4.5\text{ V}$ , $V_{CCB} = 4.5\text{ V}$			0.6	V
V <sub>OH</sub>	HIGH-level Output Voltage	$V_I = V_{IH}$				
		$I_O = -100\ \mu\text{A}$ , $V_{CCA} = 1.65\text{ V to }4.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }4.5\text{ V}$	$V_{CCO} - 0.1$			V
		$I_O = -4\ \text{mA}$ , $V_{CCA} = 1.65\text{ V}$ , $V_{CCB} = 1.65\text{ V}$	1.2			V
		$I_O = -8\ \text{mA}$ , $V_{CCA} = 2.3\text{ V}$ , $V_{CCB} = 2.3\text{ V}$	1.9			V
		$I_O = -24\ \text{mA}$ , $V_{CCA} = 3\text{ V}$ , $V_{CCB} = 3\text{ V}$	2.35			V
		$I_O = -32\ \text{mA}$ , $V_{CCA} = 4.5\text{ V}$ , $V_{CCB} = 4.5\text{ V}$	3.78			V
V <sub>IL</sub>	LOW-level Input Voltage (Data Input)	$V_{CCI} = 1.65\text{ V to }1.95\text{ V}$			$0.35 * V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$			0.7	V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$			0.8	V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$			$0.3 * V_{CCI}$	V
	LOW-level Input Voltage (DIRn, $\overline{\text{OE}}$ Input)	$V_{CCA} = 1.65\text{ V to }1.95\text{ V}$			$0.35 * V_{CCA}$	V
		$V_{CCA} = 2.3\text{ V to }2.7\text{ V}$			0.7	V
		$V_{CCA} = 3\text{ V to }3.6\text{ V}$			0.8	V
		$V_{CCA} = 4.5\text{ V to }5.5\text{ V}$			$0.3 * V_{CCA}$	V
V <sub>IH</sub>	HIGH-level Input Voltage (Data Input)	$V_{CCI} = 1.65\text{ V to }1.95\text{ V}$	$0.65 * V_{CCI}$			V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7			V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	2			V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$0.7 * V_{CCI}$			V
	HIGH-level Input Voltage (DIRn, $\overline{\text{OE}}$ Input)	$V_{CCA} = 1.65\text{ V to }1.95\text{ V}$	$0.72 * V_{CCA}$			V
		$V_{CCA} = 2.3\text{ V to }2.7\text{ V}$	1.7			V
		$V_{CCA} = 3\text{ V to }3.6\text{ V}$	2			V
		$V_{CCA} = 4.5\text{ V to }5.5\text{ V}$	$0.7 * V_{CCA}$			V

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

Parameter		Conditions	Min	Typ	Max	Unit
$I_i$	Input Leakage Current	DIRn, $\overline{OE}$ input, $V_I = 0\text{ V or }5.5\text{ V}$ , $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	-10		10	$\mu\text{A}$
$I_{OZ}$	OFF State Output Current	A or B port, $V_O = 0\text{ V or }V_{CCO}$	-10		10	$\mu\text{A}$
		A port, $V_O = 0\text{ V or }V_{CCO}$ , $V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 0\text{ V}$	-10		10	$\mu\text{A}$
		B port, $V_O = 0\text{ V or }V_{CCO}$ , $V_{CCA} = 0\text{ V}$ , $V_{CCB} = 5.5\text{ V}$	-10		10	$\mu\text{A}$
$I_{OFF}$	Power-off Leakage Current	A port, $V_I$ or $V_O = 0\text{ V to }5.5\text{ V}$ , $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	-10		10	$\mu\text{A}$
		B port, $V_I$ or $V_O = 0\text{ V to }5.5\text{ V}$ , $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	-10		10	$\mu\text{A}$
$I_{CCA}$	Supply Current	A port, $V_I = 0\text{ V or }V_{CCI}$ , $I_O = 0\text{ A}$ , $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$			20	$\mu\text{A}$
		A port, $V_I = 0\text{ V or }V_{CCI}$ , $I_O = 0\text{ A}$ , $V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 0\text{ V}$			20	$\mu\text{A}$
		A port, $V_I = 0\text{ V or }V_{CCI}$ , $I_O = 0\text{ A}$ , $V_{CCA} = 0\text{ V}$ , $V_{CCB} = 5.5\text{ V}$	-4			$\mu\text{A}$
$I_{CCB}$	Supply Current	B port, $V_I = 0\text{ V or }V_{CCI}$ , $I_O = 0\text{ A}$ , $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$			20	$\mu\text{A}$
		B port, $V_I = 0\text{ V or }V_{CCI}$ , $I_O = 0\text{ A}$ , $V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 0\text{ V}$	-4			$\mu\text{A}$
		B port, $V_I = 0\text{ V or }V_{CCI}$ , $I_O = 0\text{ A}$ , $V_{CCA} = 0\text{ V}$ , $V_{CCB} = 5.5\text{ V}$			20	$\mu\text{A}$
$I_{CCA} + I_{CCB}$	Combined Supply Current	A plus B port, $I_O = 0\text{ A}$ , $V_I = 0\text{ V or }V_{CCI}$ , $V_{CCA} = 1.65\text{ V to }5.5\text{ V}$ , $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$			30	$\mu\text{A}$
$\Delta I_{CC}$	Additional Supply Current	DIRn, $\overline{OE}$ input, input at $V_{CCA} - 0.6\text{ V}$ , $A = V_{CCA}$ or GND, $B = \text{open}$ , $V_{CCA} = 3\text{ V to }5.5\text{ V}$ , $V_{CCB} = 3\text{ V to }5.5\text{ V}$			75	$\mu\text{A}$
		A port, $A = V_{CCA} - 0.6$ , $B = \text{open}$ , $V_{CCA} = 3\text{ V to }5.5\text{ V}$ , $V_{CCB} = 3\text{ V to }5.5\text{ V}$			75	$\mu\text{A}$
		B port, $A = \text{open}$ , $B = V_{CCA} - 0.6$ , $V_{CCA} = 3\text{ V to }5.5\text{ V}$ , $V_{CCB} = 3\text{ V to }5.5\text{ V}$			75	$\mu\text{A}$
$C_{I(1)}$	Input Capacitance	DIRn, $\overline{OE}$ input, $V_I = 0\text{ V or }5.5\text{ V}$ , $V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 5.5\text{ V}$		6		pF
$C_{IO(1)}$	Input/output Capacitance	A or B port, $V_O = 5.5\text{ V or }0\text{ V}$ , $V_{CCA} = 5.5\text{ V}$ , $V_{CCB} = 5.5\text{ V}$		10		pF

(1) The data based on bench tests and design simulation, NOT test in production.

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### AC Timing Requirements — $V_{CCA} = 1.8\text{ V}$

All test conditions:  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ , the data is based on bench test and design simulation, NOT test in production. unless otherwise noted.

$t_{en}$  includes  $t_{PZL}$  and  $t_{PHL}$ ,  $t_{dis}$  includes  $t_{PLZ}$  and  $t_{PHZ}$ .

Parameter		Condition	$V_{CCB}$	Min	Typ	Max	Unit
$t_{PLH}, t_{PHL}$	Propagation Delay	A-to-B push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		25.9	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		13.2	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		11.4	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		11.1	ns
		B-to-A push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		28.8	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		27.6	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		27.4	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		27.4	ns
$t_{en}$	Enable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		28	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		27.8	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		27.7	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		27.7	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		40	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		20	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		16.6	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		14.8	ns
$t_{dis}$	Disable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		33.6	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		33.4	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		33.3	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		33.2	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		36.2	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		17.1	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		16	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		14.3	ns
$C_{PD}^{(1)}$	Power Dissipation Capacitance	A port, A-to-B	1.8 V		1		pF
		A port, B-to-A			17		pF
		B port, A-to-B			17		pF
		B port, B-to-A			1		pF

(1) Tested at  $V_{CCA} = 1.8\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### AC Timing Requirements — $V_{CCA} = 2.5\text{ V}$

All test conditions:  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ , the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

$t_{en}$  includes  $t_{PZL}$  and  $t_{PHL}$ ,  $t_{dis}$  includes  $t_{PLZ}$  and  $t_{PHZ}$ .

Parameter		Condition	$V_{CCB}$	Min	Typ	Max	Unit
$t_{PLH}, t_{PHL}$	Propagation Delay	A-to-B push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		25.4	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		13	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		10.2	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		8.8	ns
		B-to-A push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		13.3	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		13.1	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		12.9	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		12.8	ns
$t_{en}$	Enable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		17.2	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		17.2	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		17.2	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		17.2	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		32.2	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		18.1	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		14.1	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		11.2	ns
$t_{dis}$	Disable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		13	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		13	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		13	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		13	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		33.6	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		15	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		14.3	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10.9	ns
$C_{PD}^{(1)}$	Power Dissipation Capacitance	A port, A-to-B	2.5 V		1		pF
		A port, B-to-A			18		pF
		B port, A-to-B			18		pF
		B port, B-to-A			1		pF

(1) Tested at  $V_{CCA} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### AC Timing Requirements — $V_{CCA} = 3.3\text{ V}$

All test conditions:  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ , the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

$t_{en}$  includes  $t_{PZL}$  and  $t_{PHL}$ ,  $t_{dis}$  includes  $t_{PLZ}$  and  $t_{PHZ}$ .

Parameter		Condition	$V_{CCB}$	Min	Typ	Max	Unit
$t_{PLH}, t_{PHL}$	Propagation Delay	A-to-B push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		25.2	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		12.8	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		10.3	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10.4	ns
		B-to-A push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		11.2	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		10.2	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		10.1	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10	ns
$t_{en}$	Enable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		14.1	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		13.6	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		13.2	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		13.2	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		31.7	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		18.4	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		12.9	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10.9	ns
$t_{dis}$	Disable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		12.2	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		12.2	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		12.2	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		12.2	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		33	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		14.3	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		12.6	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10.3	ns
$C_{PD}^{(1)}$	power dissipation capacitance	A port, A-to-B	3.3 V		1		pF
		A port, B-to-A			19		pF
		B port, A-to-B			19		pF
		B port, B-to-A			1		pF

(1) Tested at  $V_{CCA} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### AC Timing Requirements — $V_{CCA} = 5\text{ V}$

All test conditions:  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ , the data is based on bench test and design simulation, NOT test in production, unless otherwise noted.

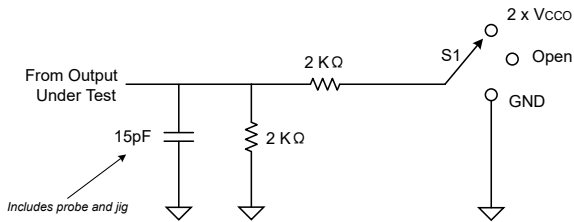
$t_{en}$  includes  $t_{PZL}$  and  $t_{PHL}$ ,  $t_{dis}$  includes  $t_{PLZ}$  and  $t_{PHZ}$ .

Parameter		Condition	$V_{CCB}$	Min	Typ	Max	Unit
$t_{PLH}, t_{PHL}$	Propagation Delay	A-to-B push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		25.4	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		12.8	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		10	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		8.2	ns
		B-to-A push-pull driving	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		11	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		8.8	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		8.5	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		8.3	ns
$t_{en}$	Enable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		10.9	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		10.9	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		10.9	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10.9	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		31.6	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		18.4	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		13.	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		10.7	ns
$t_{dis}$	Disable Time	$\overline{OE}$ -to-A	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		9.4	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		9.4	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		9.4	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		9.4	ns
		$\overline{OE}$ -to-B	$1.8\text{ V} \pm 0.15\text{ V}$	1.0		32.7	ns
			$2.5\text{ V} \pm 0.2\text{ V}$	1.0		13.7	ns
			$3.3\text{ V} \pm 0.3\text{ V}$	1.0		12	ns
			$5\text{ V} \pm 0.5\text{ V}$	1.0		9.7	ns
$C_{PD}^{(1)}$	power dissipation capacitance	A port, A-to-B	5 V		1		pF
		A port, B-to-A			22		pF
		B port, A-to-B			22		pF
		B port, B-to-A			1		pF

(1) Tested at  $V_{CCA} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

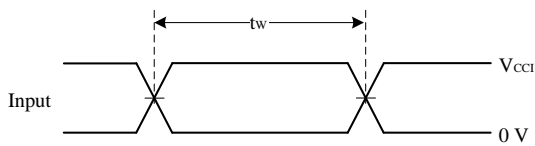
# 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

## Parameter Measurement Waveforms

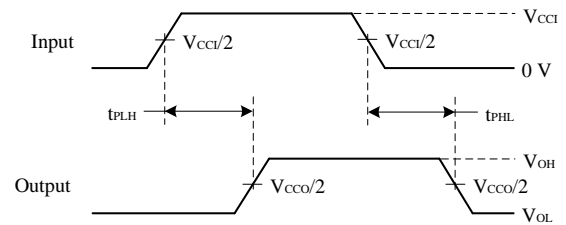


**Figure 1. Timing Measurement Load Circuit**

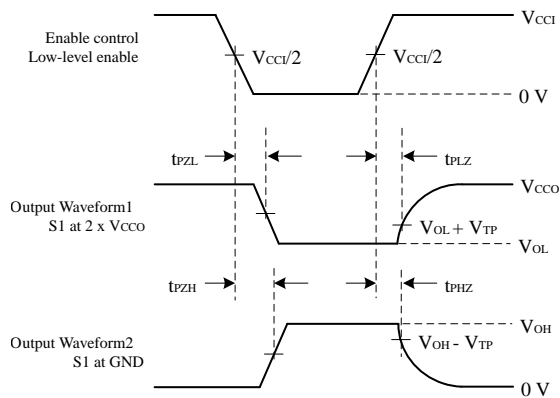
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC0}$
$t_{PHZ}/t_{PZH}$	GND



**Figure 2. Pulse Duration**



**Figure 3. Propagation Delay Times**



**Figure 4. Enable and Disable Times**

$V_{CC0}$	$V_{TP}$
$1.8 \text{ V} \pm 0.15 \text{ V}$	$0.15 \text{ V}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	$0.15 \text{ V}$
$3.3 \text{ V} \pm 0.3 \text{ V}$	$0.3 \text{ V}$
$5 \text{ V} \pm 0.5 \text{ V}$	$0.3 \text{ V}$

**Note:**

$t_{plz}$  and  $t_{phz}$  are the same as  $t_{dis}$ .

$t_{pzi}$  and  $t_{pzh}$  are the same as  $t_{en}$ .

$V_{CC1}$  is  $V_{CC}$  associated with the input port.

$V_{CC0}$  is  $V_{CC}$  associated with the output port.

$t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Detailed Description

#### Overview

The T74L8T245 device is an 8-bit level shifter, and only supports Push-Pull mode, which functions with an enable ( $\overline{OE}$ ) input and can work within the  $V_{CCA}$  range from 1.65 V to 5.5 V and the  $V_{CCB}$  range from 1.65 V to 5.5 V.  $V_{CCA}$  powers the A-port and control pins (DIRn and  $\overline{OE}$ ), while  $V_{CCB}$  supplies the B-port. The A-port supports I/O voltage levels from 1.65 V to 5.5 V, and the B-port also accommodates I/O voltages ranging from 1.65 V to 5.5 V. When  $\overline{OE}$  is set high, both A and B ports enter a high-impedance state.

#### Functional Block Diagram

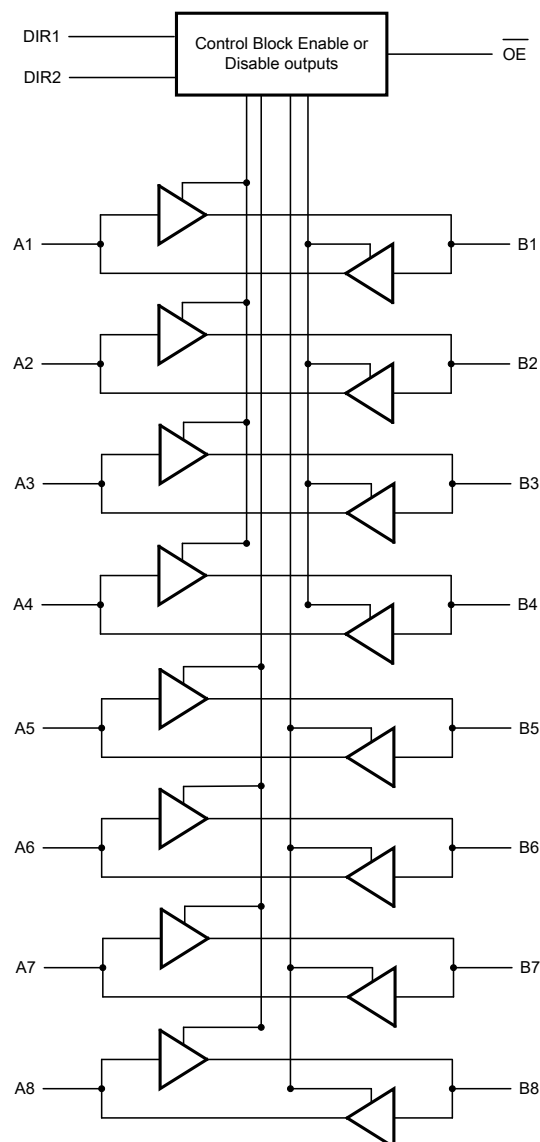


Figure 5. Functional Block Diagram

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Feature Description

#### **I<sub>off</sub> Feature**

The I<sub>off</sub> feature ensures safe operation when the chip is powered down (VCC = 0 V). It automatically disables all outputs in a high-impedance state, preventing any damaging backflow current from flowing through the unpowered device. This allows the bus to remain active while protecting both the chip and connected components.

#### **Enable ( $\overline{OE}$ ) and Direction-control (DIRn)**

The Output Enable ( $\overline{OE}$ ) is a critical chip function that manages output states. When  $\overline{OE}$  is high, all output ports enter a high-impedance state, when  $\overline{OE}$  is low, the chip operates normally according to the DIRn pin's configuration.

The T74L8T245 features a directional control function, where the state of the control pin (DIRn) determines the data transmission path between Port A and Port B. To ensure reliable operation during DIR state transitions, strict timing requirements must be followed. It is generally recommended to first disable the outputs using the  $\overline{OE}$  pin, allow the DIRn signal to stabilize, and then re-enable the outputs. This sequence prevents bus contention and signal conflicts.

**Table 2. Device Function Table**

V <sub>CCA</sub> , V <sub>CCB</sub>	Input $\overline{OE}$ <sup>(1)</sup>	Input DIR1	Input DIR2	Translator Function 1 to 4	Translator Function 5 to 8
1.65 V to 5.5 V	L	L	L	B => A	
1.65 V to 5.5 V	L	H	L	A => B	
1.65 V to 5.5 V	L	L	H	B => A	A => B
1.65 V to 5.5 V	L	H	H	A => B	B => A
1.65 V to 5.5 V	H	X	X	Hi-Z	
0 V	X	X	X	Hi-Z	

(1) Keep OE following V<sub>CCA</sub> during power-up to avoid glitches.

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Application and Implementation

**Note**

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

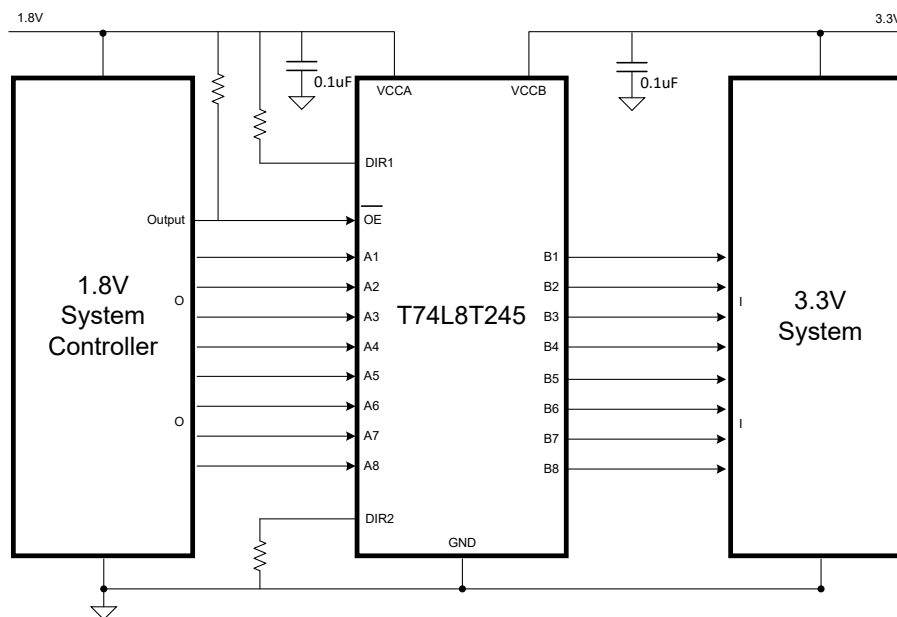
### Application Information

The T74L8T245 can be used for level-translation applications to interface devices or systems operating at different supply voltages. This device is an ideal solution for bidirectional data transmission scenarios. It is recommended to connect all unused I/O pins to ground, and no I/O pins should be left floating during direction switching. When the supply voltage exceeds 3.3 V, the device can support a maximum data rate of up to 210 Mbps.

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer Handsets
- Industrial Automation

### Typical Application

A typical application is shown in [Figure 6](#). The T74L8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The T74L8T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os.



**Figure 6. Typical Application Circuit**

# 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

## Layout

### Layout Example

Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. Below are progressively better techniques for rounding corners. Only the last example (BEST) maintains a constant trace width and minimizes reflections.

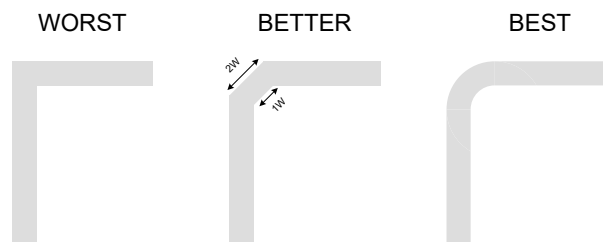


Figure 7. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

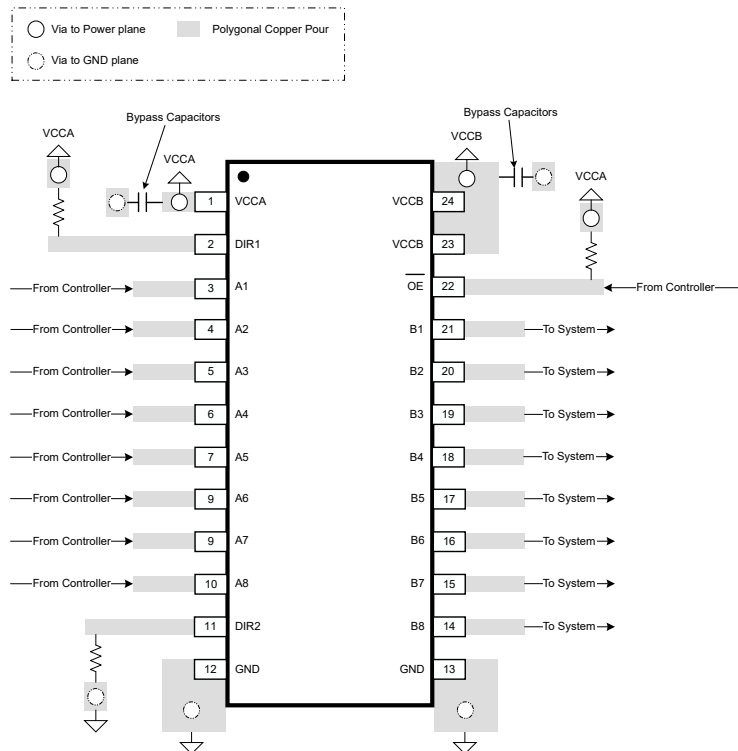
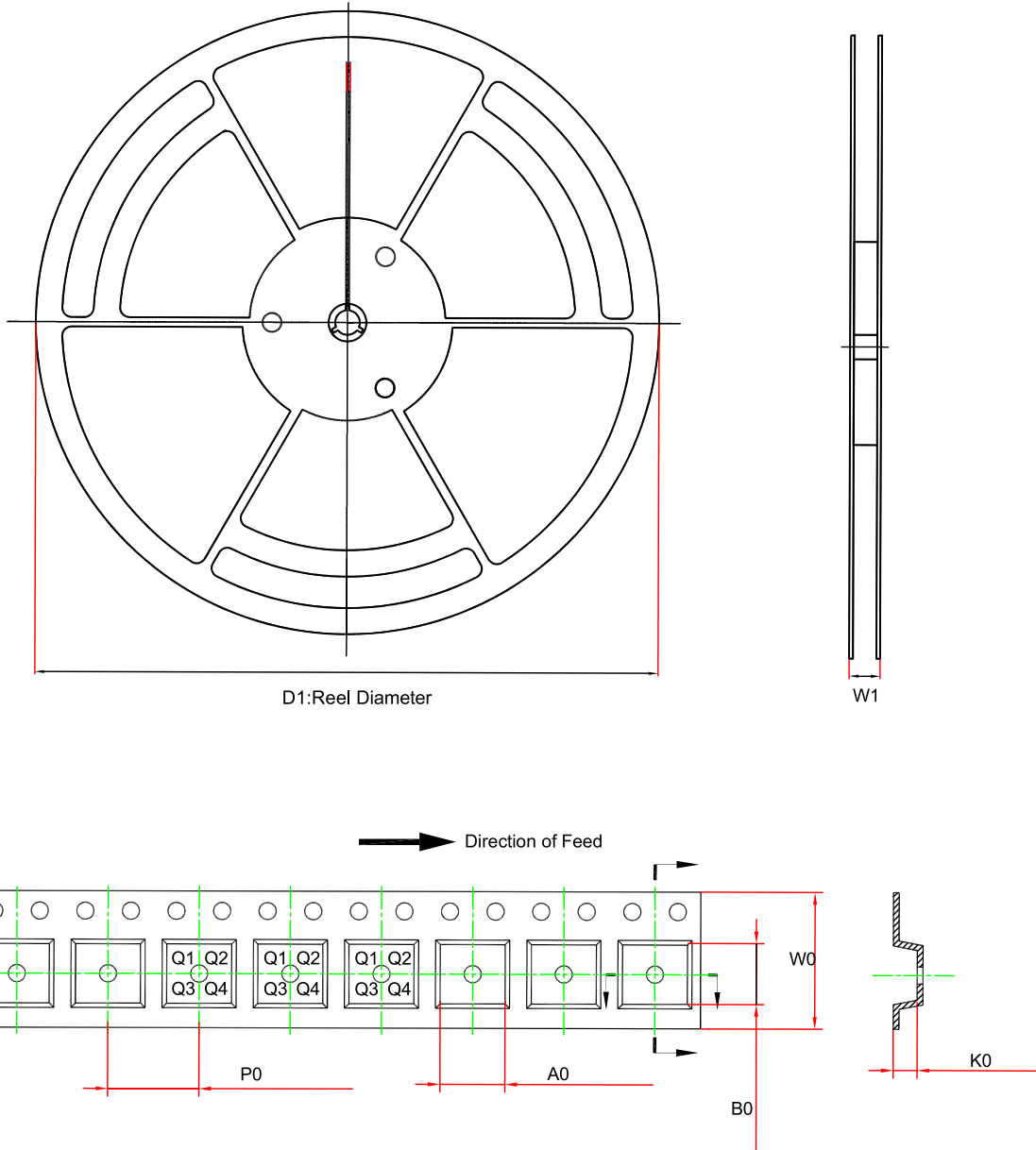


Figure 8. Layout Example

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Tape and Reel Information

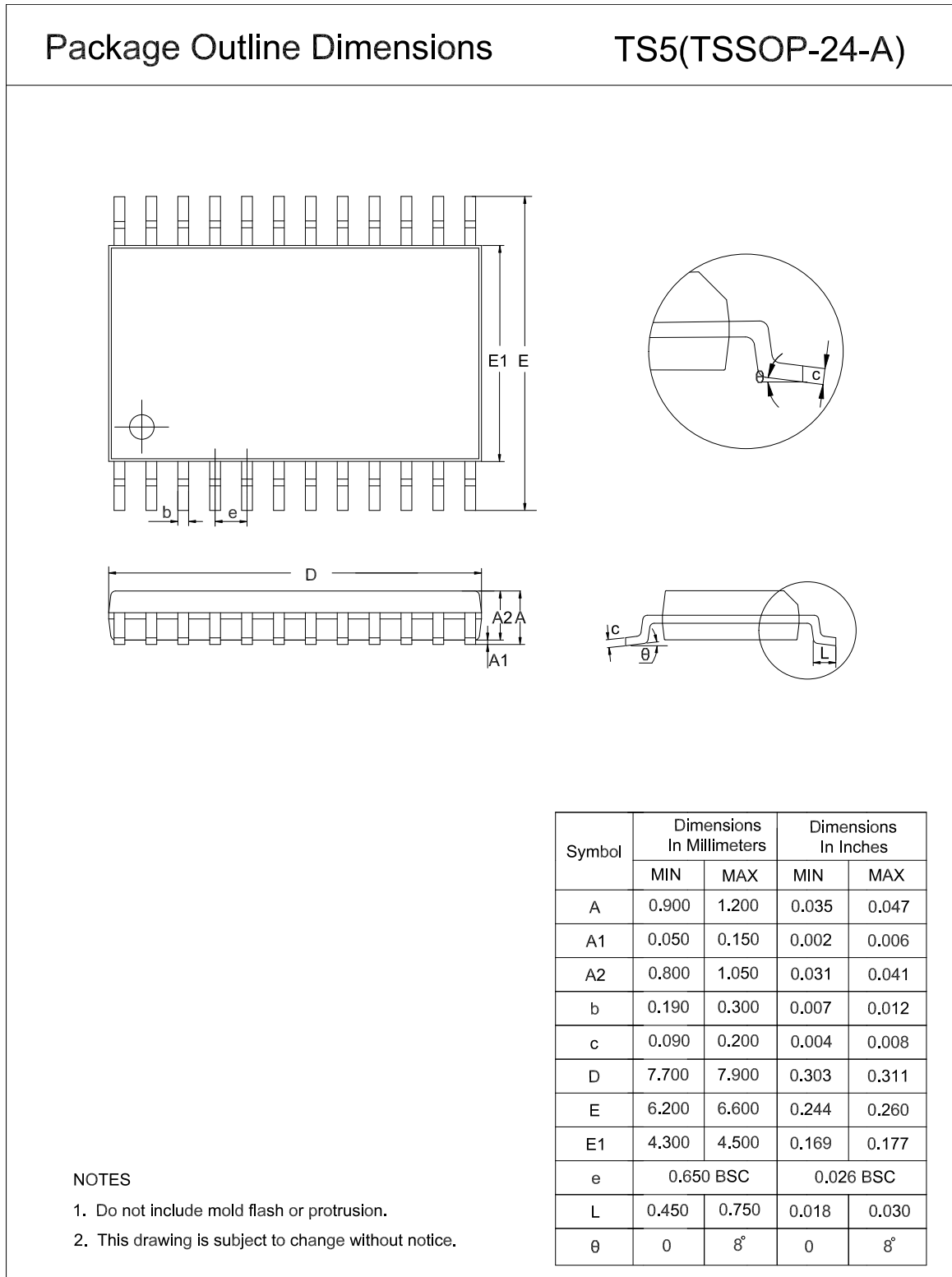


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
T74L8T245-TS5R	TSSOP-24	330	6.95	1.6	16	20.4	8.3	8.0	Q1

## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

### Package Outline Dimensions

#### TSSOP24



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**8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation****Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
T74L8T245-TS5R	-40 to 125°C	TSSOP-24	L8T245	MSL3	Tape and Reel,4000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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## 8-bit Dual Supply Translating Transceiver with Configurable Voltage Translation

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