



QNHCHIP

QNM15PD02

Product Specification

QNM15PD02

20V Dual P-Channel MOSFET



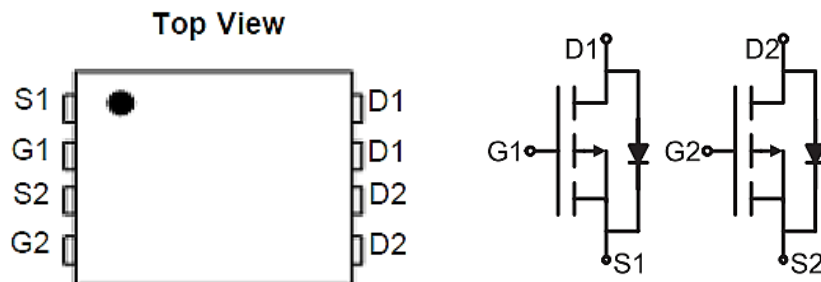
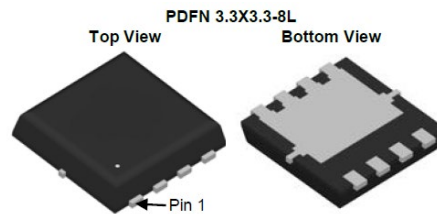
FEATURES

- -20V, -12A
 $R_{DS(ON)} = 14m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} = 18m\Omega @ V_{GS} = -2.5V$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate charge
- Lead free product is acquired

Applications

- Load Switch
- PWM Application
- Power management

Pin Description



NO.	Symbol	Description
1	S1	SOURCE
2	G1	GATE
3	S2	SOURCE
4	G2	GATE
5	D1	DRAIN
6	D1	DRAIN
7	D2	DRAIN
8	D2	DRAIN



Absolute Maximum Ratings

(@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current	-12	A
I_{DM}	Pulsed Drain Current ⁽¹⁾	-50	A
P_D	Power Dissipation	15	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽²⁾	4.5	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$



Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250uA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-12V, V _{GS} =0V			-1	uA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V			±100	nA
On Characteristics⁽³⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.4	-0.65	-1.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-6A		14	23	m Ω
		V _{GS} =-2.5V, I _D =-5A		18	28	
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-6A		20		S
Dynamic Characteristics⁽⁴⁾						
Input Capacitance	C _{iss}	V _{DS} =-6V, V _{GS} =0V, F=1.0MHz		1652		PF
Output Capacitance	C _{oss}			135		PF
Reverse Transfer Capacitance	C _{rss}			113		PF
Switching Characteristics⁽⁴⁾						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-6V, I _D =-1A,		20		nS
Turn-on Rise Time	t _r			35		nS
Turn-Off Delay Time	t _{d(off)}	R _L =6 Ω,		90		nS
Turn-Off Fall Time	t _f	V _{GEN} =-4.5V, R _g =6 Ω		70		nS
Total Gate Charge	Q _g	V _{DS} =-6V, I _D =-6A, V _{GS} =-4.5V		19.5		nC
Gate-Source Charge	Q _{gs}			4.1		nC
Gate-Drain Charge	Q _{gd}			5.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ⁽³⁾	V _{SD}	V _{GS} =0V, I _S =-1.0A			-1.2	V
Diode Forward Current ⁽²⁾	I _S				-12	A

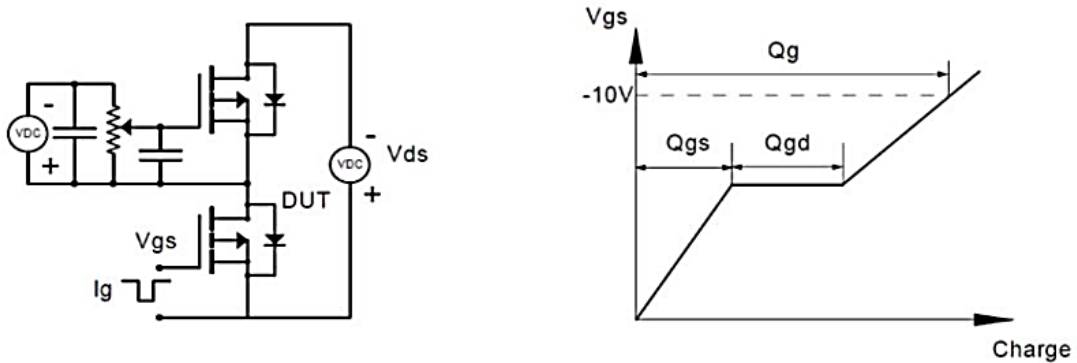
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

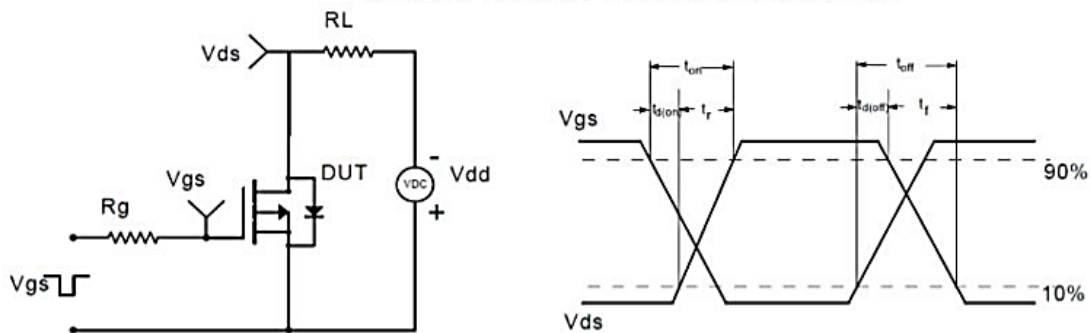


Test Circuit

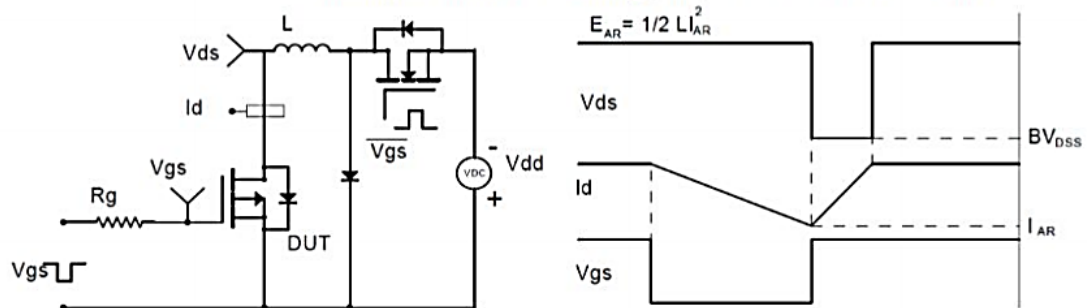
Gate Charge Test Circuit & Waveform



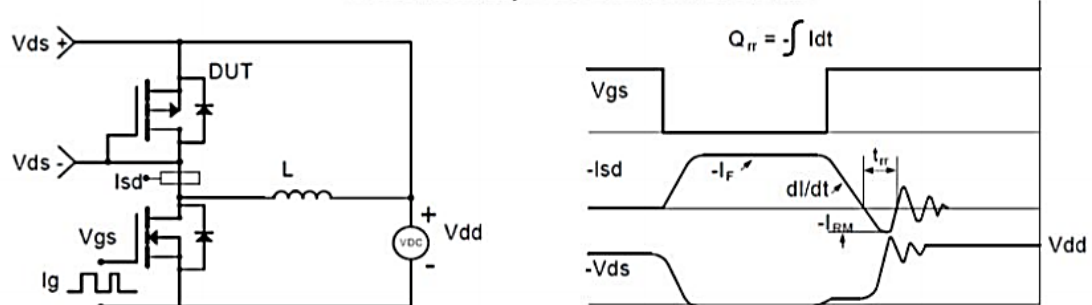
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

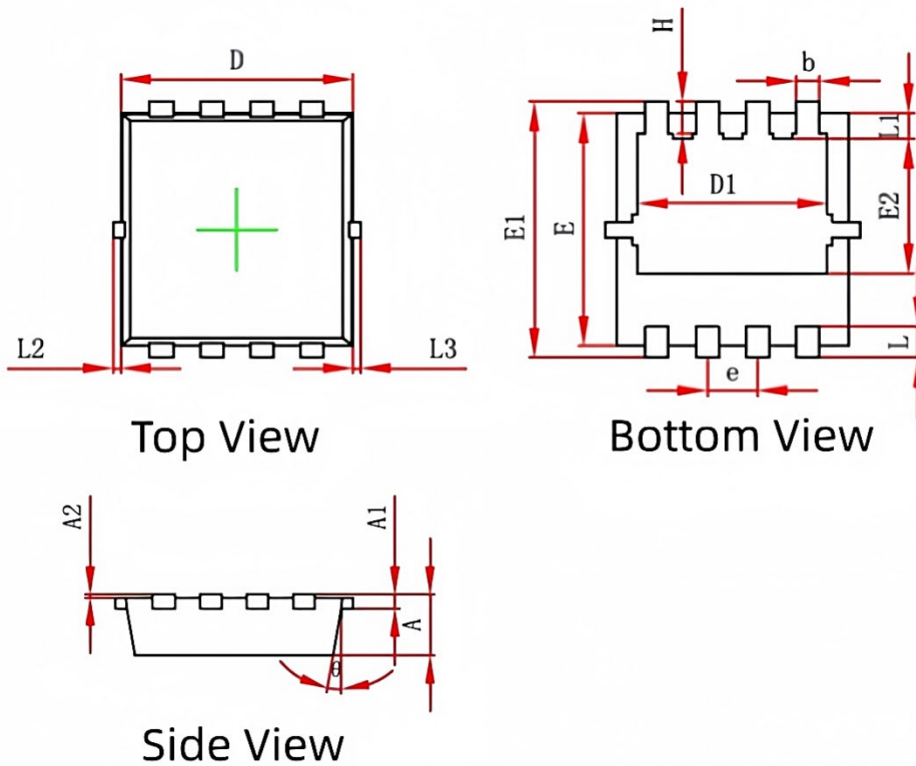


Diode Recovery Test Circuit & Waveforms

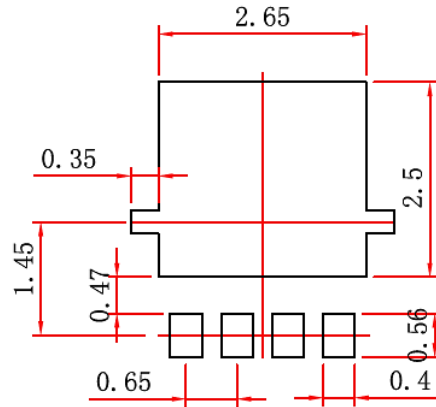




Package Mechanical Data(PDFN 3.3x3.3-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

Ordering information

Order Code	Package	$V_{DS}(V)$	$I_D(A)$	$R_{DS(ON)}(m\Omega)$	
QNM15PD02	PDFN 3.3x3.3-8	-20	-12	$V_{GS}=-4.5V$	14
				$V_{GS}=-2.5V$	18