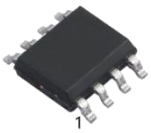
LM2662 Switched Capacitor Voltage Converter

Features

- Inverts or Doubles Input Supply Voltage
- 9-Ω Typical Output Resistance
- 86% Typical Conversion Efficiency at 200 mA
- Selectable Oscillator Frequency: 20kHz/150 kHz

DIP-8



SOP-8

MSOP-8

DFN-8 3*3

Applications

- Laptop Computers
- Cellular Phones
- Medical Instruments
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

Ordering Information

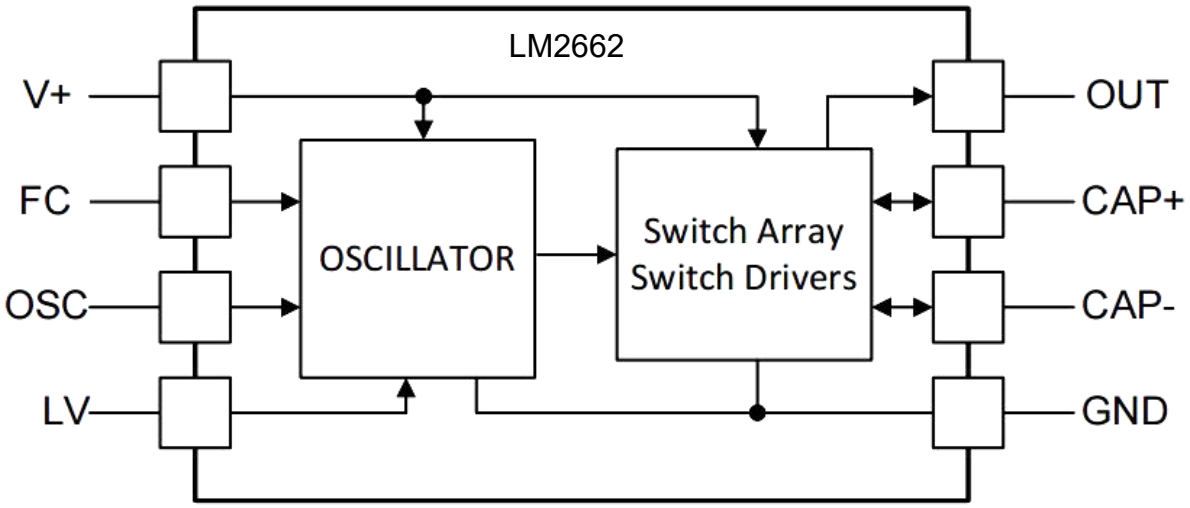
DEVICE	Package Type	MARKING	Packing	Packing Qty
LM2662N/HG	DIP-8	LM2662	TUBE	2000pcs/reel
LM2662M/TR-HG	SOP-8	LM2662	REEL	2500pcs/reel
LM2662MM/TR-HG	MSOP-8	LM2662,2662	REEL	3000pcs/reel
LM2662DQ3/TR-HG	DFN-8 3*3	LM2662,2662	REEL	5000pcs/reel

Description

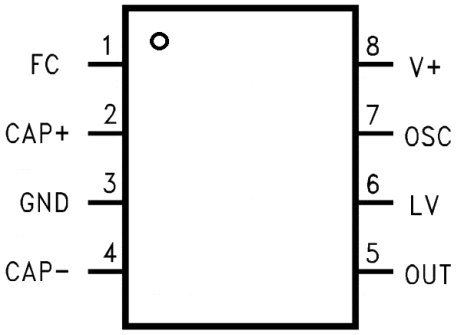
The LM2662 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5 V to 5.5 V to the corresponding negative voltage.The LM2662 uses two low cost capacitors to provide 200 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 300 μA and operating efficiency greater than 90% at most loads, the LM2662 provides ideal performance for battery powered systems. The LM2662 may also be used as a positive voltage doubler.

The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2662 with an external clock. For LM2662, a frequency control(FC) pin selects the oscillator frequency of 20 kHz or 150 kHz.

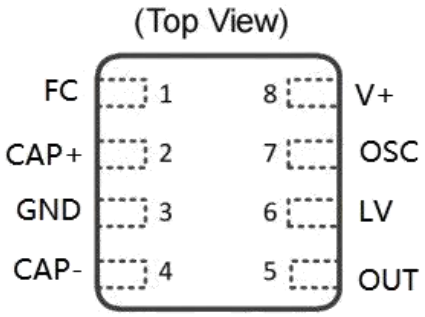
Functional Block Diagram



Pin Configuration and Functions



DIP-8/SOP-8/MSOP-8



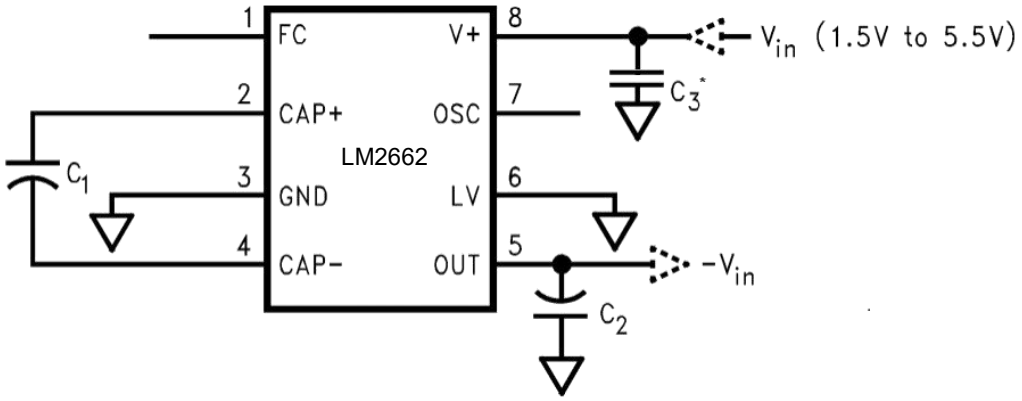
DFN-8 3*3

Pin Functions

PIN		TYPE	DESCRIPTION	
NUMBE R	NAME		VOLTAGE INVERTER	VOLTAGE DOUBLER
1	FC	Input	Frequency control for internal oscillator: FC = open, f_{OSC} = 20 kHz (typ); FC = V+, f_{OSC} = 150 kHz (typ); FC has no effect when OSC pin is driven externally.	Same as inverter.
2	CAP+	Power	Connect this pin to the positive terminal of charge-pump capacitor.	Same as inverter.
3	GND	Ground	Power supply ground input.	Power supply positive voltage input.
4	CAP−	Power	Connect this pin to the negative terminal of charge-pump capacitor.	Same as inverter.
5	OUT	Power	Negative voltage output.	Power supply ground input.
6	LV	Input	Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5 V. Above 3.5 V, LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND.	LV must be tied to OUT.
7	OSC	Input	Oscillator control input. OSC is connected to an internal 15-pF capacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC.	Same as inverter except that OSC cannot be driven by an external clock.
8	V+	Power Input	Power supply positive voltage input.	Positive voltage output.

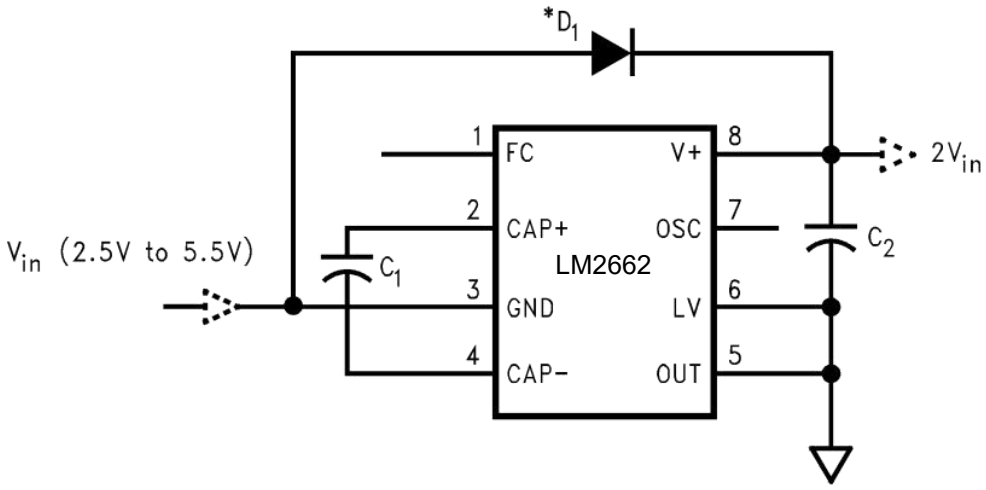
Application Diagram

Voltage Inverter



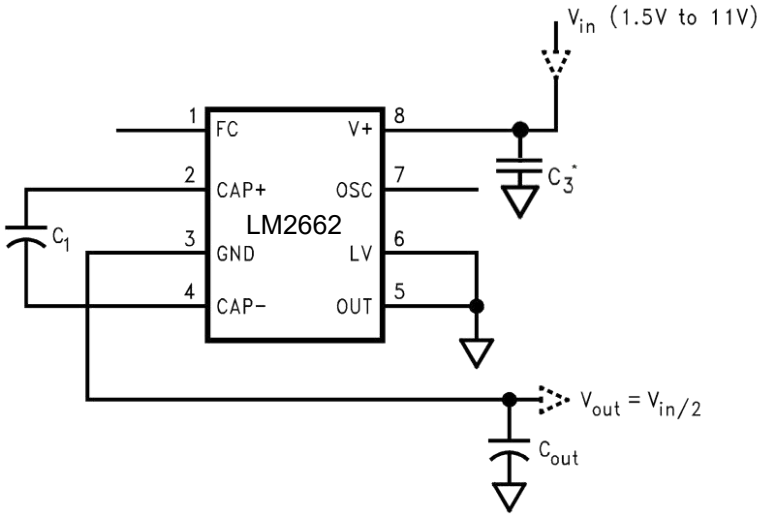
* When Iout>100ma FC=Vdd, the C_3 capacitance should be greater than 0.1uf.

Positive Voltage Doubler



* Please see Positive Voltage Doubler section regarding choice of D1.

Splitting VIN in Half



* When Iout>100ma FC=Vdd, the C_3 capacitance should be greater than 0.1uf.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or GND to OUT)		7.5	V
LV	OUT − 0.3 V	GND + 3 V	
FC, OSC	The least negative of (OUT − 0.3 V) or (V+ − 6 V) to (V+ + 0.3 V)		
V+ and OUT continuous output current		250	
Output short-circuit duration to GND(3)		1	sec.
Power dissipation (TA = 25°C)(4)		735	mW
T_J max(4)		150	°C
Operating ambient temperature	−40	85	
Operating junction temperature	−40	105	
Lead temperature (soldering, 10 seconds)		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package

Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000		V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V+ (supply voltage)	2.5	5.5	V
Junction temperature (T_J)	–40	105	°C
Ambient temperature (T_J)	–40	85	

Thermal Information

THERMAL METRIC(1)		SOP-8	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Electrical Characteristics

Unless otherwise specified: V+ = 5 V, FC = Open, $C_1 = C_2 = 47$ µF.(1)

PARAMETER		TEST CONDITION		MIN(2)	TYP(3)	MAX(2)	UNIT
V_+	Supply Voltage	RL = 1k	Inverter, LV = Open	3.5		5.5	V
			Inverter, LV = GND	1.5		5.5	
			Doubler, LV = OUT	2.5		5.5	
I_Q	Supply Current	No Load LV = Open	FC = V+		1.3	4	A
			FC = Open		0.3	0.8	
I_L	Output Current			200			mA
R_{OUT}	Output Resistance(5)(7)	IL = 200 mA			9	13	Ω
f_{OSC}	Oscillator Frequency	OSC = Open	FC = Open	7	20		kHz
			FC = V+	55	150		
f_{SW}	Switching Frequency(6)	OSC = Open	FC = Open	3.5	10		kHz
			FC = V+	27.5	75		
I_{OSC}	OSC Input Current	FC = Open			±2		µA
		FC = V+			±10		
P_{EFF}	Power Efficiency	RL (500) between V+ and OUT		90%	96%		
		IL = 200 mA to GND			86%		
V_{OEFF}	Voltage Conversion Efficiency	No Load		99%	99.96%		

(1) In the test circuit, capacitors C_1 and C_2 are 47-µF, 0.2-Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

(2) –40°C to 105°C

(3) T_J = 25°C

(4) In doubling mode, when V_{out} > 5 V, minimum input high for shutdown equals V_{out} − 3 V.

(5) Specified output resistance includes internal switch resistance and capacitor ESR.

(6) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

(7)When Iout>100ma FC=Vdd, the capacitance should be greater than 0.1uf.

Typical Performance Characteristics

(Circuit of Figure 13)

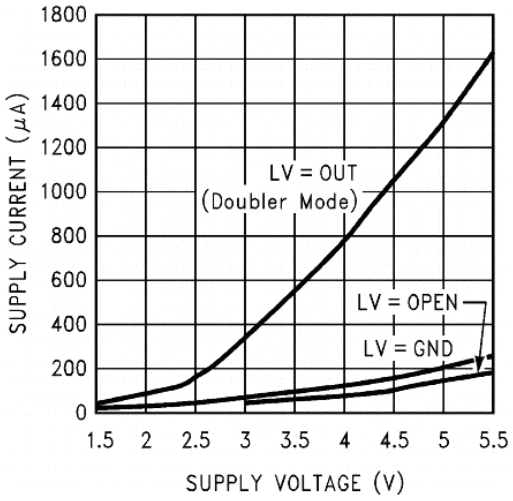


Figure 1. Supply Current vs Supply Voltage

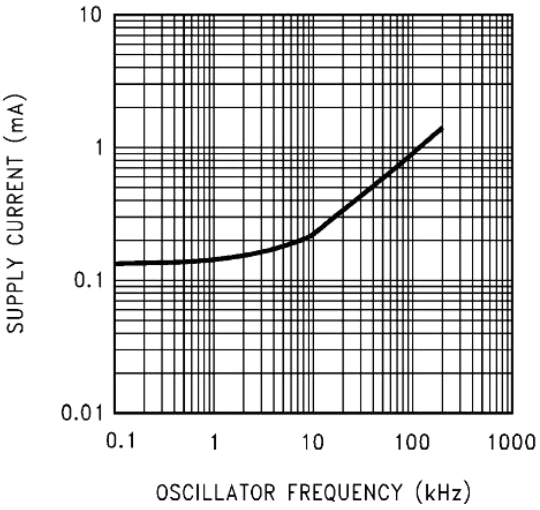


Figure 2. Supply Current vs Oscillator Frequency

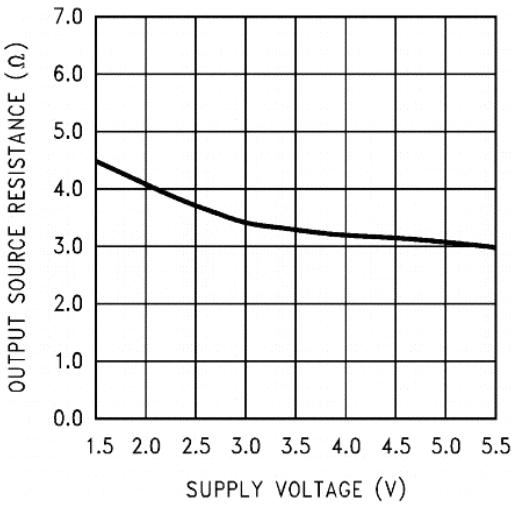


Figure 3. Output Source Resistance vs Supply Voltage

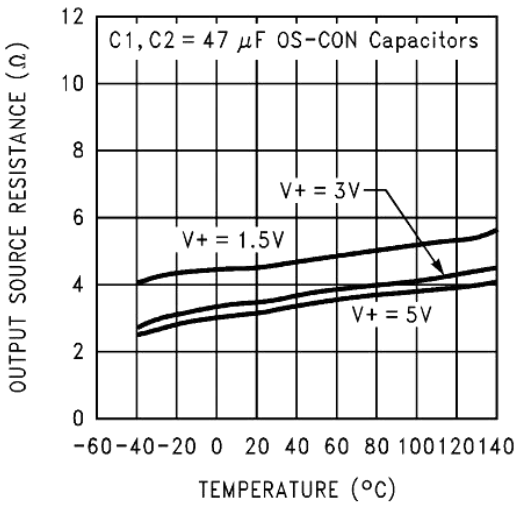


Figure 4. Output Source Resistance vs Temperature

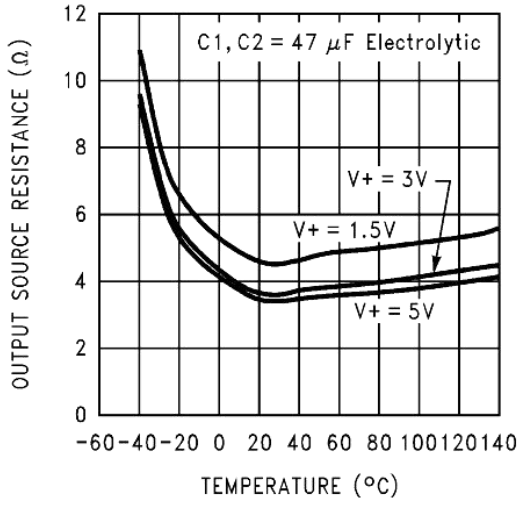


Figure 5. Output Source Resistance vs Temperature

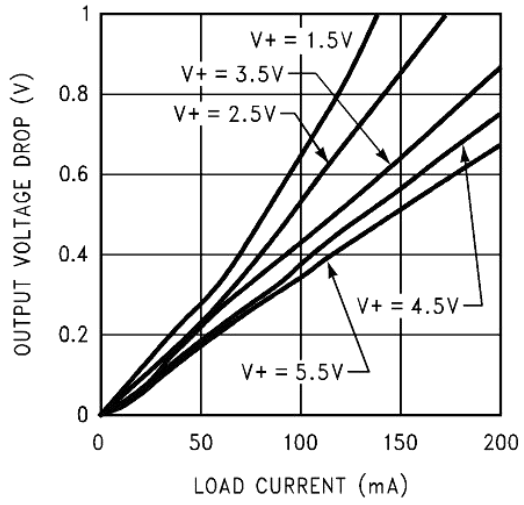


Figure 6. Output Voltage Drop vs Load Current

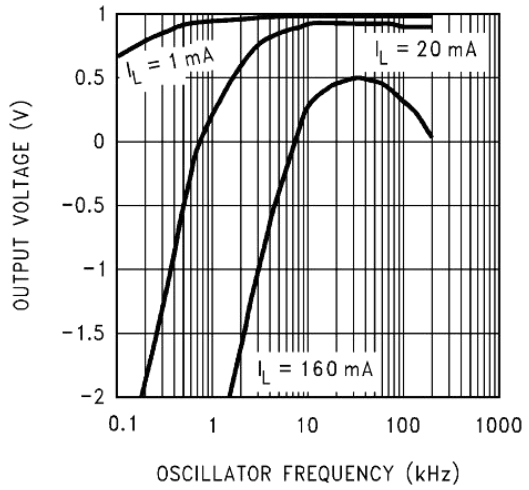


Figure 7. Output Voltage vs Oscillator Frequency

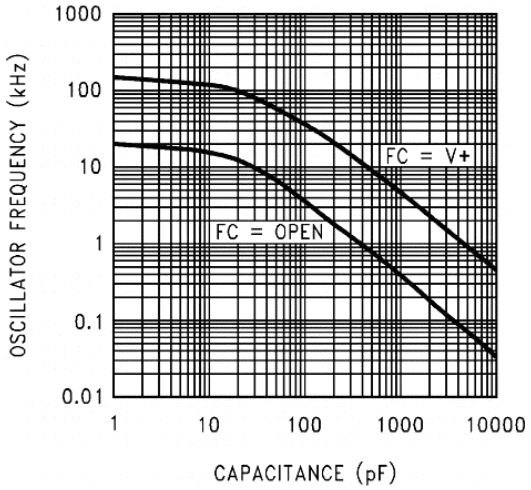


Figure 8. Oscillator Frequency vs External Capacitance

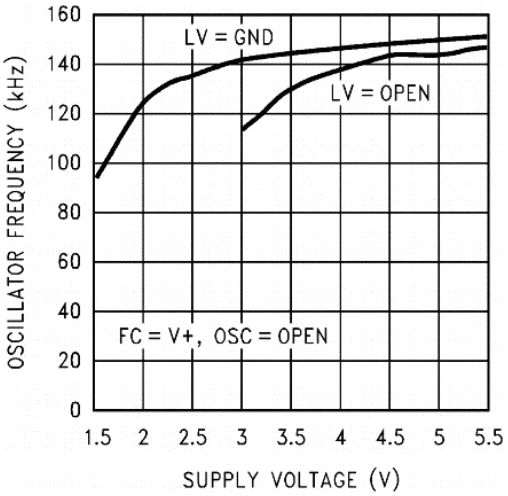


Figure 9. Oscillator Frequency vs Supply Voltage

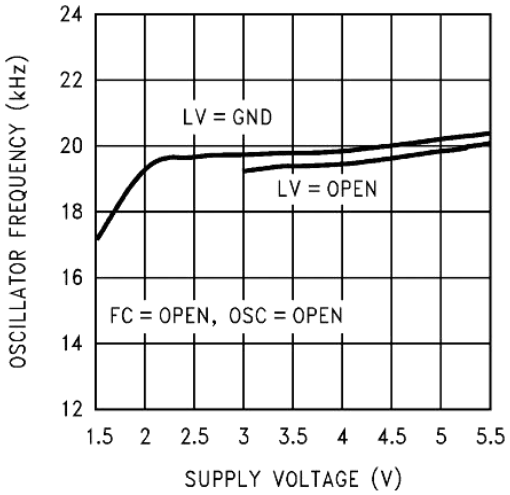


Figure 10. Oscillator Frequency vs Supply Voltage

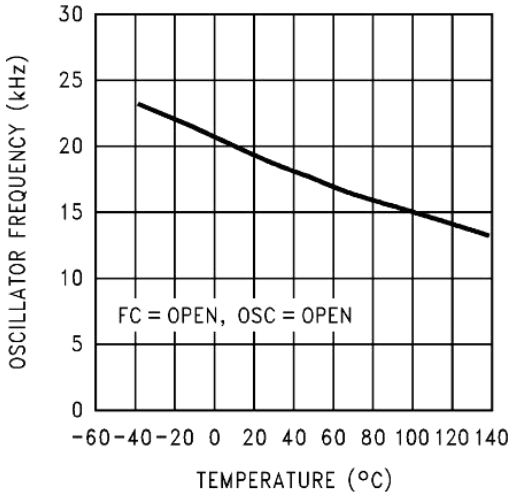


Figure 11. Oscillator Frequency vs Temperatur

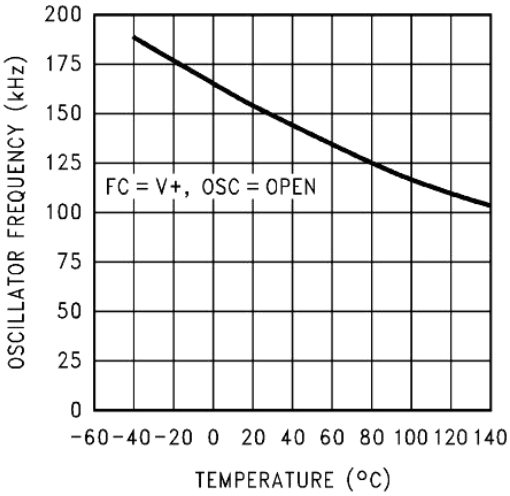
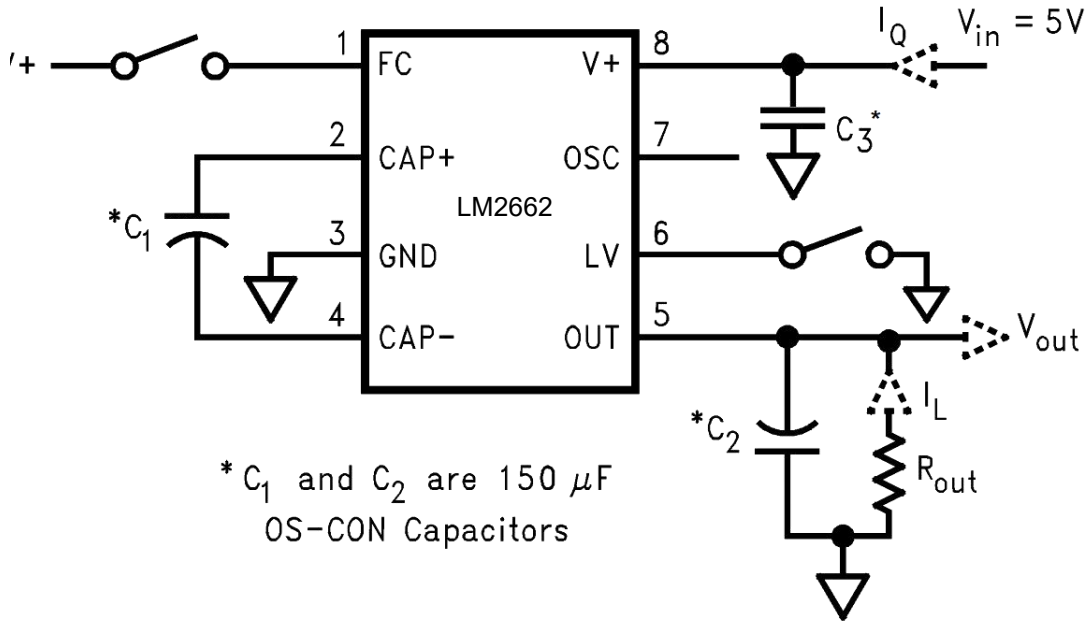


Figure 12. Oscillator Frequency vs Temperature

Parameter Measurement Information



* When Iout>100ma FC=Vdd, the C_3 capacitance should be greater than 0.1uf.

Figure 13. LM2662 Test Circuit

Detailed Description

Overview

The LM2662 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 14 illustrates the voltage conversion scheme. When S1 and S3 are closed, C1 charges to the supply voltage V+. During this time interval switches S2 and S4 are open. In the second time interval, S1 and S3 are open and S2 and S4 are closed, C1 is charging C2 . After a number of cycles, the voltage across C2 will be pumped to V+. Since the anode of C2 is connected to ground, the output at the cathode of C2 equals −(V+) assuming no load on C2 , no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.

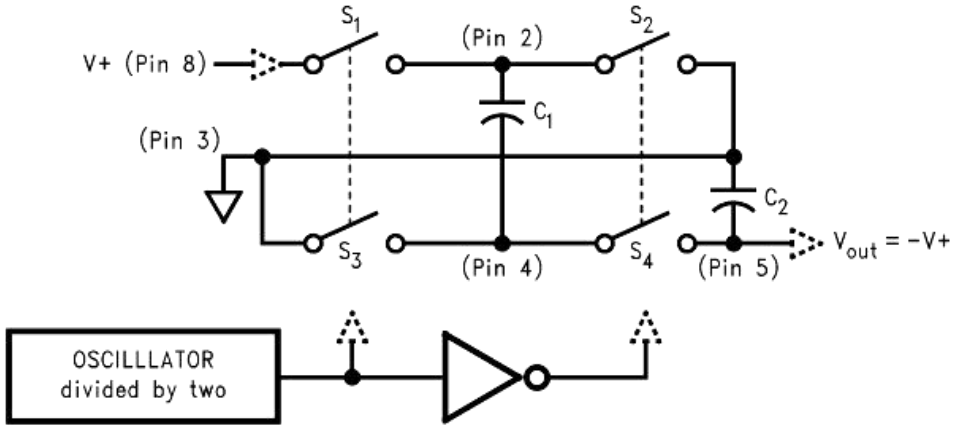


Figure 14. Voltage Inverting Principle

Feature Description

Changing Oscillator Frequency

For the LM2662, the internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 20 kHz; when FC is connected to V+, the frequency increases to 150 kHz. A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.3 mA to 1.3 mA.

The oscillator frequency can be lowered by adding an external capacitor between OSC and GND (See typical performance characteristics). Also, in the inverter mode, an external clock that swings within 100 mV of V+ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency.

NOTE OSC cannot be driven by an external clock in the voltage-doubling mode.

Table 1. LM2662 Oscillator Frequency Selection

FC	OSC	OSCILLATOR
Open	Open	20 kHz
V+	Open	150 kHz
Open or V+	External Capacitor	See Typical Performance Characteristics
N/A	External Clock (inverter mode only)	External Clock Frequency

Application Information

The LM2662 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5 V to 5.5 V to the corresponding negative voltage. The LM2662 uses two low cost capacitors to provide 200 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 300 μA and operating efficiency greater than 90% at most loads, the LM2662 provides ideal performance for battery powered systems. The LM2662 may also be used as a positive voltage doubler.

Typical Applications

Simple Negative Voltage Converter

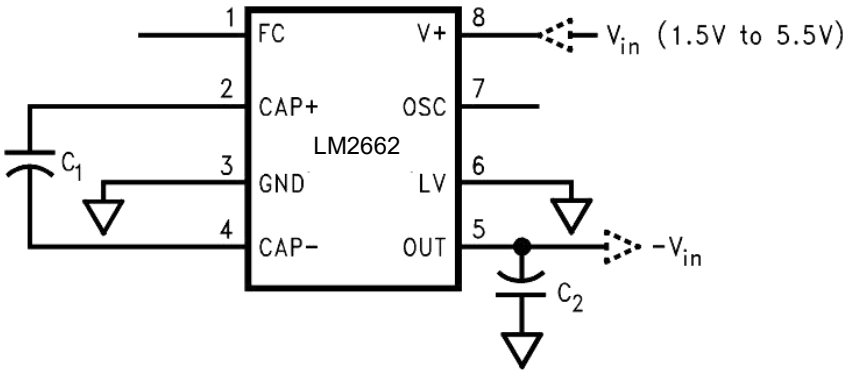


Figure 15. Simple Negative Voltage Converter

Design Requirements

The main application of LM2662 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in Figure 15. The range of the input supply voltage is 1.5 V to 5.5 V. For a supply voltage less than 3.5 V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5 V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the LM2662 for the LMC7660 Switched Capacitor Voltage Converter.

Detailed Design Procedure

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals −(V+). The output resistance R_{out} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C_1 and C_2 . Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation is:

$$R_{out} \cong 2R_{SW} + \frac{2}{f_{osc} \times C_1} + 4\,ESR_{C1} + ESR_{C2} \quad (1)$$

where R_{SW} is the sum of the ON resistance of the internal MOS switches shown in the Voltage Inverting Principle.

High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the 2/(fosc × C1) term. Once this term is trivial compared with RSW and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C_2 :

$$V_{ripple} = \frac{I_L}{f_{osc} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

Again, using a low ESR capacitor will result in lower ripple.

Paralleling Devices

Any number of LM2662 devicess can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C1 , while only one output capacitor Cout is needed as shown in Figure 16. The composite output resistance is:

$$R_{out} = \frac{R_{out} \text{ of each LM2662}}{\text{Number of Devices}} \quad (3)$$

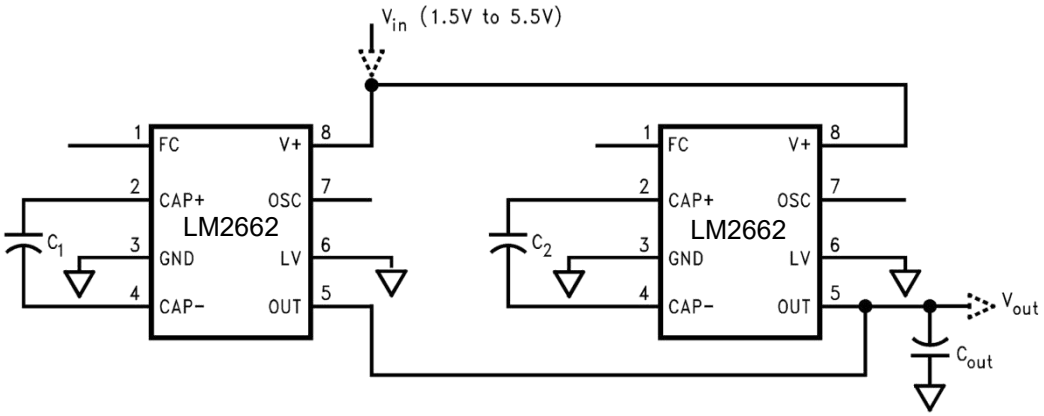


Figure 16. Lowering Output Resistance by Paralleling Devices

Cascading Devices

Cascading the LM2662 devices is an easy way to produce a greater negative voltage (as shown in Figure 17). If n is the integer representing the number of devices cascaded, the unloaded output voltage V_{out}t is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + \frac{n}{2}R_{out\_2} + \ldots + R_{out\_n} \quad (4)$$

A three-stage cascade circuit shown in Figure 18 generates −3 Vin, from Vin.

Cascading is also possible when devices are operating in doubling mode. In Figure 19, two devices are cascaded to generate 3 V_{in}.

An example of using the circuit in Figure 18 or Figure 19 is generating +15 V or −15 V from a +5-V input.

Note that, the number of n is practically limited since the increasing of n significantly reduces the efficiency and increases the output resistance and output voltage ripple.

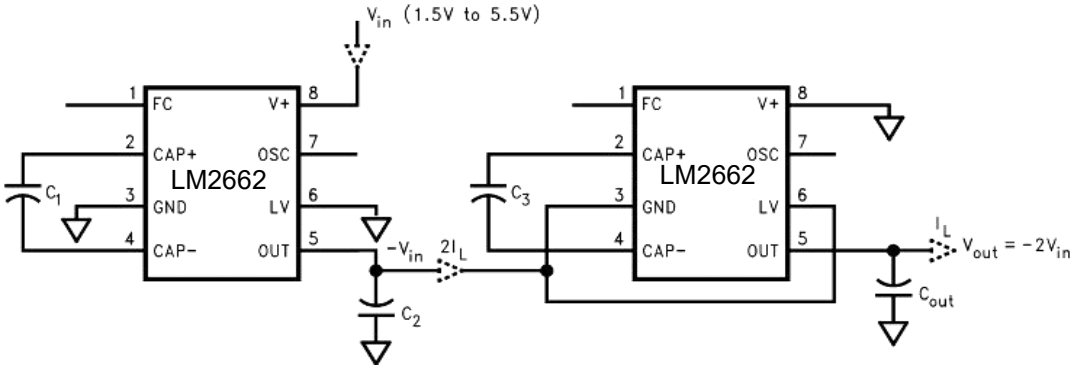


Figure 17. Increasing Output Voltage by Cascading Devices

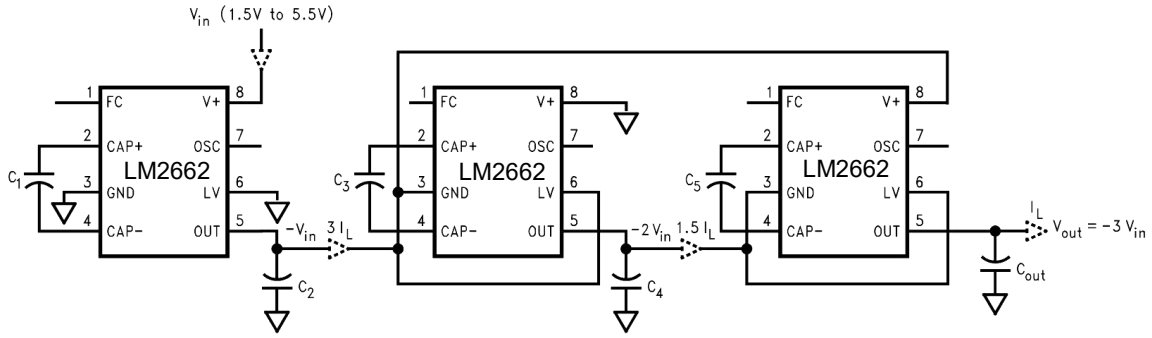


Figure 18. Generating −3 V_{IN} From +V_{IN}

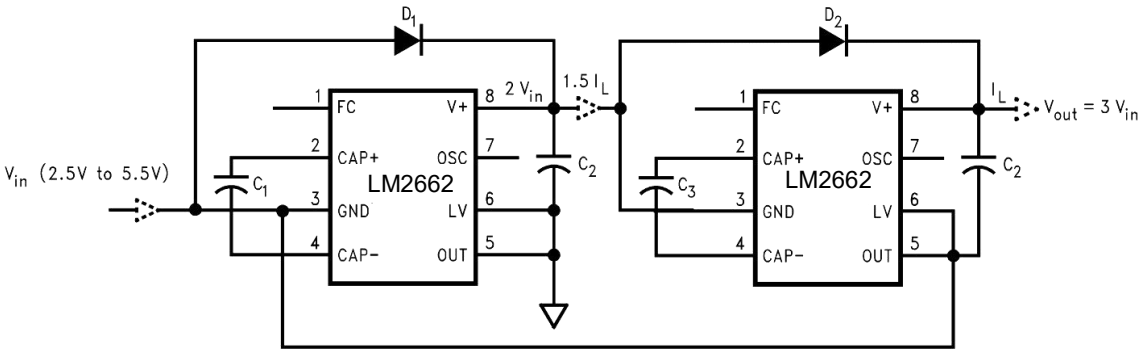


Figure 19. Generating +3 V_{IN} From +VI_N

Regulating V_{OUT}

It is possible to regulate the output of the LM2662 by use of a low dropout regulator (such as LP2986). The whole converter is depicted in Figure 20. This converter can give a regulated output from −1.5 V to −5.5 V by choosing the proper resistor ratio:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{100k}\right) \quad (5)$$

where

- $V_{ref} = 1.23V$

he error flag on pin 7 of the LP2986 goes low when the regulated output at pin 5 drops by about 5% below nominal. The LP2986 can be shutdown by taking pin 8 low. The less than 1 µA quiescent current in the shutdown mode is favorable for battery powered applications.

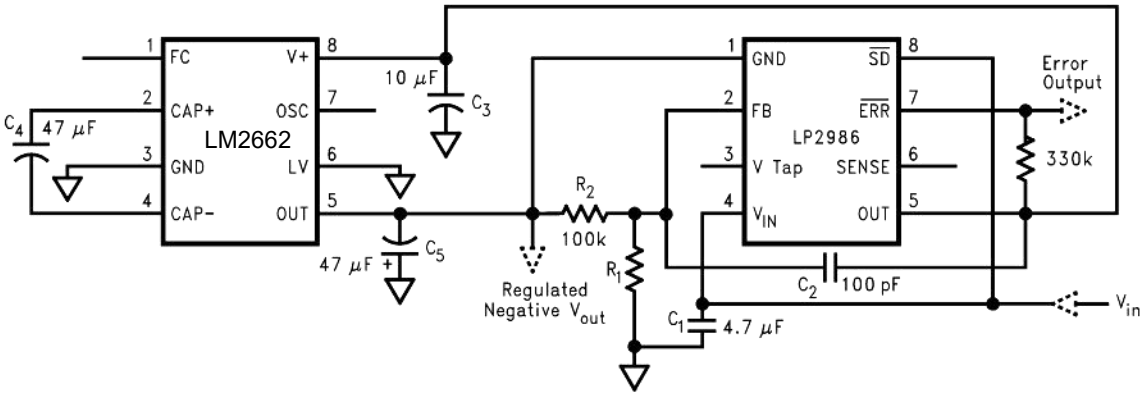


Figure 20. Combining LM2662 With LP2986 to Make a Negative Adjustable Regulator

Also, as shown in Figure 21 by operating the LM2662 in voltage doubling mode and adding a low dropout regulator (such as LP2986) at the output, we can get +5 V output from an input as low as +3.3 V.

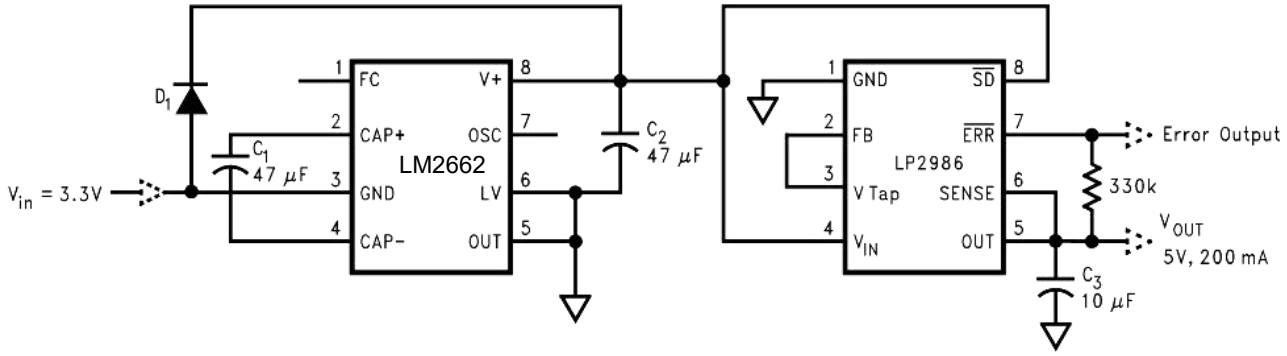


Figure 21. Generating +5 V From +3.3 V Input Voltage

Application Curves

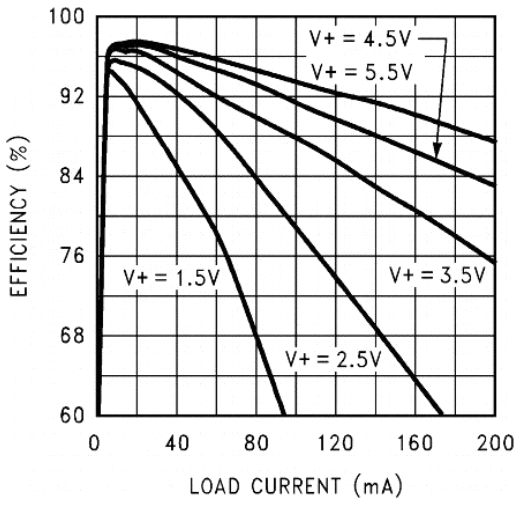


Figure 22. Efficiency vs Load Current

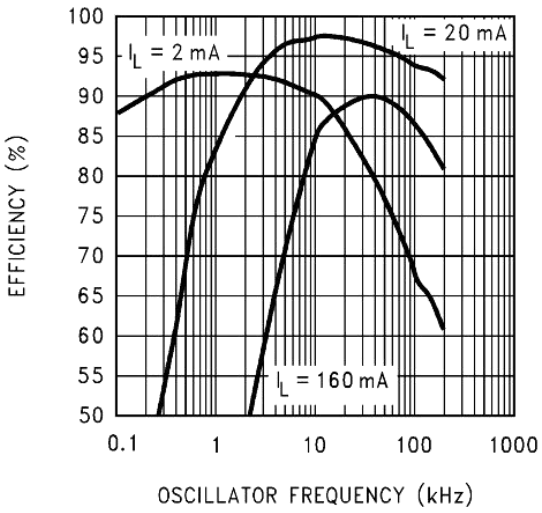


Figure 23. Efficiency vs Oscillator Frequency

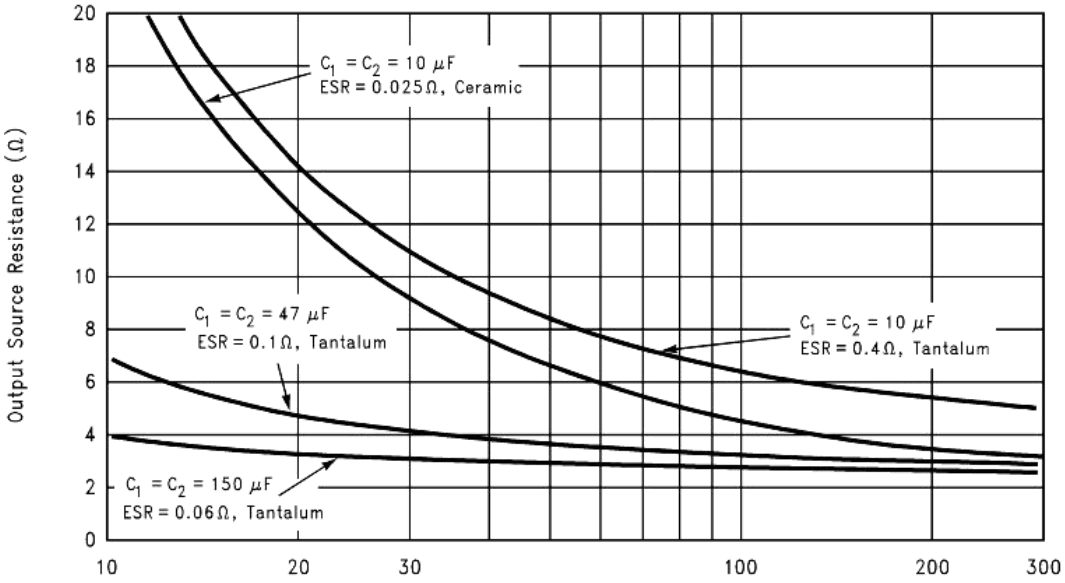


Figure 24. Output Source Resistance vs Oscillator Frequency

Positive Voltage Doubler

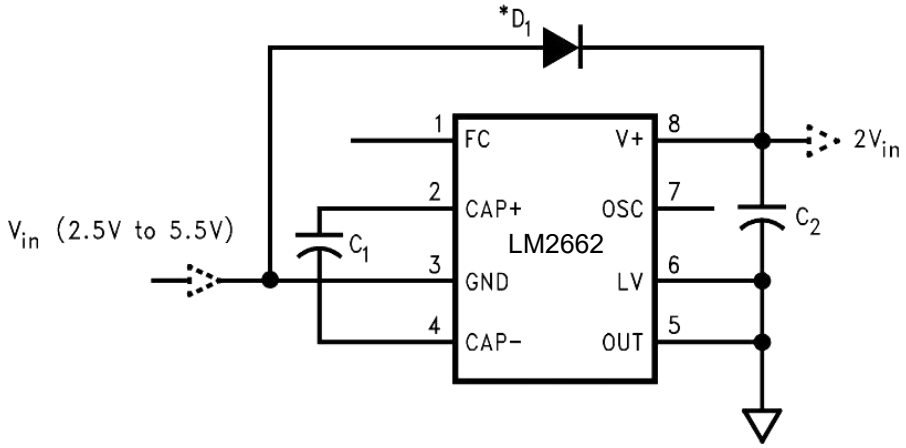


Figure 25. Positive Voltage Doubler

Design Requirements

The LM2662 can operate as a positive voltage doubler (as shown in Figure 25). The doubling function is achieved by reversing some of the connections to the device.

Detailed Design Procedure

The input voltage is applied to the GND pin with an allowable voltage from 2.5 V to 5.5 V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode D_1 's forward drop.

The Schottky diode D_1 is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5 V to insure the operation of the oscillator. During start-up, D_1 is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latchingup. Therefore, the Schottky diode D_1 should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

Splitting V_{IN} in Half

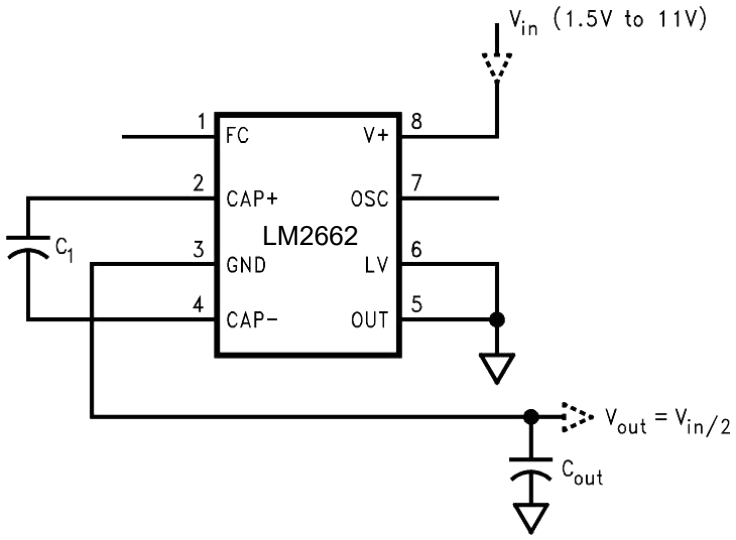


Figure 26. Splitting VIN in Half

Design Requirements

Another interesting application shown in Figure 26 is using the LM2662 as a precision voltage divider. Since the off-voltage across each switch equals $V_{IN}/2$, the input voltage can be raised to +11 V.

Detailed Design Procedure

As discussed in the Simple Negative Voltage Converter section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L{}^2 R_L}{I_L{}^2 R_L + I_L{}^2 R_{out} + I_Q(V+)} \quad (6)$$

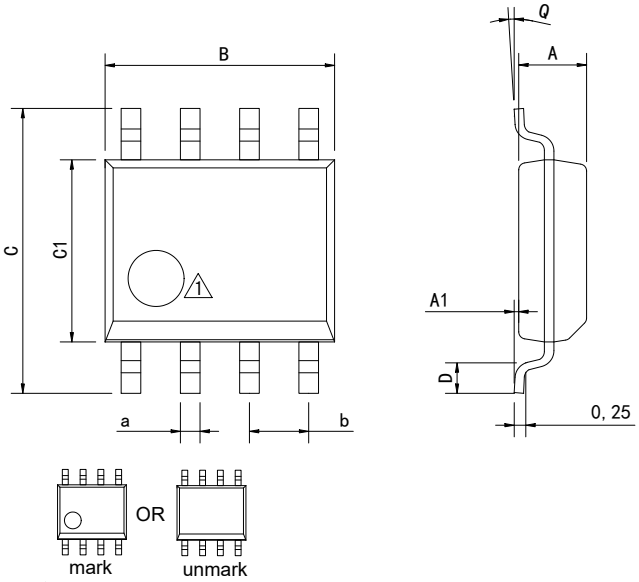
Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $_{IL}{}^2R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

Low ESR capacitors are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, C_1 and C_2 are usually chosen to be the same.

The output resistance varies with the oscillator frequency and the capacitors. In Figure 24, the output resistancevs. oscillator frequency curves are drawn for four difference capacitor values. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 100 kHz for the 47-μF capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. Ceramic capacitors can be chosen for their lower ESR. As shown in Figure 24, in higher frequency range, the output resistance using the 10-μF ceramic capacitors is close to these using higher value tantalum capacitors.

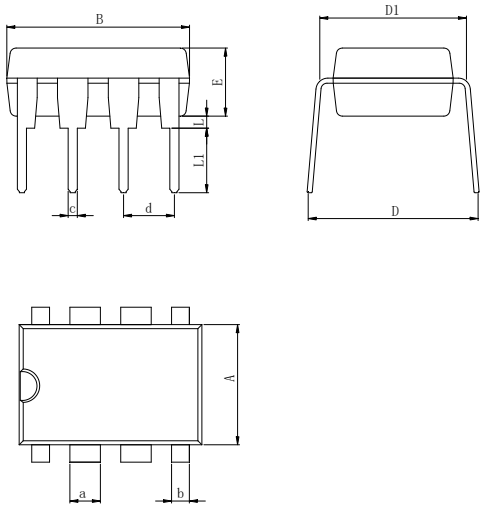
Physical Dimensions

SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

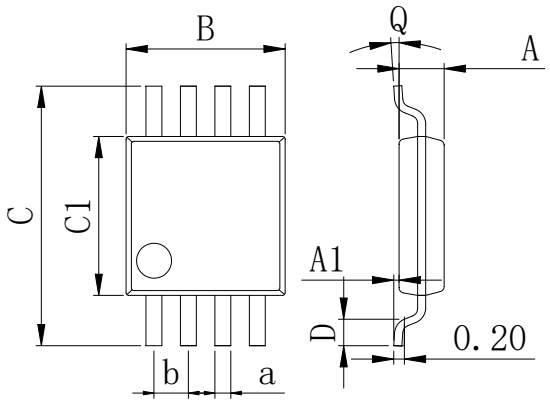
DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	**A**	**B**	**D**	**D1**	**E**	**L**	**L1**	**a**	**b**	**c**	**d**
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.75	1.20	0.50	

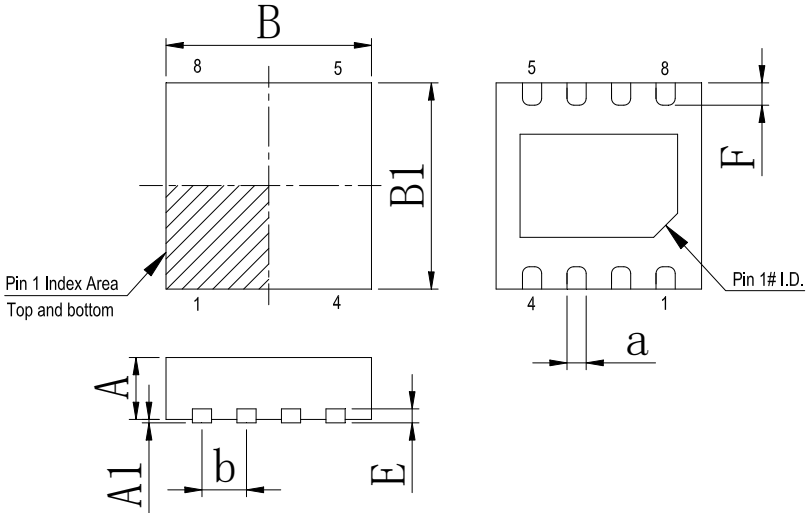
Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

DFN-8 3*3_0.65 Pin spacing



Dimensions In Millimeters(DFN-8 3*3)								
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**a**	**b**
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65 BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2016-5	New	1-21
V1.1	2025-10	Document Reformatting	1-19
V1.2	2025-12	Add DIP-8、MSOP-8 and DFN-8 package model	1

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change products and services offered without prior notice. Customers should obtain the latest relevant information before placing orders and verify that such information is current and complete. Huaguan Semiconductor assumes no responsibility or liability for altered documents.

Customers are responsible for complying with safety standards and implementing safety measures when using Huaguan Semiconductor products in system design and end-product manufacturing. You assume full responsibility for: selecting the appropriate Huaguan Semiconductor products for your application; designing, validating, and testing your application; and ensuring that your application complies with applicable standards and all other safety, security, or other requirements. This is to prevent potential risks that may lead to personal injury or property damage.

Huaguan Semiconductor products are not approved for use in life support, military, aerospace, or other high-risk applications. Huaguan products are neither intended nor warranted for use in such systems or equipment. Any failure or malfunction may lead to personal injury or severe property damage. Such applications are deemed "Unsafe Use." Unsafe Use includes, but is not limited to: surgical and medical equipment, nuclear energy control equipment, aircraft or spacecraft instruments, control or operation of vehicle power, braking, or safety systems, traffic signal instruments, all types of safety devices, and any other applications intended to support or sustain life. Huaguan Semiconductor shall not be liable for consequences resulting from Unsafe Use in these fields. Users must independently evaluate and assume all risks. Any issues, liabilities, or losses arising from the use of products beyond their approved applications shall be solely borne by the user. Users may not claim any compensation from Huaguan Semiconductor based on these terms. If any third party claims against Huaguan Semiconductor due to such Unsafe Use, the user shall compensate Huaguan Semiconductor for all resulting damages and liabilities.

Huaguan Semiconductor provides technical and reliability data (including datasheets), design resources (including reference designs), application or other design advice, web tools, safety information, and other resources for its semiconductor products. However, no guarantee is made that these resources are free from defects, and no express or implied warranties are provided. The use of testing and other quality control techniques is limited to Huaguan Semiconductor's quality assurance scope. Not all parameters of each device are tested.

Huaguan Semiconductor's documentation authorizes you to use these resources only for developing applications related to the products described herein. You are not granted rights to any other intellectual property of Huaguan Semiconductor or any third party. Any other reproduction or display of these resources is strictly prohibited. You shall fully indemnify Huaguan Semiconductor and its agents against any claims, damages, costs, losses, and liabilities arising from your use of these resources. Huaguan Semiconductor shall not be held responsible.