



QNHCHIP

QNM40N03AJ

Product Specification

QNM40N03AJ

30V N-Channel MOSFET



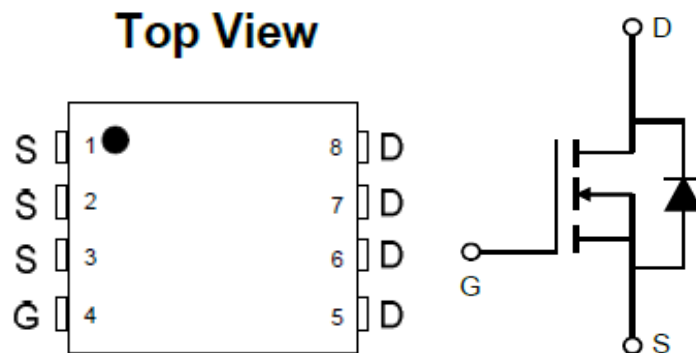
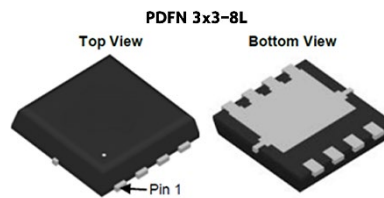
FEATURES

- 30V, 40A
 $R_{DS(ON)}$ Typ= 5.5m Ω @ $V_{GS} = 10V$
 $R_{DS(ON)}$ Typ= 8m Ω @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge

Applications

- Load Switch
- PWM Application
- Power Management

Pin Description



NO.	Symbol	Description
1	S	SOURCE
2	S	SOURCE
3	S	SOURCE
4	G	GATE
5	D	DRAIN
6	D	DRAIN
7	D	DRAIN
8	D	DRAIN



Absolute Maximum Ratings

(@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units	
V_{DS}	Drain-to-Source Voltage	30	V	
V_{GS}	Gate-to-Source Voltage	± 20	V	
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	40	A
		$T_C = 100^\circ\text{C}$	26	
I_{DM}	Pulsed Drain Current ⁽¹⁾	100	A	
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	35	mJ	
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	6	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	39.6	$^\circ\text{C}/\text{W}$	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	21.1		
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$	



Electrical Characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.6	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS}=10\text{V}, I_D=20\text{A}$	-	5.5	11.2	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=10\text{A}$	-	8	13.9	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V},$ $f=1\text{MHz}$	-	838	-	pF
C_{oss}	Output Capacitance		-	162	-	pF
C_{rss}	Reverse Transfer Capacitance		-	102	-	pF
Q_g	Total Gate Charge	$V_{GS}=0\sim 10\text{V}$ $V_{DD}=15\text{V}, I_D=20\text{A}$	-	20	-	nC
Q_{gs}	Gate Source Charge		-	4	-	nC
Q_{gd}	Gate Drain ("Miller") Charge		-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DD}=15\text{V},$ $I_D=20\text{A}, R_{GEN}=3\Omega$	-	6	-	ns
t_r	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	22	-	ns
t_f	Turn-Off Fall Time		-	5	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward	-	-	40	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward	-	-	100	A	
V_{SD}	Drain to Source Diode	$V_{GS}=0\text{V}, I_S=30\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery	$I_F=20\text{A}, di/dt=100\text{A}/\mu\text{s}$	-	8	-	ns
Q_{rr}	Body Diode Reverse Recovery		-	1.6	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=20\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=11.9\text{A}$
3. $R_{\theta JA}$ is measured with the device mounted on a 1 inch² pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Output Characteristics

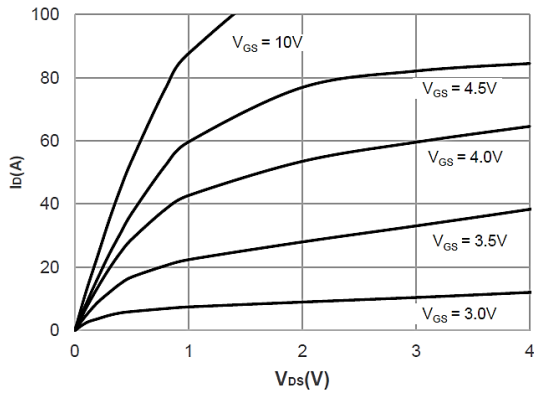


Figure 2: Typical Transfer Characteristics

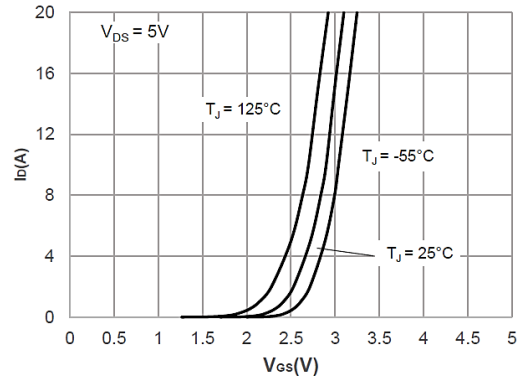


Figure 3: On-resistance vs. Drain Current

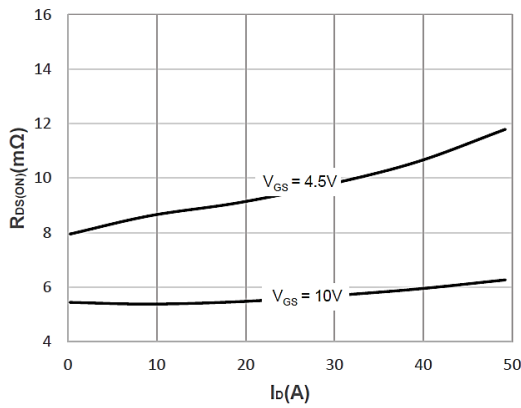


Figure 4: Body Diode Characteristics

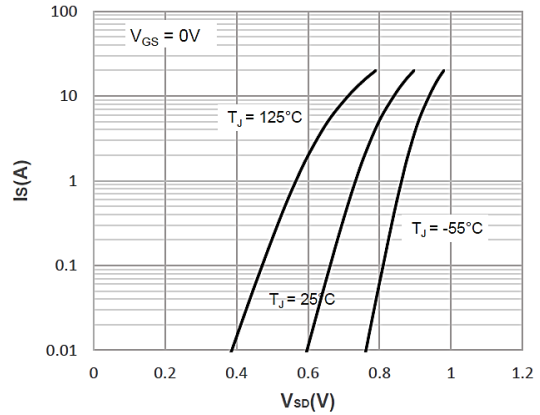


Figure 5: Gate Charge Characteristics

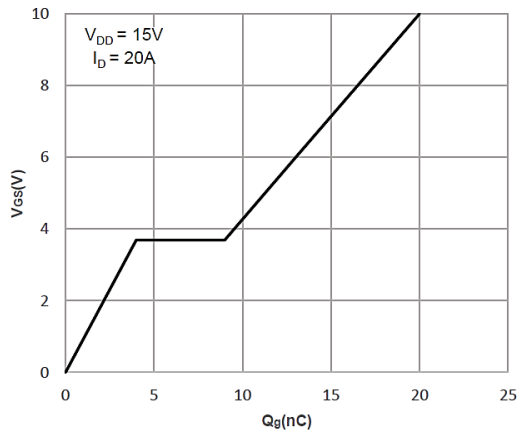


Figure 6: Capacitance Characteristics

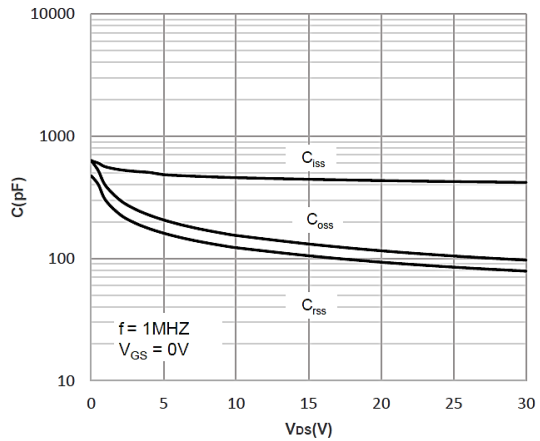


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

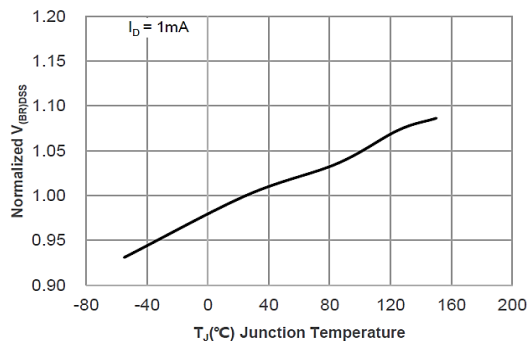


Figure 8: Normalized on Resistance vs. Junction Temperature

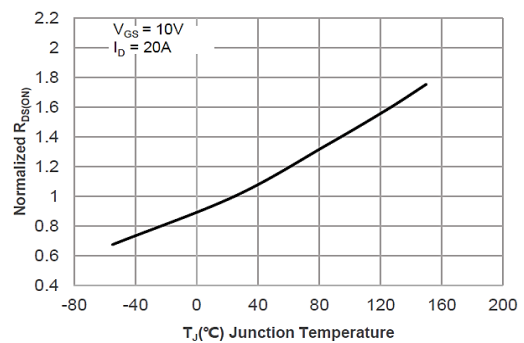




Figure 9: Maximum Safe Operating Area

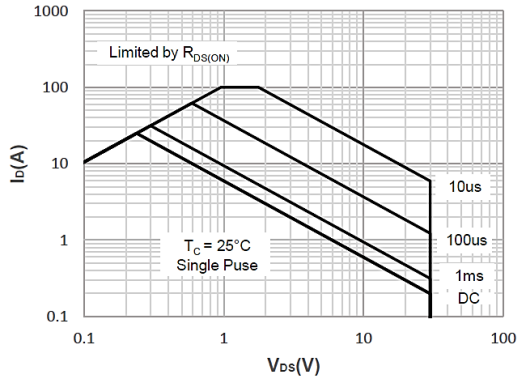


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

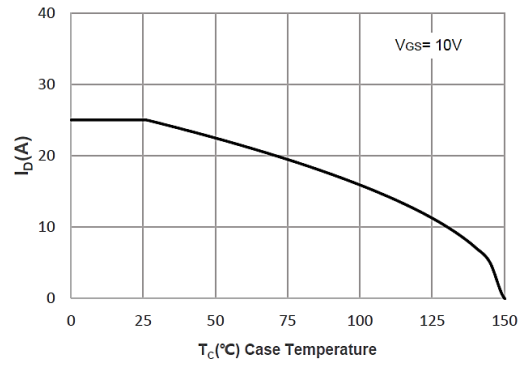


Figure 11: Normalized Maximum Transient Thermal Impedance

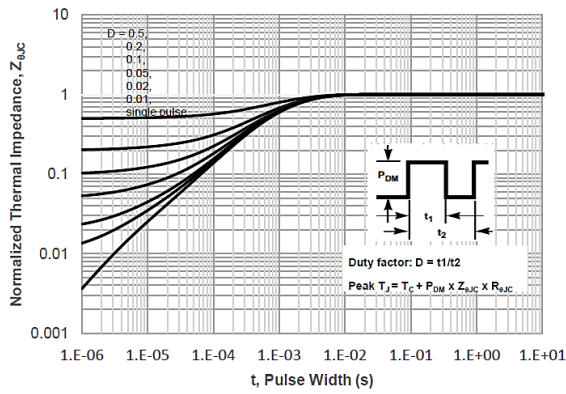
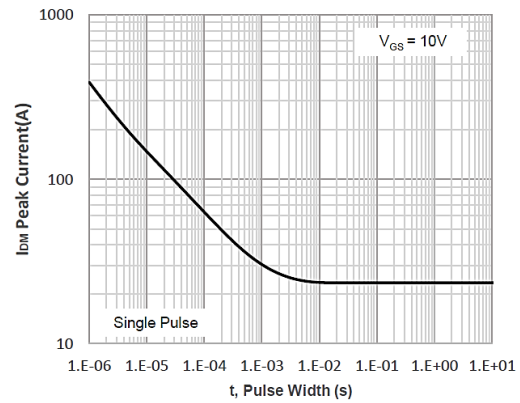


Figure 12: Peak Current Capacity





Test Circuit

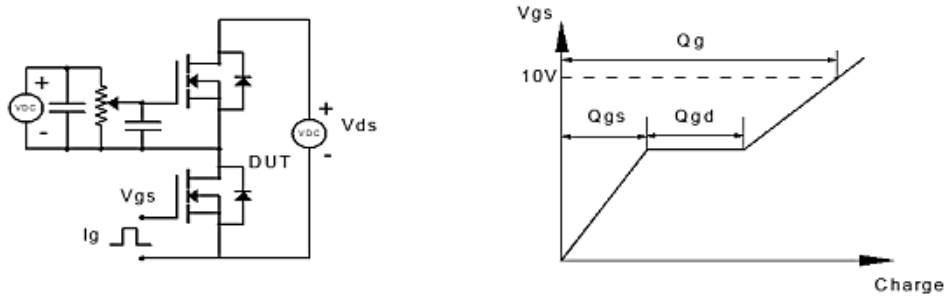


Figure 1: Gate Charge Test Circuit & Waveform

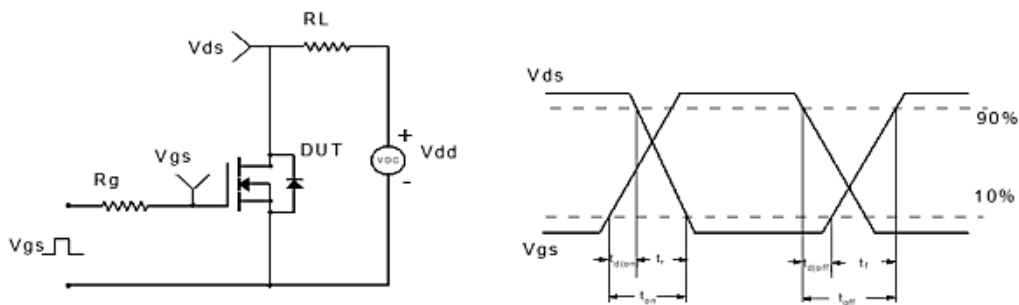


Figure 2: Resistive Switching Test Circuit & Waveform

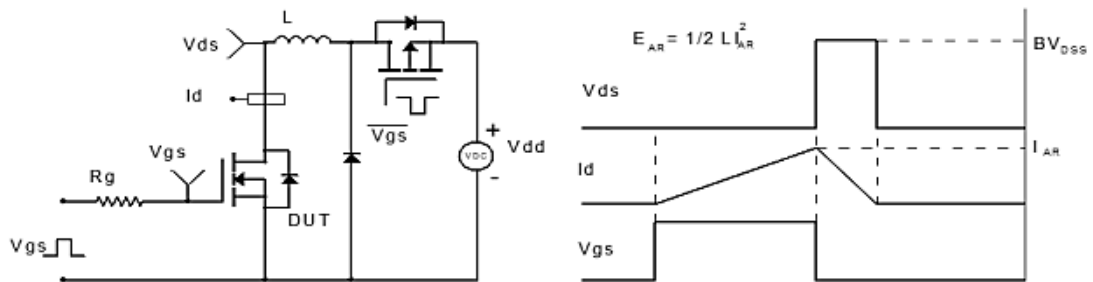


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

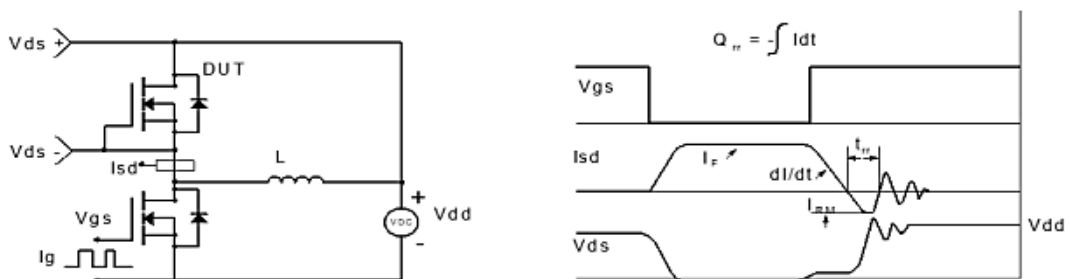
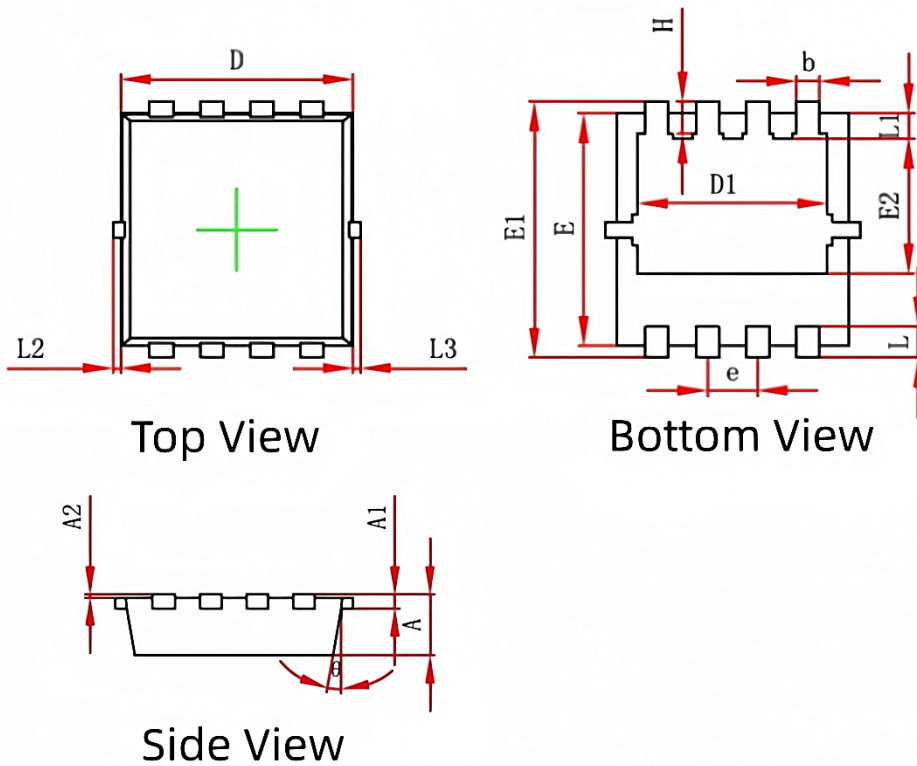


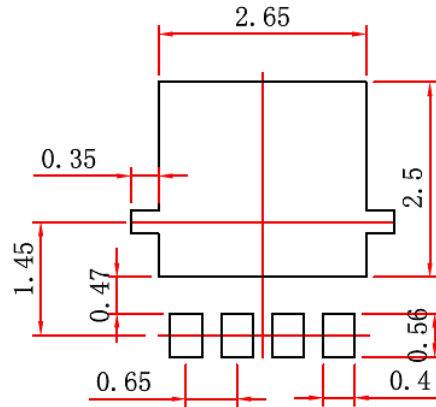
Figure 4: Diode Recovery Test Circuit & Waveform



Package Mechanical Data(PDFN 3x3-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

Ordering information

Order Code	Package	$V_{DS}(V)$	$I_D(A)$	$R_{DS(ON)}(m\Omega)$	
QNM40N03AJ	PDFN 3x3-8	30	40	$V_{GS}=10V$	5.5
				$V_{GS}=4.5V$	8