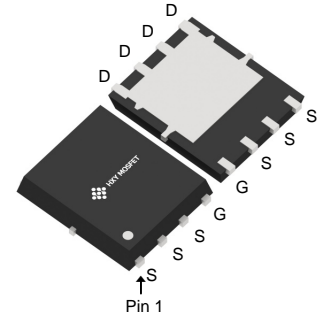




### Description

The SM6442D1RL uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



DFN5X6-8L  
(TDFN-8(5.2x5.9))

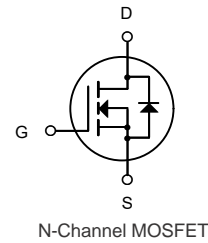
### General Features

$V_{DS} = 40V$   $I_D = 70A$

$R_{DS(ON)} < 8.5m\Omega @ V_{GS}=10V$

### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SM6442D1RL	DFN5X6-8L(TDFN-8(5.2x5.9))	HXY MOSFET	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	70	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	44	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	280	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	76	mJ
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	72.3	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.73	$^\circ C/W$



**Electrical Characteristics (Ta=25°C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =10A	---	7.5	8.5	mΩ
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =5A	---	10	15	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	1.7	3	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ± 20V , V <sub>DS</sub> =0V	---	---	± 100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =5A	---	13	---	S
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V , V <sub>GS</sub> =10V , I <sub>D</sub> =10A	---	20	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	2.8	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	5.1	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V , V <sub>GS</sub> =10V R <sub>G</sub> =3.3 Ω I <sub>D</sub> =1A	---	13.2	---	ns
T <sub>r</sub>	Rise Time		---	2.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	72	---	
T <sub>f</sub>	Fall Time		---	4.5	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V , V <sub>GS</sub> =0V , f=1MHz	---	1278	---	pF
C <sub>oss</sub>	Output Capacitance		---	135	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	87	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	70	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>s</sub> =1A , T <sub>J</sub> =25°C	---	---	1	V

**Note :**

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%.
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V,V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=47A.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.



### Typical Characteristics

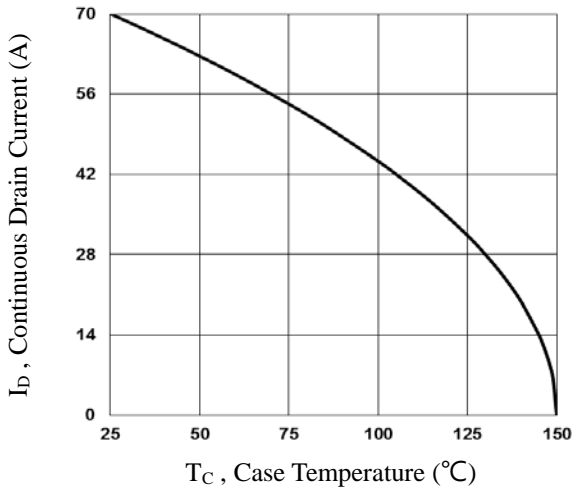


Fig.1 Continuous Drain Current vs. T<sub>C</sub>

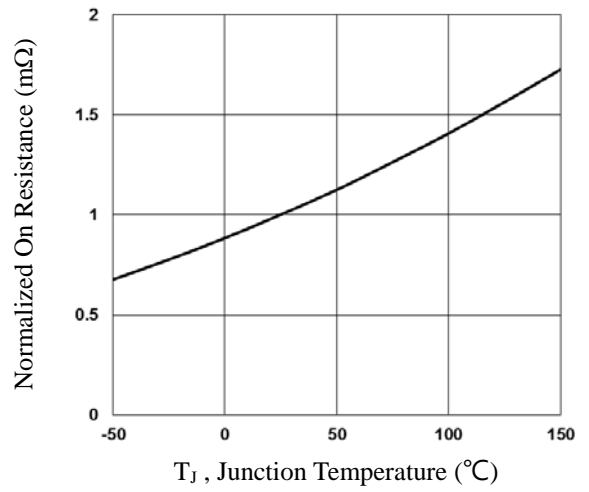


Fig.2 Normalized R<sub>DS(on)</sub> vs. T<sub>J</sub>

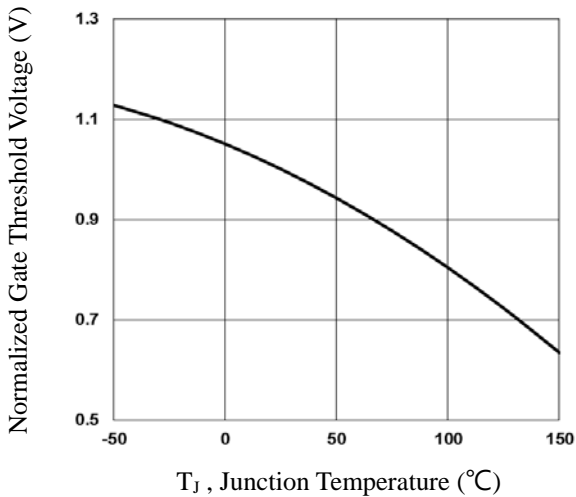


Fig.3 Normalized V<sub>th</sub> vs. T<sub>J</sub>

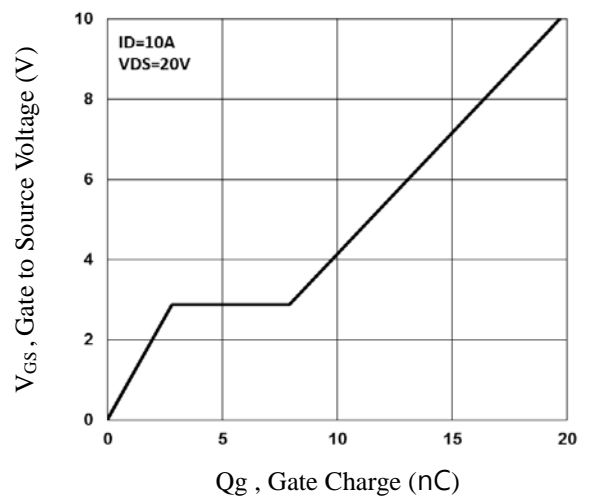


Fig.4 Gate Charge Waveform

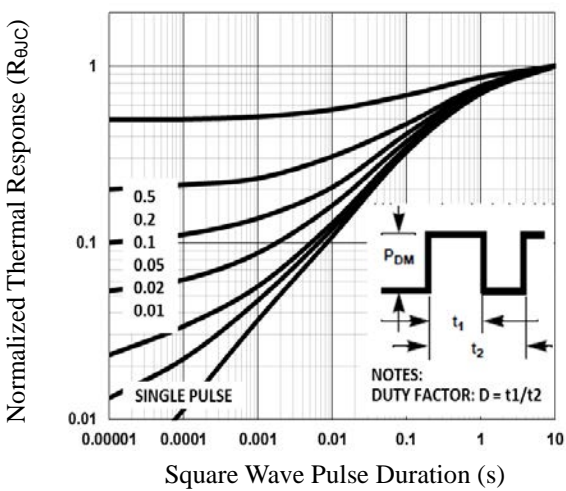


Fig.5 Normalized Transient Impedance

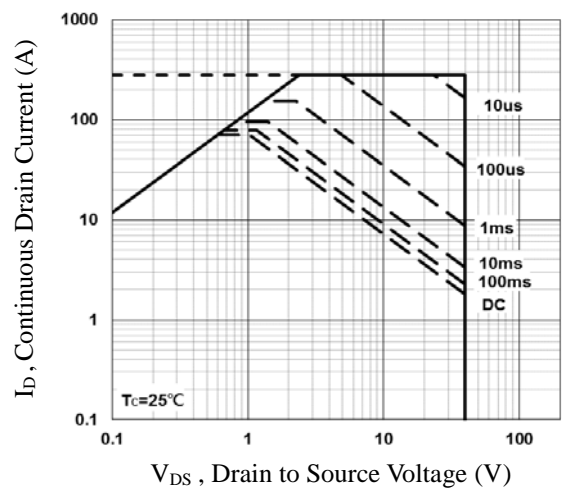


Fig.6 Maximum Safe Operation Area

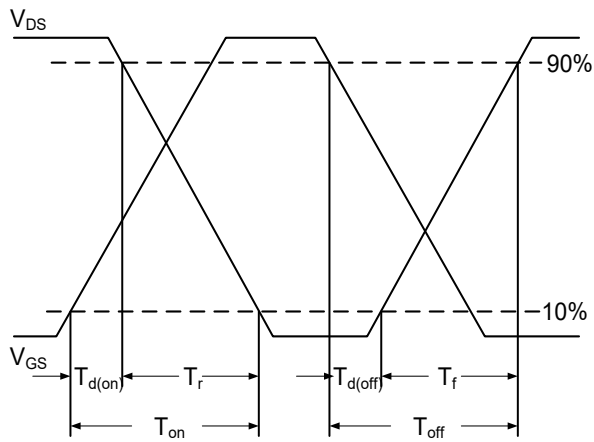


Fig.7 Switching Time Waveform

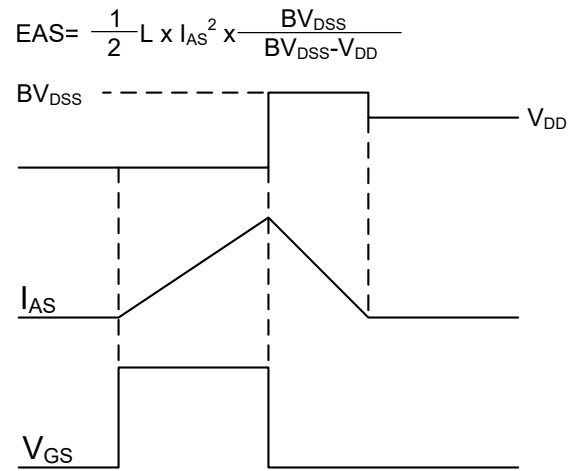
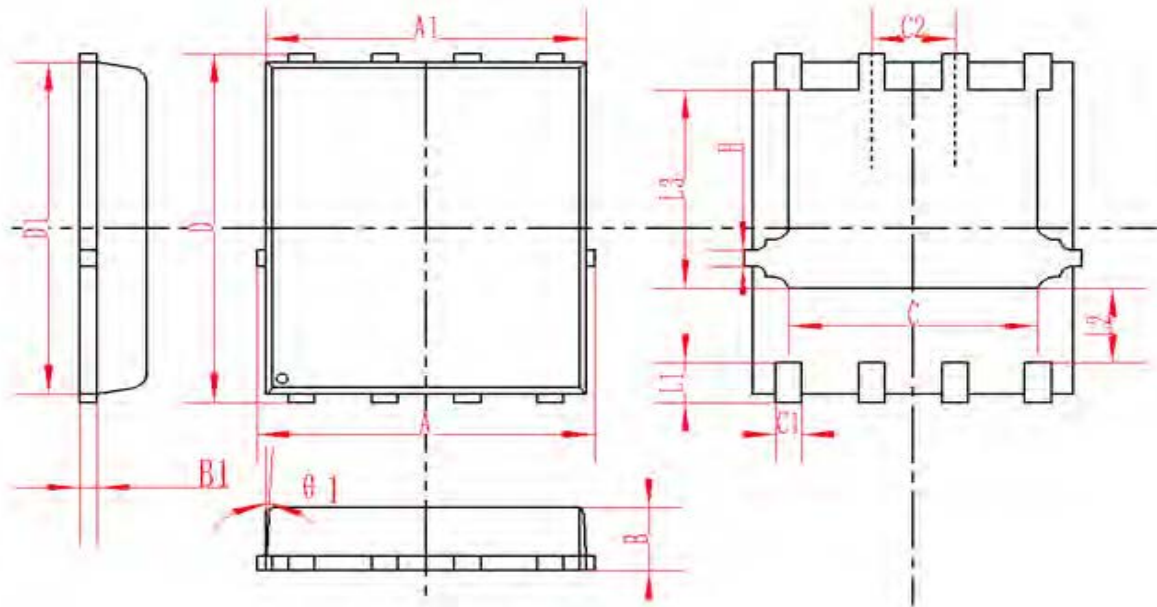


Fig.8 EAS Waveform



### DFN5X6-8L(TDFN-8(5.2x5.9))Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	5.3	5.5	5.7	0.208	0.216	0.224
A1	5.1	5.2	5.3	0.2	0.204	0.209
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.85	6.05	6.25	0.23	0.238	0.246
B	0.85	0.95	1.05	0.033	0.037	0.041
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
$\theta 1$	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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