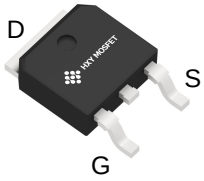
STD2LN60K3

Silicon N-Channel Power MOSFET

Description

The STD2LN60K3 can be used in various power swithching circuit for system miniaturization and higher efficiency.The package form is TO-252-2L, which accords with the RoHS standard.



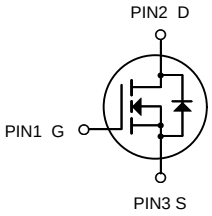
TO-252-2L (DPAK)

General Features

V_{DS} = 650V,I_D = 2A
$R_{DS(ON)}$ < 5Ω@ V_{GS}=10V

Application

- Power switch circuit of adaptor and charger.



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
STD2LN60K3	TO-252-2L(DPAK)	HXY MOSFET	2500

Absolute Maximum Ratings @T_j = 25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	650	V
VGS	Gate-Source Voltage	±30	V
I_D@T_C=25°C	Drain Current, V_{GS} @ 10V	2	A
I_D@T_C=100°C	Drain Current, V_{GS} @ 10V	1.3	A
IDM	Pulsed Drain Current	8	A
P_D@T_C=25°C	Total Power Dissipation	35	W
E_{AS}	Single Pulse Avalanche Energy	50	mJ
TSTG	Storage Temperature Range	-45 to 125	°C
T_J	Operating Junction Temperature Range	-45 to 125	°C

Electrical Characteristics（Tc= 25°C℃ unless otherwise specified）：

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	650	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference 25°C	--	0.7	--	V/°C
I_{DSS}	Drain to Source Leakage Current	V_{DS} =650V, V_{GS}= 0V, T_a = 25°C	--	--	1	μA
		V_{DS} =520V, V_{GS}= 0V, T_a = 125°C	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=1A	--	4.2	5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D =1A	--	1.8	--	S
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	335	--	pF
C_{oss}	Output Capacitance		--	33	--	
C_{rss}	Reverse Transfer Capacitance		--	3	--	
$t_{d(ON)}$	Turn-on Delay Time		--	11	--	
tr	Rise Time	I_D =2A V_{DD} = 325V R_G =10Ω	--	13	--	ns
$t_{d(OFF)}$	Turn-Off Delay Time		--	29	--	
t_f	Fall Time		--	12	--	
Q_g	Total Gate Charge	I_D =2A V_{DD} =520V V_{GS} = 10V	--	9.5	--	nC
Q_{gs}	Gate to Source Charge		--	1.5	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	4.9	--	
I_S	Continuous Source Current (Body Diode)		--	--	2	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	8	A
V_{SD}	Diode Forward Voltage	I_S=2.0A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=2.0A,T_j = 25°C dI$_F$/dt=100A/us, V_{GS}=0V	--	187	--	ns
Qrr	Reverse Recovery Charge		--	610	--	nC
I_{RRM}	Reverse Recovery Current		--	6.6	--	A

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	3.57	°C/W
$R_{\theta JA}$	Junction-to-Ambient	100	°C/W

[a1]：Repetitive rating; pulse width limited by maximum junction temperature

[a2]：L=10mH, I_D=3.1A, Start T_J=25°C

[a3]：I_{SD} =2A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25°C

Characteristics Curve：

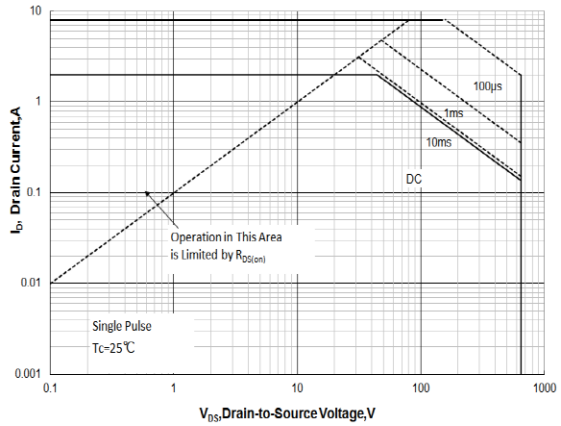


Figure 1 Maximum Forward Bias Safe Operating Area

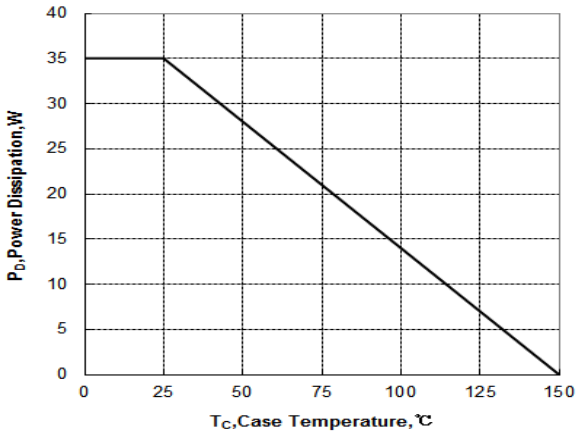


Figure 2 Maximum Power dissipation vs Case Temperature

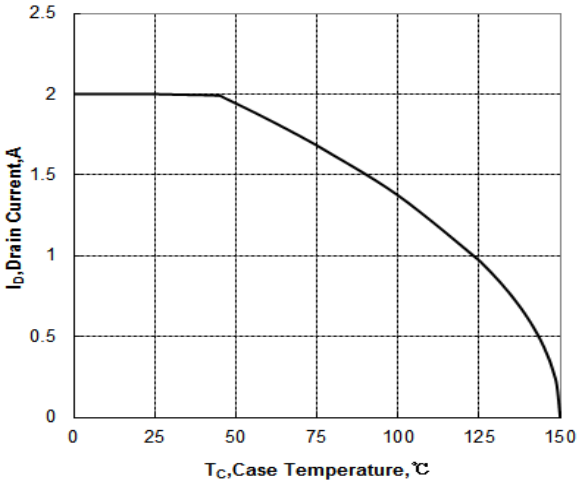


Figure 3. Maximum Continuous Drain Current vs Case Temperature

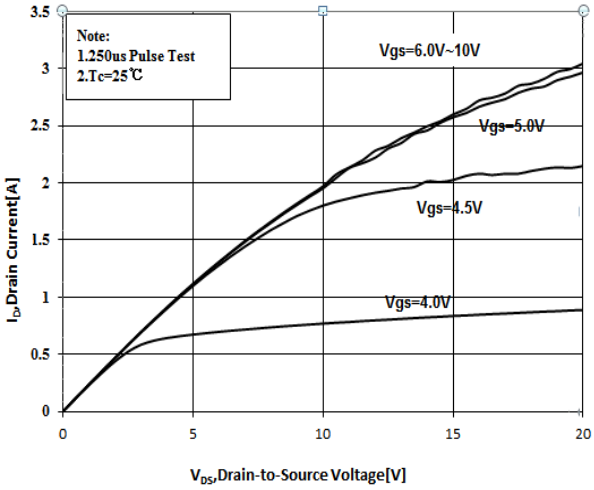


Figure 4. Typical Output Characteristics

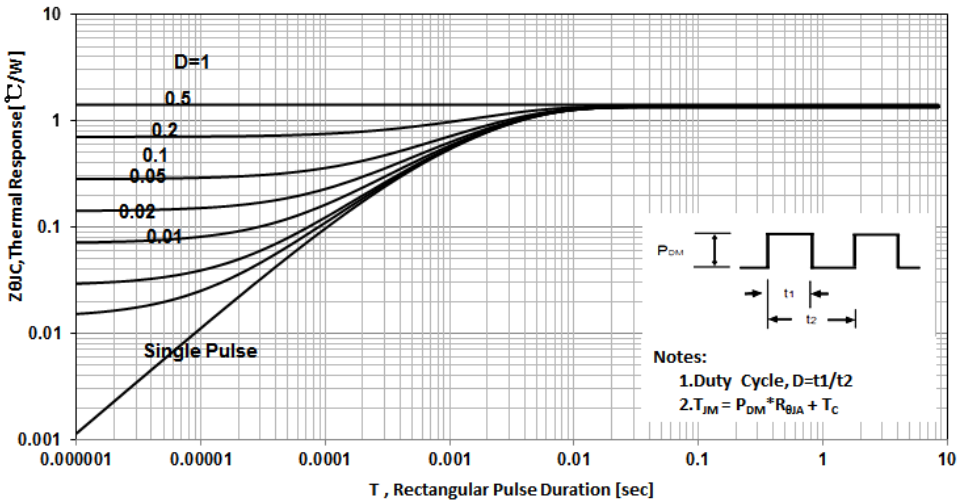


Figure 5. Maximum Effective Thermal Impedance , Junction to Case

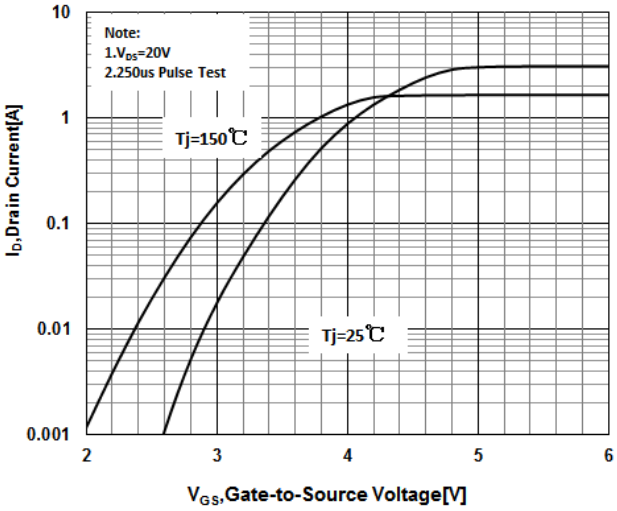


Figure 6. Typical Transfer Characteristics

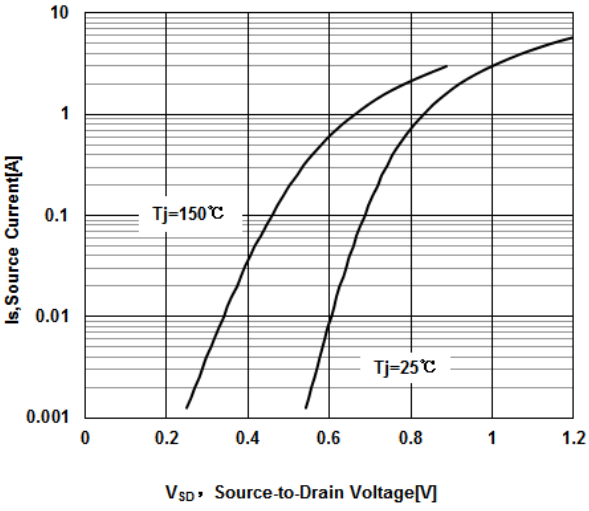


Figure 7. Typical Body Diode Transfer Characteristics

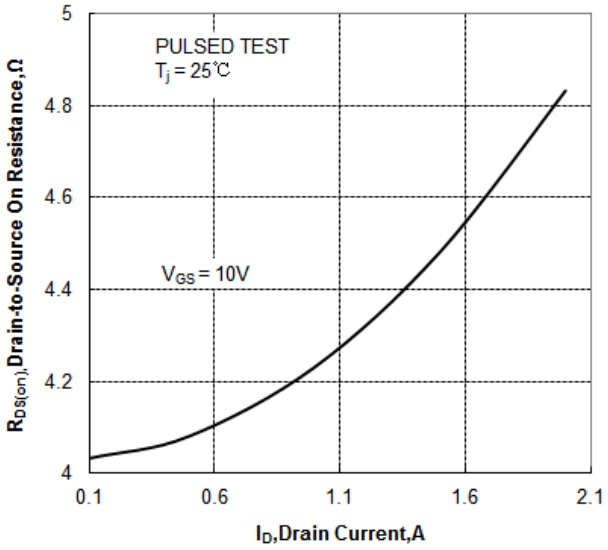


Figure 8. Typical Drain to Source ON Resistance vs Drain Current

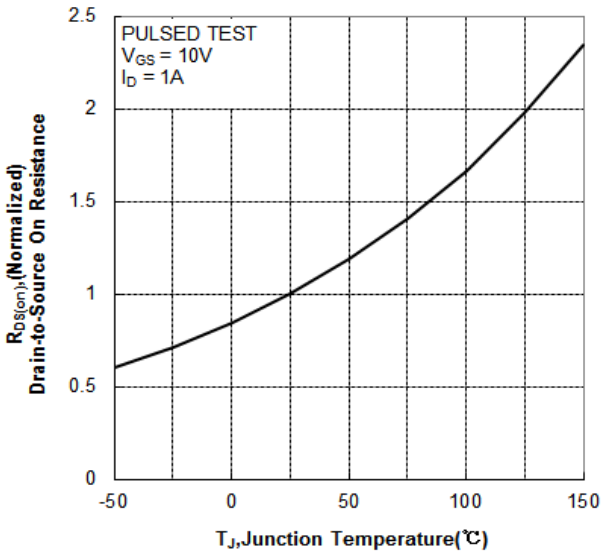


Figure 9. Typical Drian to Source on Resistance vs Junction Temperature

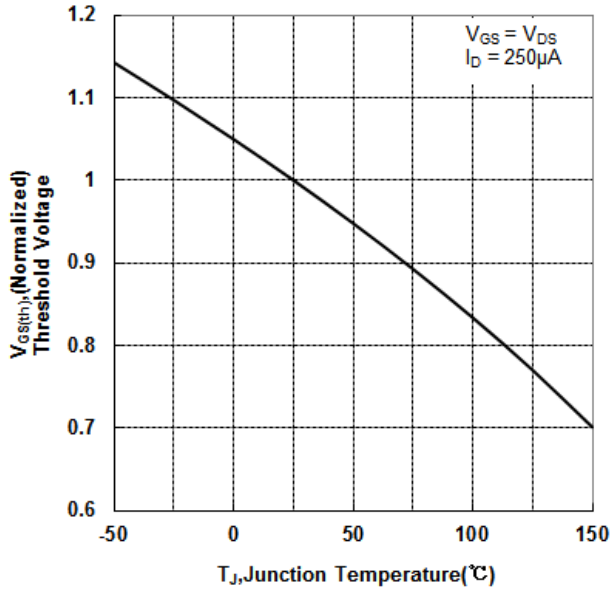


Figure 10. Typical Theshold Voltage
vs Junction Temperature

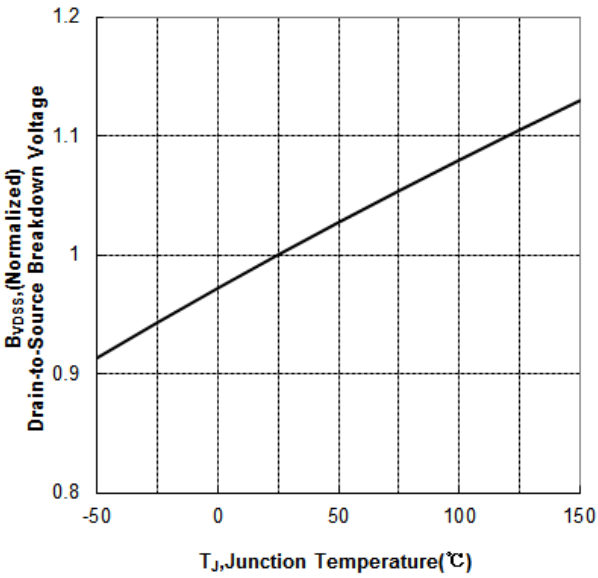


Figure 11. Typical Breakdown Voltage
vs Junction Temperature

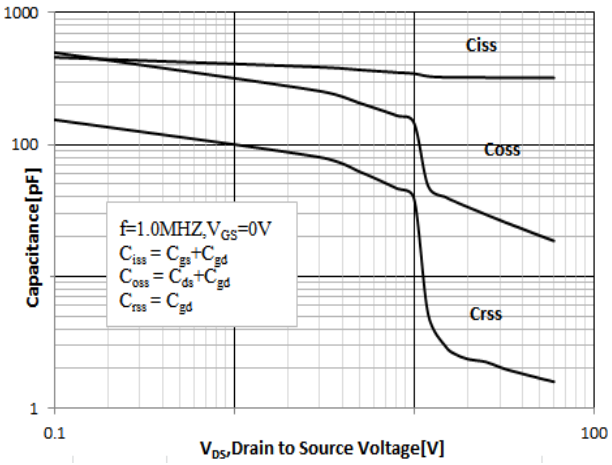


Figure 12 Typical Capacitance
vs Drain to Source Voltage

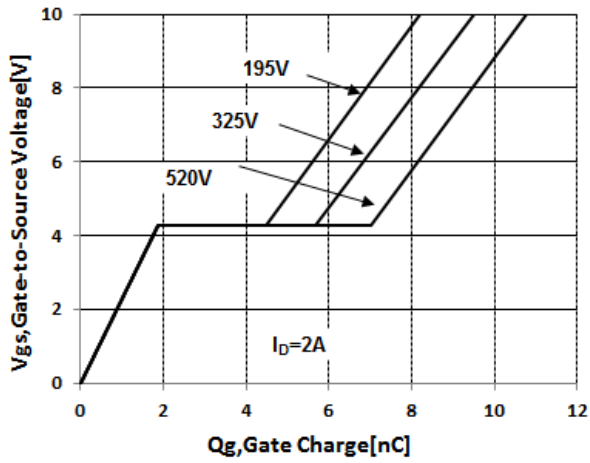


Figure 13 Typical Gate Charge
vs Gate to Source Voltage

Test Circuit and Waveform

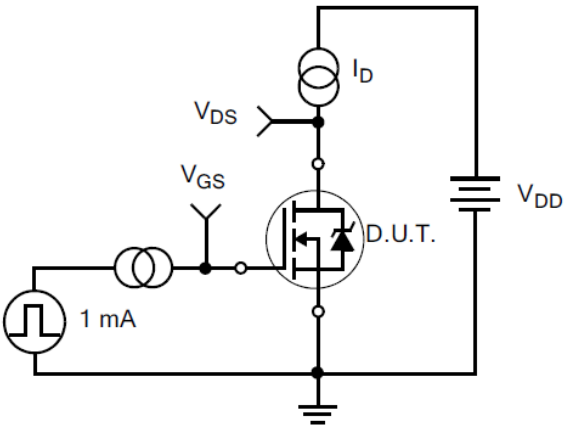


Figure 14. Gate Charge Test Circuit

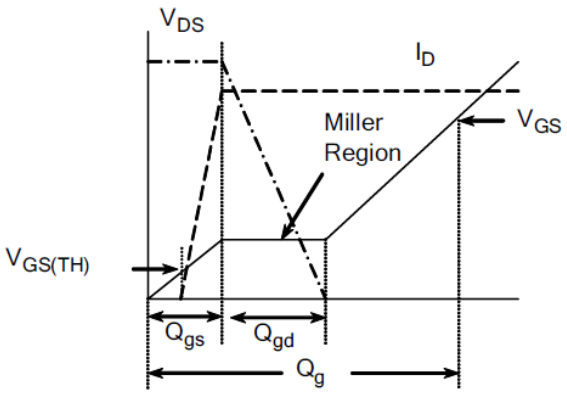


Figure 15. Gate Charge Waveforms

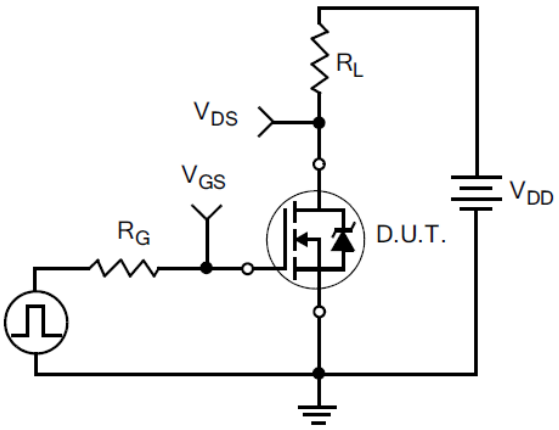


Figure 16. Resistive Switching Test Circuit

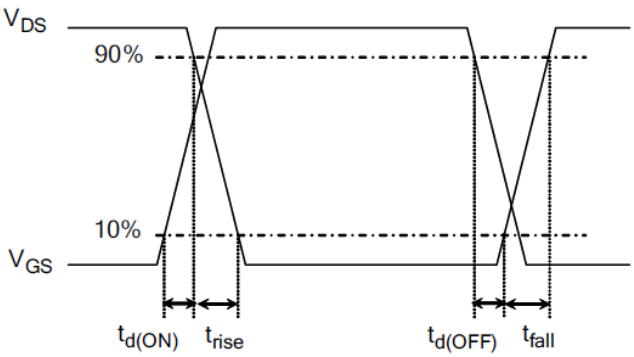


Figure 17. Resistive Switching Waveforms

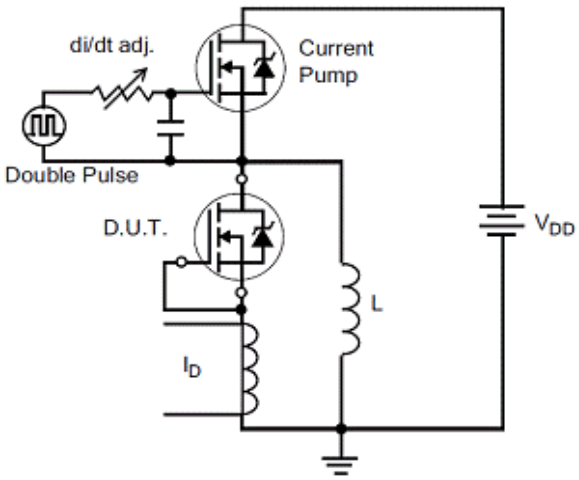


Figure 18. Diode Reverse Recovery Test Circuit

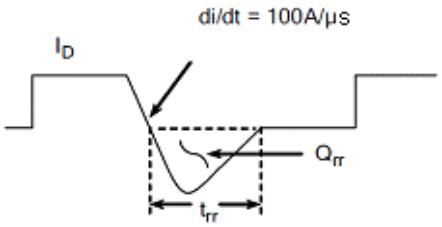


Figure 19. Diode Reverse Recovery Waveform

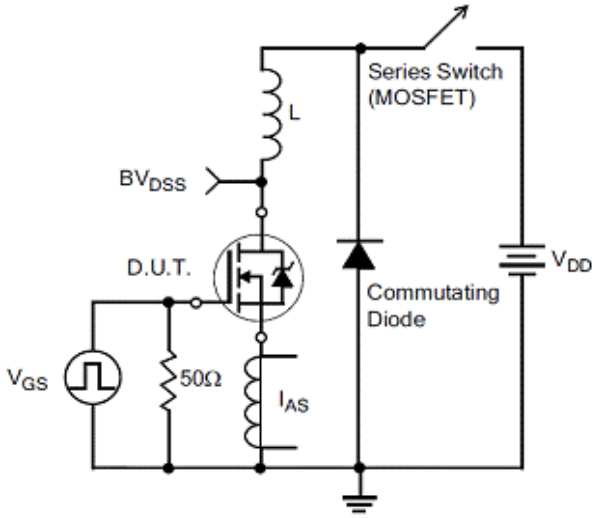


Figure20.Unclamped Inductive Switching Test Circuit

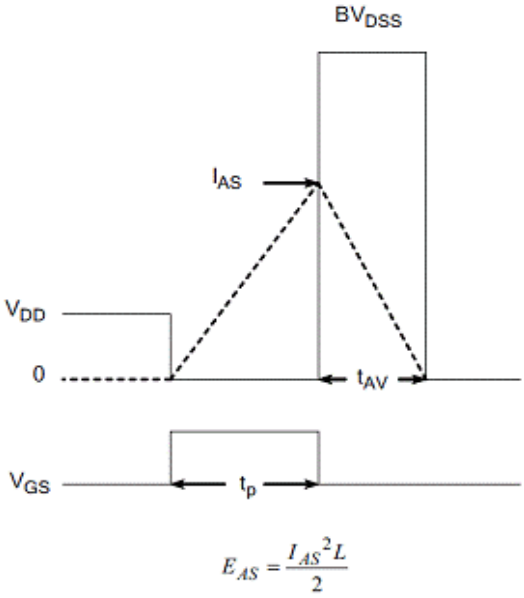
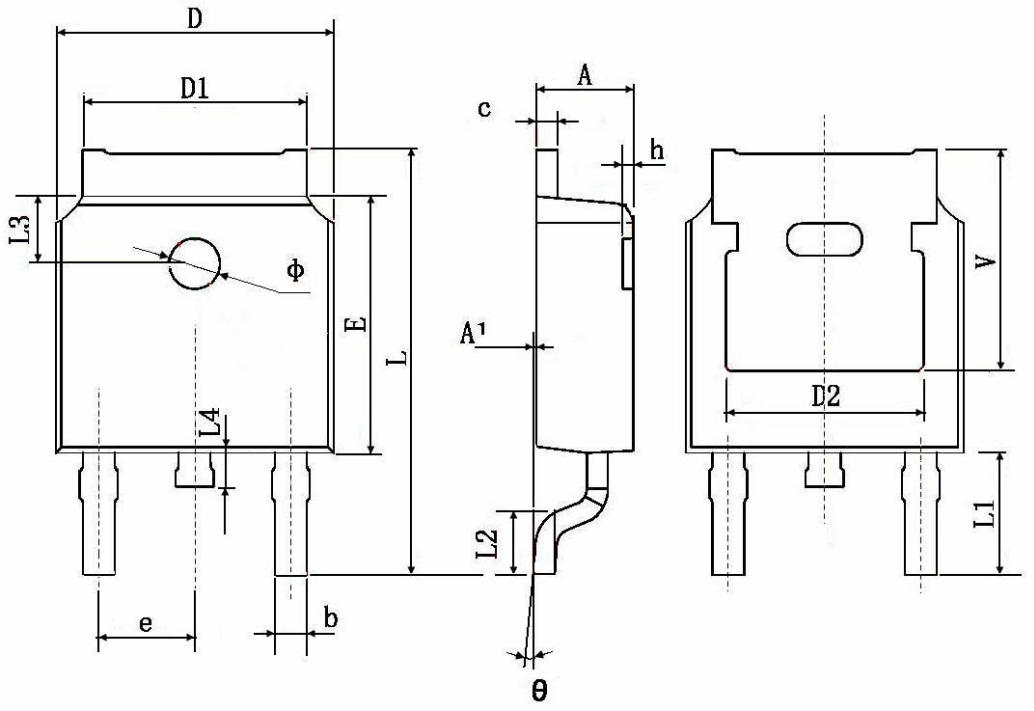


Figure21.Unclamped Inductive Switching Waveform

TO-252-2L(DPAK) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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