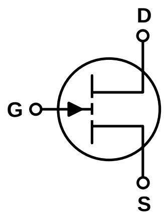
INN100EBD018DAD-C

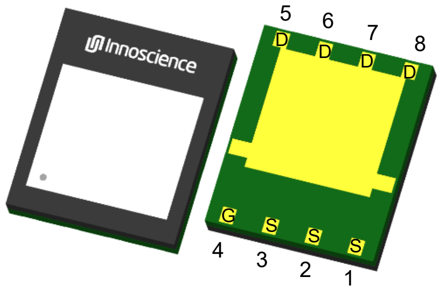
1. General Description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in En-FCLGA with 5.0 mm x 6.0 mm package size.



2. Features

- GaN-on-Silicon E-mode HEMT technology
- Industry application
- Very low gate charge
- Ultra-low on resistance
- Very small footprint



Top View Bottom View

3. Applications

- High frequency DC-DC converter
- High density DC/DC power module
- Synchronous rectification
- Motor driver
- Solar system MPPT

4. Key Performance Parameters

Table 1 Key performance parameters at T_J = 25 ˚C

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),typ}$ @ V_{GS} = 5 V	1.1	mΩ
$R_{DS(on),max}$ @ V_{GS} = 5 V	1.5	mΩ
$Q_{G,typ}$ @ V_{DS} = 50V	19	nC
$I_{DS,Pulse}$ (T_J = 25 ˚C)	980	A
Q_{OSS} @ V_{DS} = 50 V	100	nC

5. Pin Information

Table 2 Pin information

PIN	Pin Description	Pin Function
1,2,3	Source	Power Source
5-8	Drain	Power Drain
4	Gate	Driver Gate

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100EBD018DAD-C	En-FCLGA 5.0 x 6.0	J50

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6. Maximum Ratings

at T_J = 25 ˚C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage [1] (V_{GS} = 0 V, 1h total time, T_A = T_{JMAX})	120	V
I_D	Continuous current (V_{GS} = 5 V, T_C = 25 ˚C， $R_{θJC}$ = 0.2 ˚C/W)	474	A
	Continuous current (V_{GS} = 5 V, T_C = 100 ˚C， $R_{θJC}$ = 0.2 ˚C/W)	300	A
	Continuous current (V_{GS} = 5 V, T_A = 25 ˚C， $R_{θJA}$ = 38.1 ˚C/W)	33	A
	Pulsed (V_{GS} = 5 V, T_J = 25 ˚C, T_{Pulse} = 100 µs)	980	A
	Pulsed (V_{GS} = 5 V, T_J = 150 ˚C, T_{Pulse} = 100 µs)	760	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
$V_{GS(tr)}$	Gate-to-Source Voltage [1] (V_{DS} = 0 V, 168h total time, T_A = T_{JMAX})	6.5	V
P_{tot}	Power dissipation (V_{GS} = 5 V, T_C =25˚C， $R_{θJC}$ = 0.2 ˚C/W)	658	W
	Power dissipation (V_{GS} = 5 V, T_A =25˚C， $R_{θJA}$ = 38.1 ˚C/W)	3.2	W
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-55 to 150	˚C

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.2	˚C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	2.2	˚C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	38.1	˚C/W	-
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note:

2. $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

8. Electric Characteristics

at T_J = 25 °C unless otherwise specified.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{DSS}	Drain Source Leakage	-	2.5	200	µA	V_{GS} = 0 V, V_{DS} =100 V
	Drain Source Leakage (T_J = 125 ˚C)	-	500	-	µA	V_{GS} = 0 V, V_{DS} =100 V
I_{GSS}	Gate-to-Source Forward Leakage	-	2	200	µA	V_{GS} = 6 V
	Gate-to-Source Forward Leakage (T_J = 125 ˚C)	-	50	-	µA	V_{GS} = 6 V
	Gate-to-Source Reverse Leakage	-	0.1	200	µA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage [3]	0.9	1.1	2.1	V	V_{DS} = V_{GS}, I_D = 19 mA
$R_{DS(on)}$	Drain-Source On-state Resistance [3]	-	1.1	1.5	mΩ	V_{GS} = 5 V, I_D = 2.5 A
V_{SD}	Source-Drain Forward Voltage	-	1.8	-	V	I_S = 50 A, V_{GS} = 0 V

Note:

3. $V_{GS(TH)}$ and $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics [4]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	2350	-	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{OSS}	Output Capacitance	-	1010	-		V_{GS} = 0 V, V_{DS} = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	14	-		V_{GS} = 0 V, V_{DS} = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	1415	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	2000	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
R_G	Gate resistance	-	0.73	-	Ω	f= 5 MHz, open drain
Q_G	Total Gate Charge	-	19	-	nC	V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 50 A
Q_{GS}	Gate to Source Charge	-	4.2	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D = 50 A
Q_{GD}	Gate to Drain Charge	-	3	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D = 50 A
V_{Plat}	Gate Plateau Voltage	-	1.9	-	V	I_D = 50 A, V_{DS} = 50 V, V_{GS} = 0 V to 5 V
$Q_{G(TH)}$	Gate Charge at Threshold	-	2.4	-	nC	V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D = 50 A
Q_{OSS}	Output Charge	-	100	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
Q_{RR}	Reverse recovery charge	-	0	-		V_{DS} = 50 V, I_S = 50 A

Note:

4. Guaranteed by design.

9. Electric Characteristics Diagrams

at T_J = 25 °C, unless specified otherwise

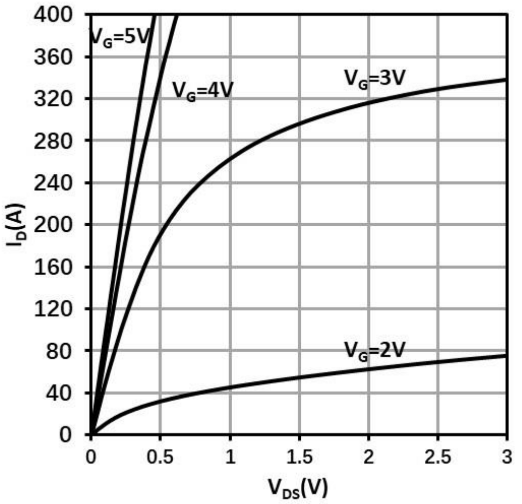
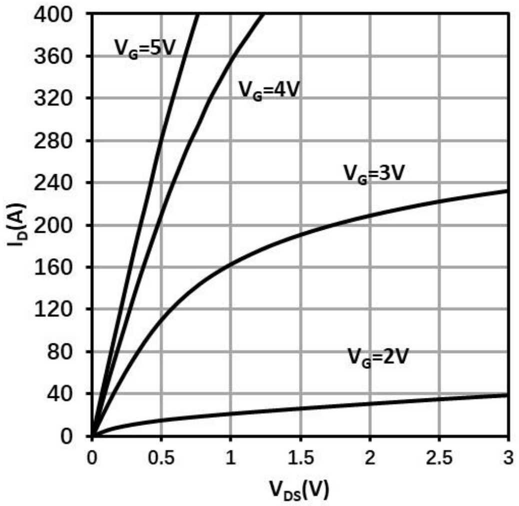
Fig. 1 Typ. Output Characteristics (T_J = 25 ˚C)	Fig. 2 Typ. Output Characteristics (T_J = 125 ˚C)
	

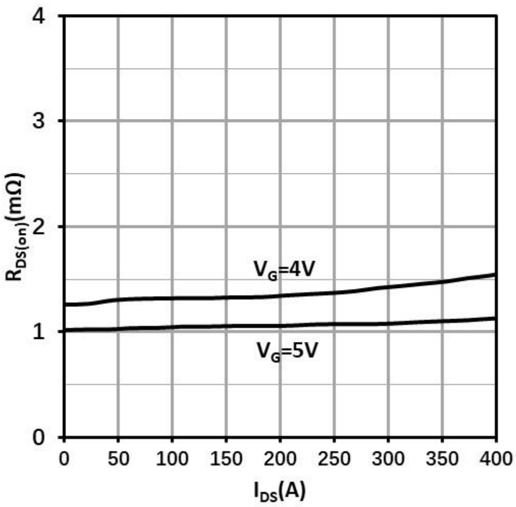
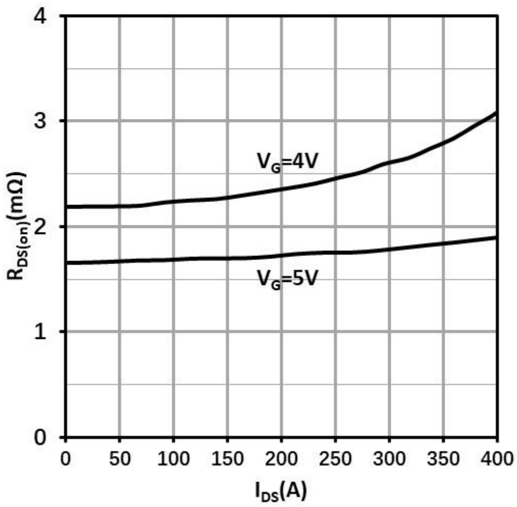
Fig. 3 Typ. Drain On-state Resistance (T_J = 25 ˚C)	Fig. 4 Typ. Drain On-state Resistance (T_J = 125 ˚C)
	

Fig. 5 Normalized On-State Resistance vs. Temp.

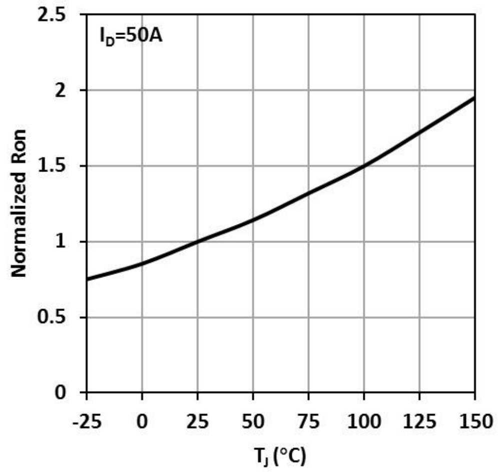


Fig. 6 Typ. Transfer Characteristics

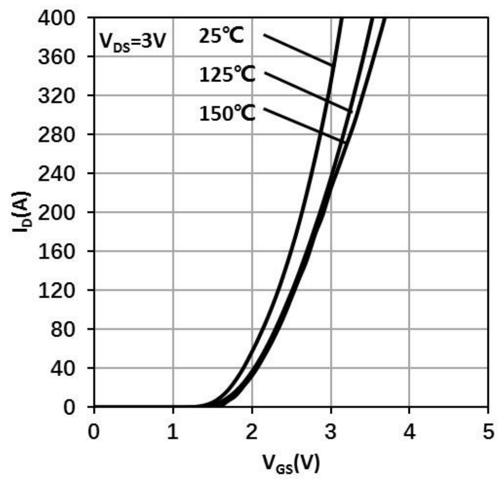


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, T_J = 25 °C)

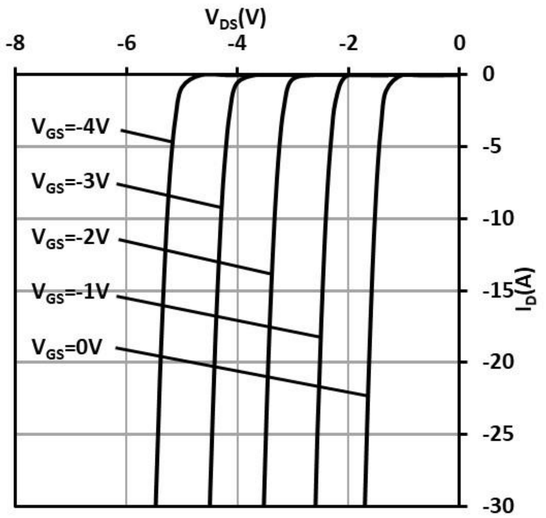


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$, T_J = 25 °C)

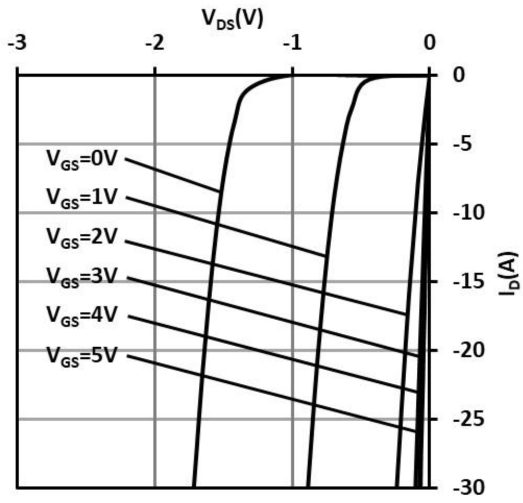


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \le 0$, T_J = 125 ˚C)

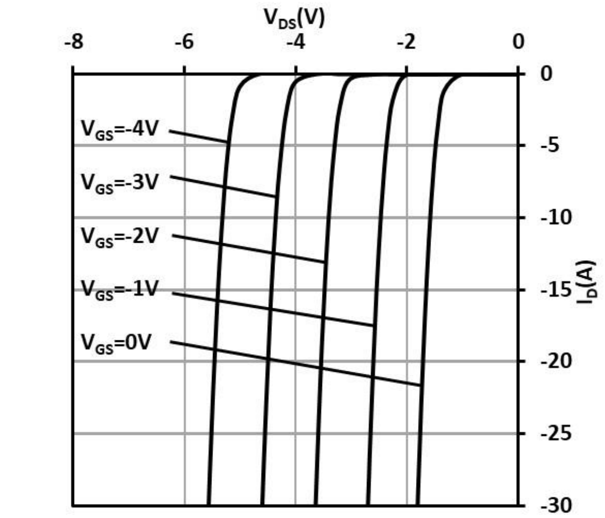


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \ge 0$, T_J = 125 ˚C)

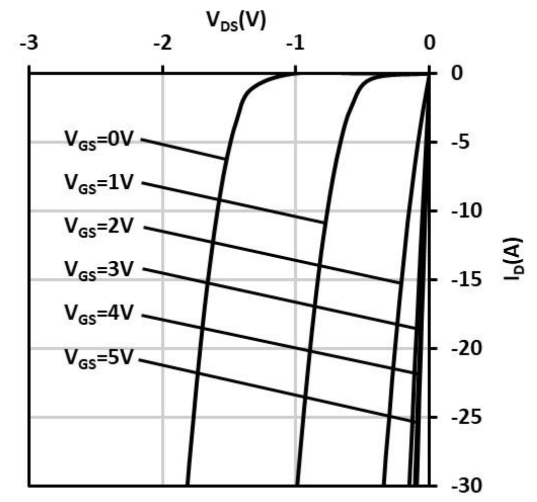


Fig. 11 Typ. Capacitances Characteristics

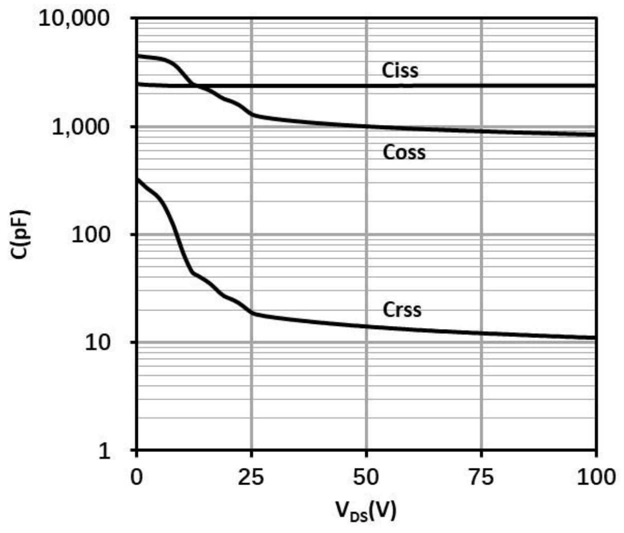


Fig. 12 Typ. Gate Charge

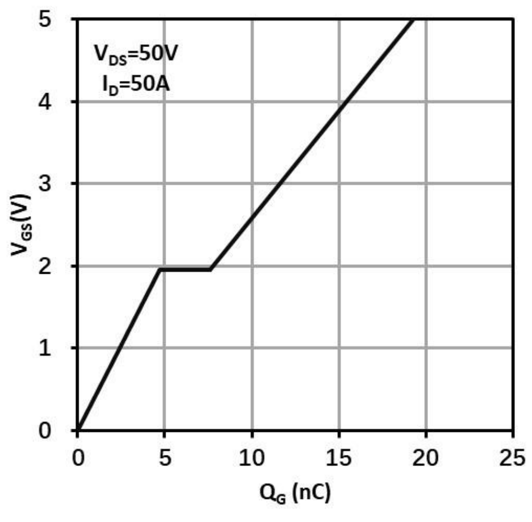


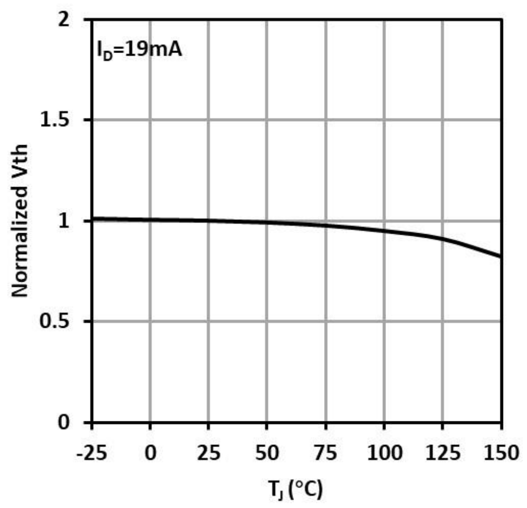
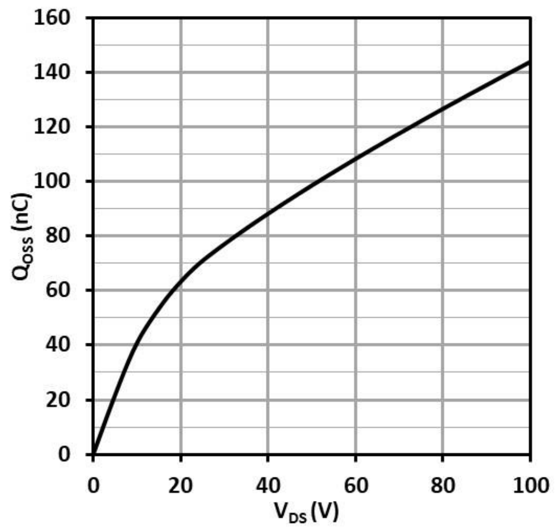
Fig. 13 Normalized Threshold Voltage vs. Temp.	Fig. 14 Typ. Output Charge
	

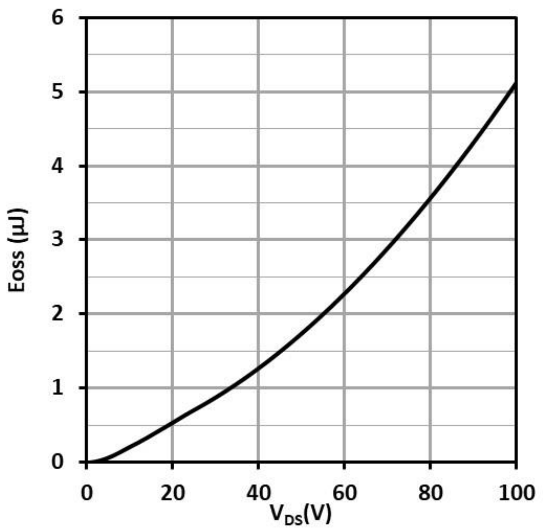
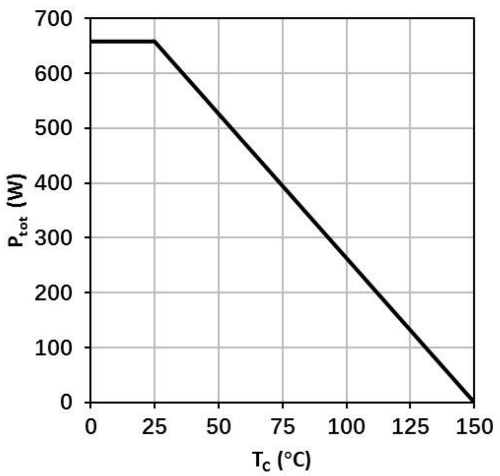
Fig. 15 Typ. Output Capacitance Stored Energy	Fig. 16 Power Dissipation $P_{tot} = f(T_C)$, $R_{\theta JC}$ = 0.2˚C/W
	

Fig. 17 Power Dissipation Ptot = f(T_A), $R_{\theta JA}$ =38.1˚C/W

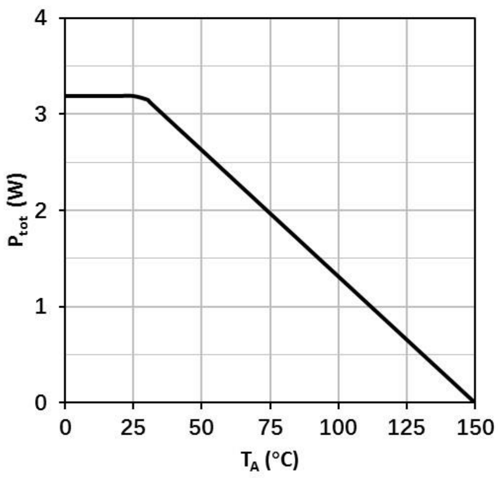


Fig. 18 Typ. Gate-to-Source Leakage Characteristics
I_G = f(V_{GS}); Drain Open

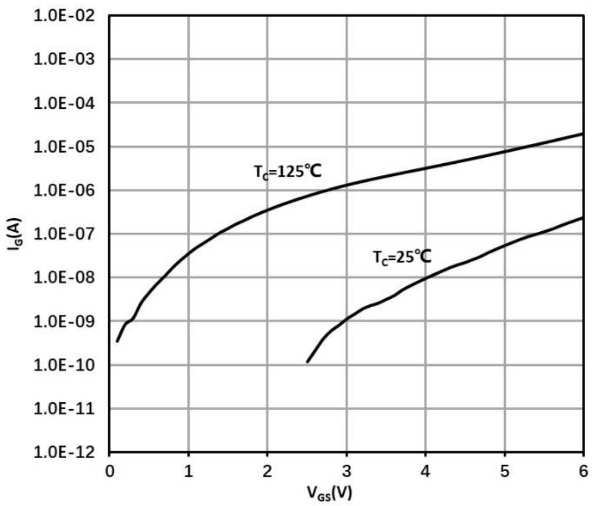


Fig. 19 Typ. Drain-source Leakage Characteristics
I_{DSS} = f(V_{DS}); V_{GS} = 0 V

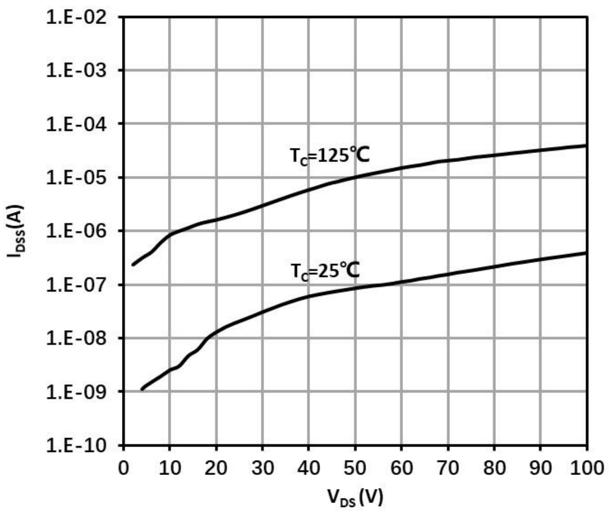


Fig. 20 Safe Operating Area
I_D = f(V_{DS}); T_C = 25 ˚C; Single Pulse; Parameter: t_p

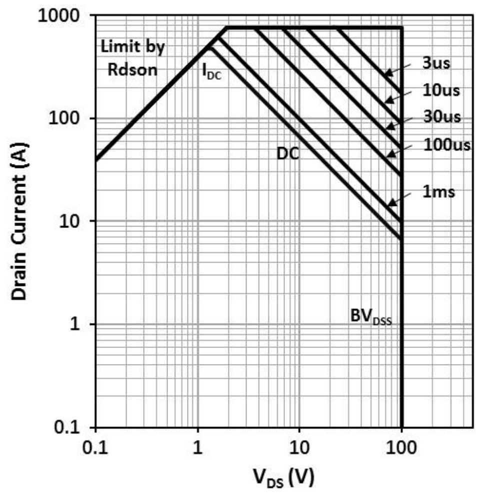
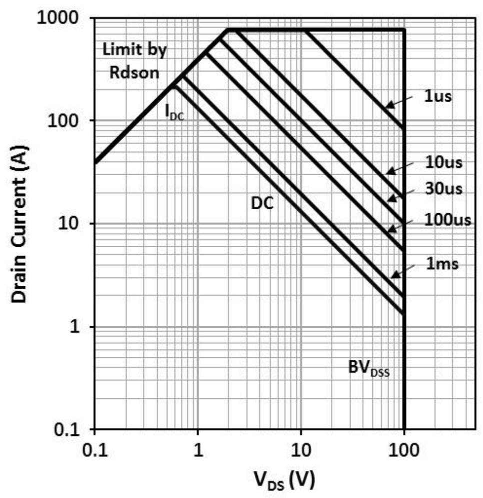
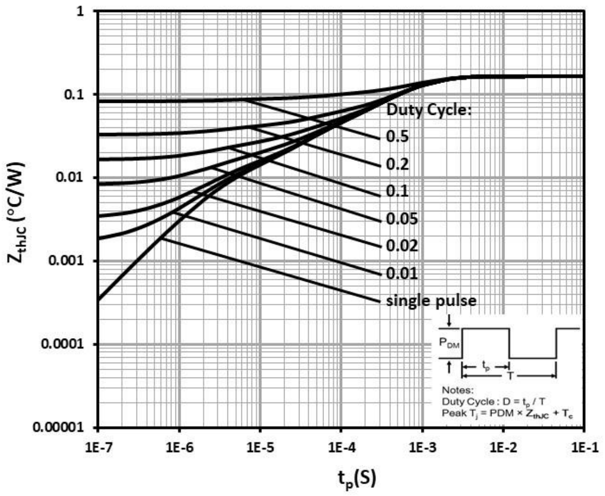
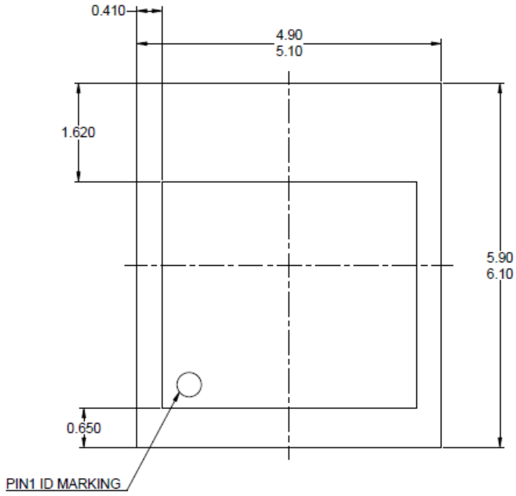


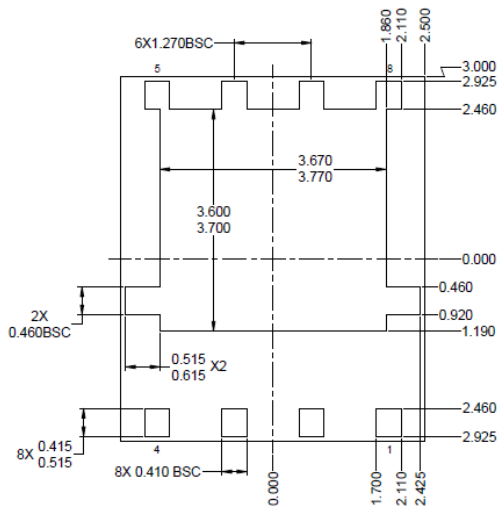
Fig. 21 Safe Operating Area $I_D = f(V_{DS})$; T_C = 125 ˚C; Single Pulse; Parameter: t_p	Fig. 22 Max. Transient Thermal Impedance $Z_{thJC} = f(t_p)$; Parameter: $D=t_p/T$
	

10. Package Outlines

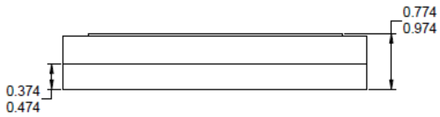
Package Reference



TOP VIEW



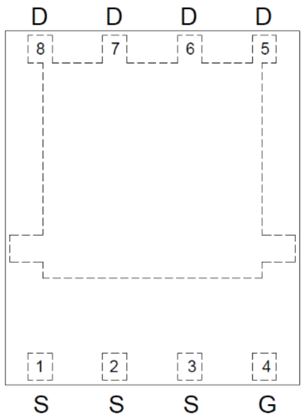
BOTTOM VIEW



SIDE VIEW

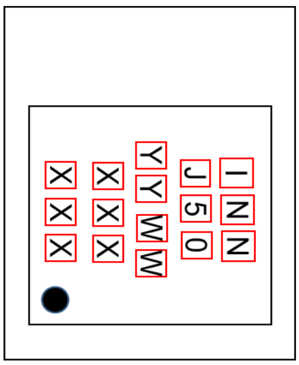
NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Pin Configuration



TOP VIEW

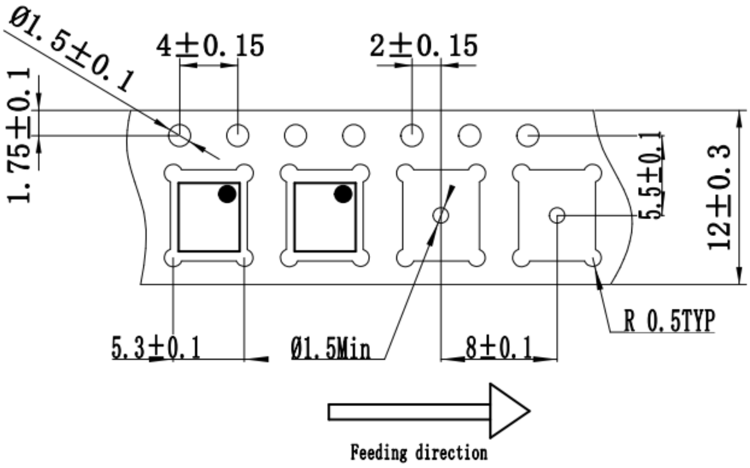
Marking Reference

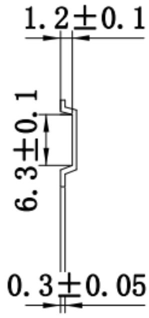


TOP VIEW

Row	Description	Example
Row1	Company Name	INN
Row2	Product Code	XXX
Row3	Date Code	YYWW
Row4	Lot Code	XXX
Row5		XXX

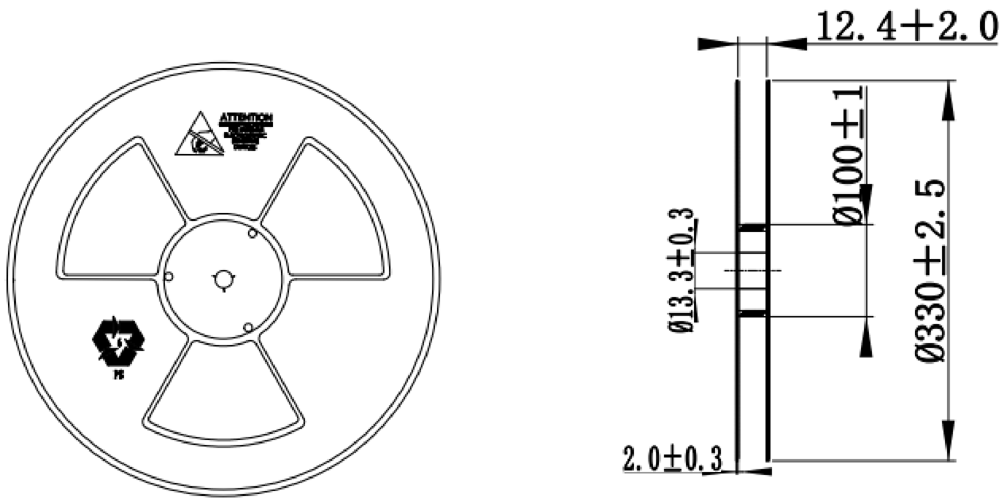
11. Reel Information





Unit: mm

Notes:
(1)The cumulative error of any 10 sprocket holes shall not exceed ± 0.20mm;
(2)The material thickness shall be measured based on the edge of the carrier tape;
(3)The unspecified tolerance is ± 0.1mm, and R<0.3mm is not specified;
(4)The unmarked demolding slope is 5 ° ;
(5)Surface Resistivity: 1*10 e 5 Ω/Δ ~ 1*11 e11

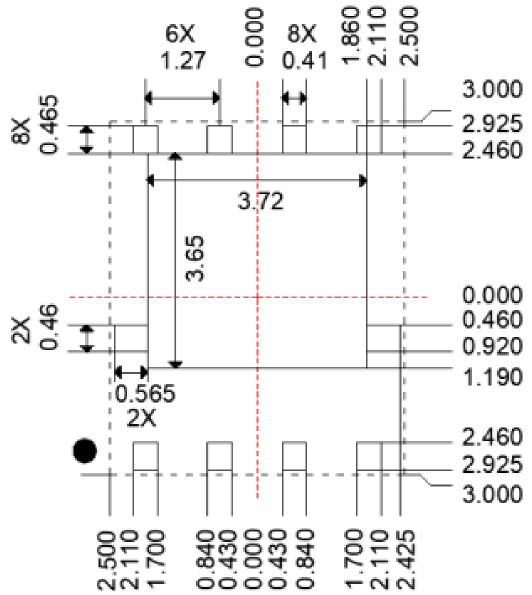


Notes:
1、The surface of the product should be smooth, clean, and free of injection molding defects, and there should be no significant burrs;
2、Material surface resistance:1*10e5Ω/Δ~1*10e10Ω/Δ;
3、No tolerance marked: ±0.3mm;

Unit: mm

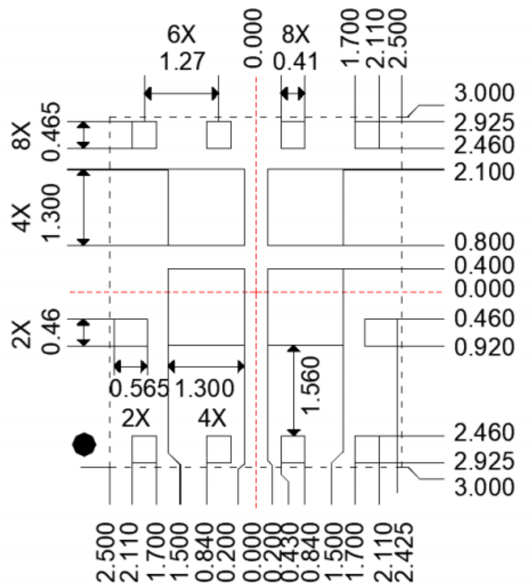
12. Land Pattern

Recommended Land Pattern



Unit: mm

Recommended Stencil Drawing



Unit: mm

13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-08-27	1.0 version release

Important Notice