TC7S00 Series

Single 2-Input Positive-NAND Gate

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General Description

The TC7S00 is a single 2-input NAND gate.The device is designed for 1.65 V to 5.5 V for V_{CC} operation, it can be driven from either 3.3 V or 5 Vdevices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 Venvironments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise andfall times.

The TC7S00 performs the Boolean function $Y = A \overline{x\ B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad Vcc operating range.

The TC7S00 is available in SOT23-5 and SOT353 packages.

Features

- Wide Supply Voltage Range : 1.65 V to 5.5 V
- Max. T_{PD} of 3.8 ns at V_{CC} = 3.3 V
- Low Power Consumption, 10 μA (Max. I_{CC})
- ±24 mA Output Drive at V_{CC} = 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Operating temperature Range : -40°C to 125°C
- Available Package : SOT23-5 and SOT353

Applications

- Active Noise Cancellation (ANC)
- Blood Pressure Monitor
- Embedded PC
- Solid State Drive (SSD) : Client and Enterprise
- TV : LCD/Digital and High-Definition (HDTV)
- Tablet : Enterprise
- Video Analytics : Server
- Wireless Headset, Keyboard, and Mouse
- Power Supply : Telecom/Server AC/DC Controller

Logic Diagram

Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
TC7S00F-TP	SOT23-5	Tape and Reel,3000
TC7S00FU-TP	SOT353	Tape and Reel,3000

TC7S00 Series

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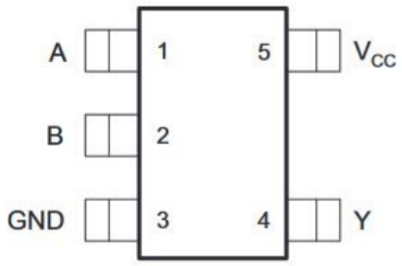
Pin Configuratio



SOT23-5 and SOT353 (Top View)

Function Table(each gate)

INPUTs		OUTPUT
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level; L = LOW voltage level;

Pin Description

Pin		Function
Num	**Name**	
1	A	Data Input
2	B	Data Input
3	GND	Ground
4	Y	Data Output
5	V_{CC}	Supply Power Input

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	-0.5 to 6.5	V
Input Voltage	V_I	-0.5 to 6.5	V
Voltage range applied to any output in the high-impedance or power-off state(2)	V_O	-0.5 to 6.5	V
Voltage range applied to any output in the high or low state(2)(3)	V_O	-0.5 to V_{CC}+0.5	V
Input clamp current, V_I < 0	I_{IK}	-50	mA
Output clamp current, V_O < 0	I_{OK}	-50	mA
Continuous output current	I_O	±50	mA
Storage temperature range	T_{STG}	-65 to 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001(4)	ESD_{HBM}	±2000	V
ESD CDM, JESD22-C101(5)	ESD_{CDM}	±1000	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O				V_{CC}	V
High-level input voltage	V_{IH}	V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}			V
		V_{CC} = 2.3 V to 2.7 V	1.7			
		V_{CC} = 3 V to 3.6 V	2			
		V_{CC} = 4.5 V to 5.5 V	0.7 x V_{CC}			
Low-level input voltage	V_{IL}	V_{CC} = 1.65 V to 1.95 V			0.35 x V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7	
		V_{CC} = 3 V to 3.6 V			0.8	
		V_{CC} = 4.5 V to 5.5 V			0.3 x V_{CC}	
High-level output current	I_{OH}	V_{CC} = 1.65 V			-4	mA
		V_{CC} = 2.3 V			-8	
		V_{CC} = 3 V			-16	
		V_{CC} = 3 V			-24	
		V_{CC} = 4.5 V			-32	
Low-level output current	I_{OL}	V_{CC} = 1.65 V			4	mA
		V_{CC} = 2.3 V			8	
		V_{CC} = 3 V			16	
		V_{CC} = 3 V			24	
		V_{CC} = 4.5 V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2 V			20	ns/V
		V_{CC} = 3.3 V ±0.3 V			10	
		V_{CC} = 5 V ±0.5 V			5	
Operating temperature	T_A		-40		125	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	V_{CC} = 1.65~5.5 V, I_{OH} = -100 μA	V_{CC}-0.1			V
		V_{CC} = 1.65 V, I_{OH} = -4 mA	1.2			
		V_{CC} = 2.3 V, I_{OH} = -8 mA	1.9			
		V_{CC} = 3 V, I_{OH} = -16 mA	2.4			
		V_{CC} = 3 V, I_{OH} = -24 mA	2.3			
		V_{CC} = 4.5 V, I_{OH} = -32 mA	3.8			
Low-level output voltage	V_{OL}	V_{CC} = 1.65~5.5 V, I_{OL} = 100 μA			0.1	V
		V_{CC} = 1.65 V, I_{OL} = 4 mA			0.45	
		V_{CC} = 2.3 V, I_{OL} = 8 mA			0.3	
		V_{CC} = 3 V, I_{OL} = 16 mA			0.4	
		V_{CC} = 3 V, I_{OL} = 24 mA			0.55	
		V_{CC} = 4.5 V, I_{OL} = 32 mA			0.55	
Input leakage current	I_L	V_{IN} = 5.5 V or GND, V_{CC} = 0~5.5 V			±5	μA
Power off leakage current	I_{OFF}	V_{IN} or GND, V_{CC} = 0~5.5 V			±10	μA
Quiescent supply current	I_Q	V_{IN} = V_{CC} or GND, I_{OUT} = 0, V_{CC} = 1.65~5.5 V			10	μA
Additional quiescent supply current per input pin	$\triangle I_Q$	V_{CC} = 3~5.5 V, one input at V_{CC}-0.6 V, other input at V_{CC} or GND			500	μA

Switching Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Propagation delay from input (A or B) to output (Y)	T_{PD}	V_{CC} = 1.8 V ±0.15 V	C_L = 15 pF, R_L = 1 MΩ	2.2		7.2	nS
		V_{CC} = 2.5 V ±0.2 V		0.9		4.4	nS
		V_{CC} = 3.3 V ±0.3 V		0.8		3.8	nS
		V_{CC} = 5 V ±0.5 V		0.8		3.4	nS

Typical Performance Characteristics

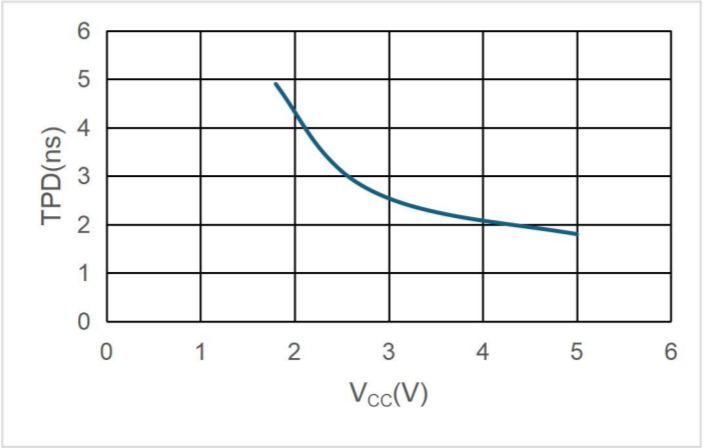
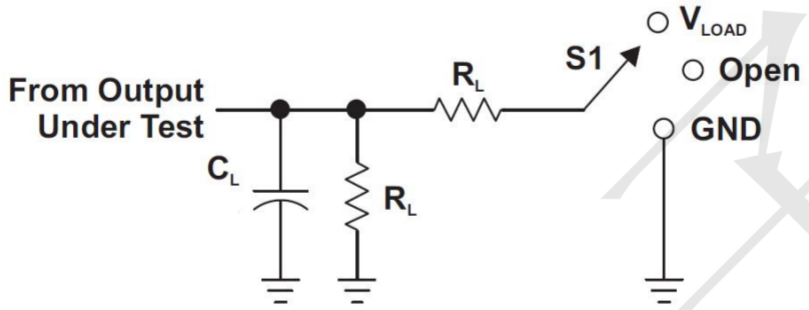


Figure 1.T_{PD} across V_{CC} at 25°C

Parameter Measurement Information



LOAD CIRCUIT

V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
1.8 V ±0.15 V	V_{CC}	≦2 ns	$V_{CC}/2$	15 pF	1 MΩ
2.5 V ±0.2 V	V_{CC}	≦2 ns	$V_{CC}/2$	15 pF	1 MΩ
3.3 V ±0.3 V	3 V	≦2.5 ns	1.5 V	15 pF	1 MΩ
5 V ±0.5 V	V_{CC}	≦2.5 ns	$V_{CC}/2$	15 pF	1 MΩ

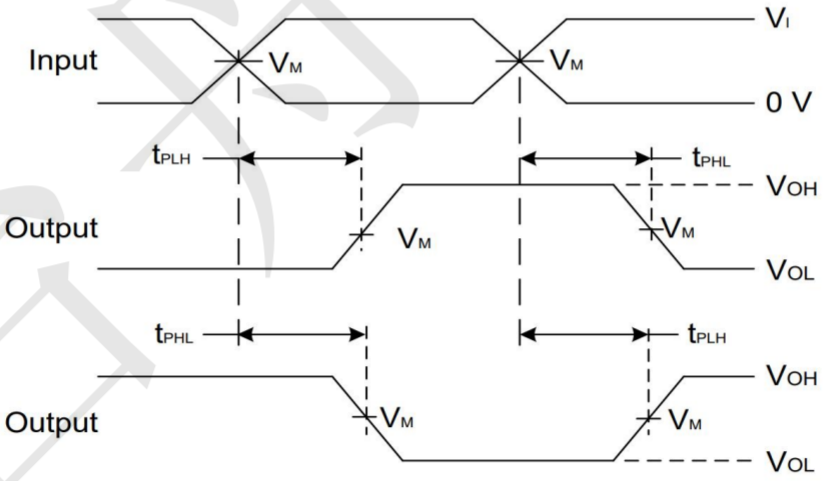


Figure 2. Voltage waveform propagation delay times,

Inverting and non-inverting outputs

Notes:

(1) C_L includes probe and jig capacitance

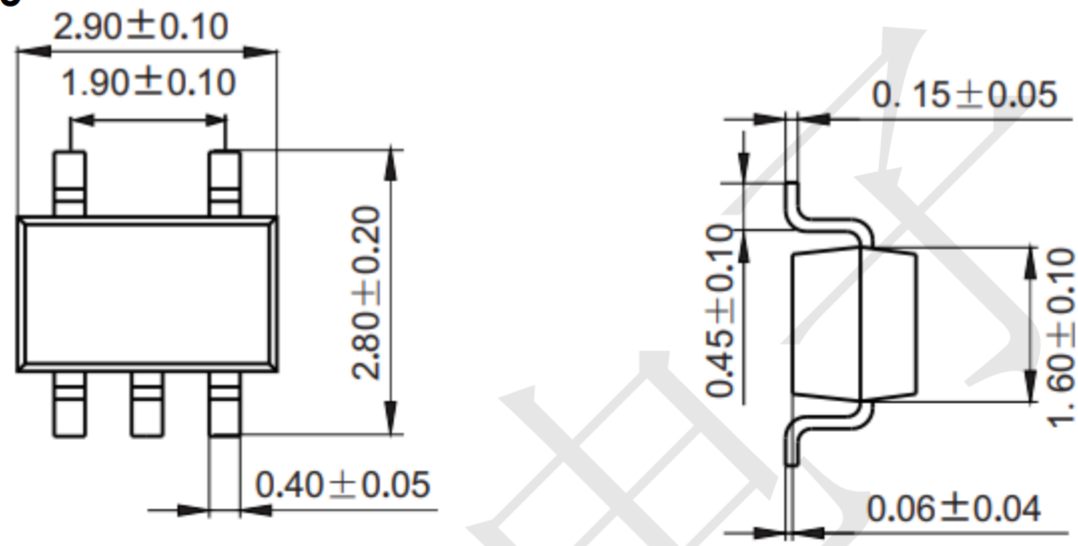
(2) All pulses and supplied at pulse repetition rate ≤ 10 MHz.

(3) The Inputs are measured separately one transition per measurement

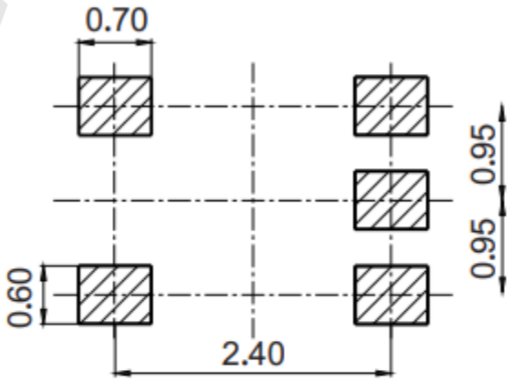
(4) t_{PLH} and t_{PHL} are the same as t_{PD}

Package Outline Dimensio Unit (mm)

SOT23-5



Mounting Pad Layout (unit: mm)



TC7S00 Series

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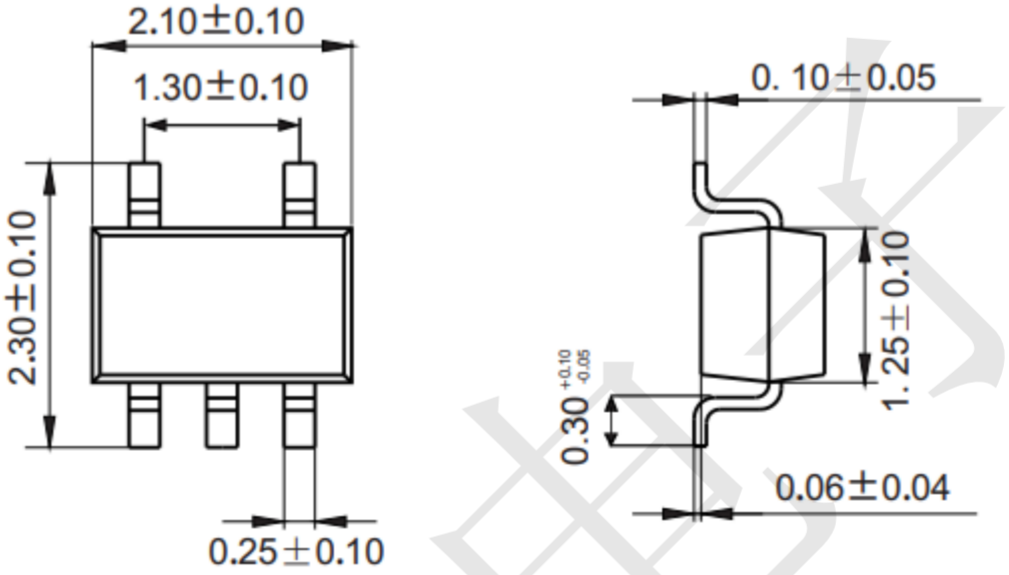
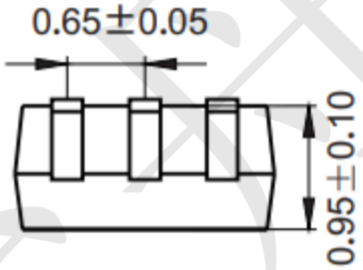
Package Outline Dimension Unit (mm)

SOT353





Mounting Pad Layout (unit: mm)