1.General Description

The 74AHC541 and 74AHCT541 are 8-bit buffer/line drivers with 3-state outputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2.Features and Benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 200 mA
- Overvoltage tolerant inputs to 5.5 V
- Input levels:
  - For 74AHC541: CMOS level
  - For 74AHCT541: TTL level
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2A exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V
- Multiple package options

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74AHC541D	SOP-20L	plastic small outline package; 20 leads; body width 7.5 mm	2000
74AHCT541D			
74AHC541PW	TSSOP-20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	2500
74AHCT541PW			

4. Function Diagram

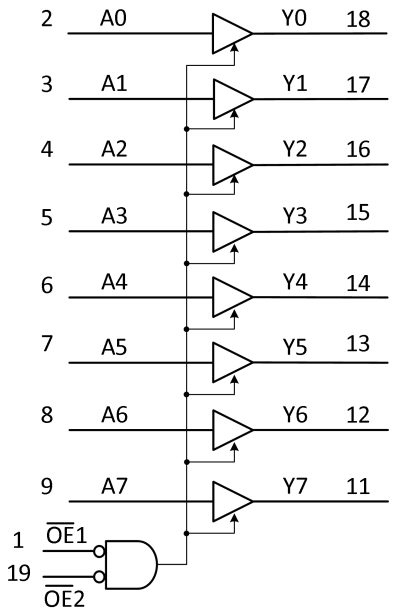


Fig. 1. Logic symbol

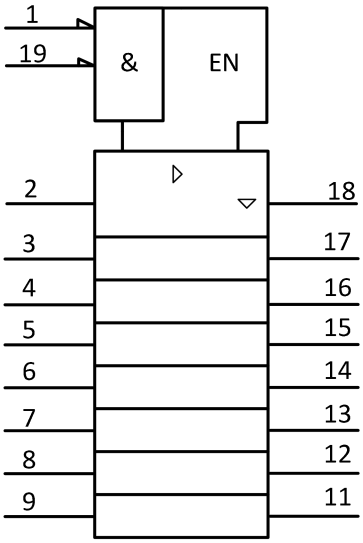


Fig. 2. IEC logic symbol

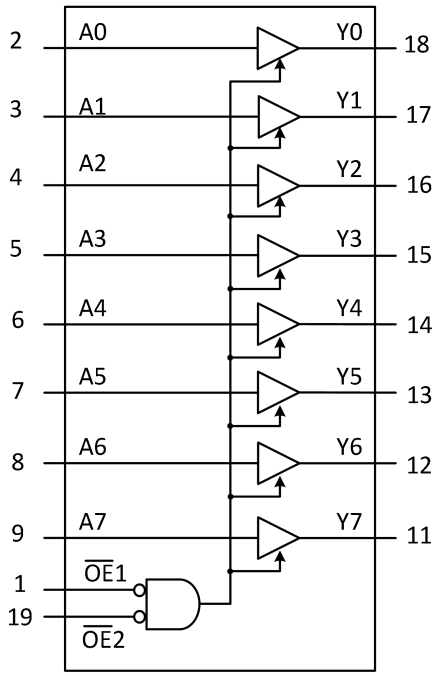


Fig. 3. Functional diagram

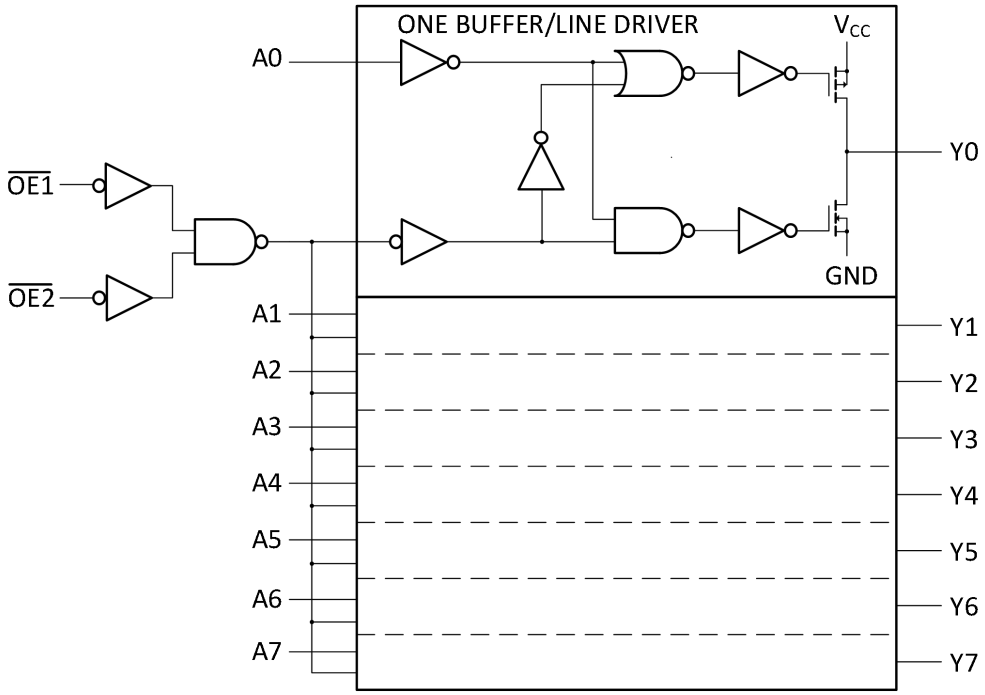


Fig. 4. Logic diagram

5. Pinning Information

5.1. Pinning

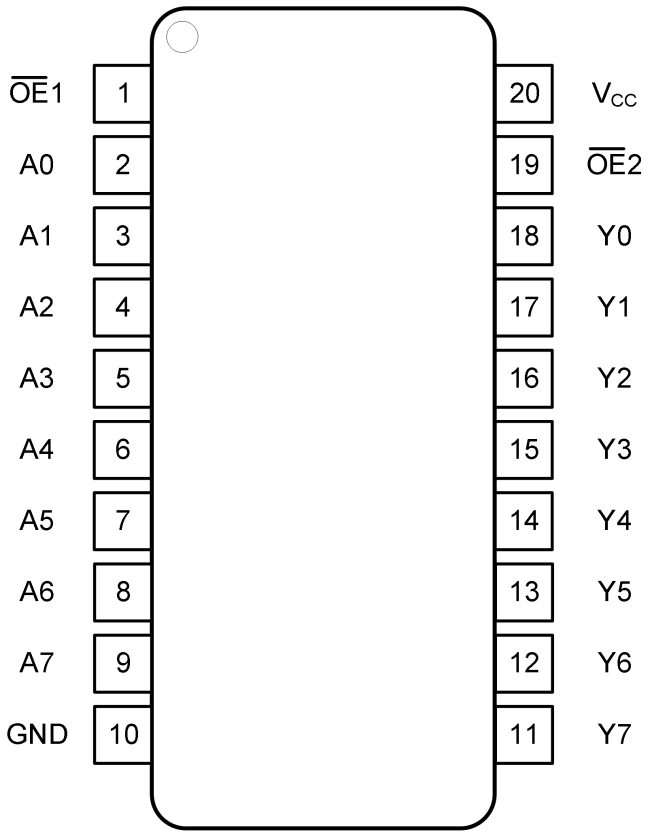


Fig. 5. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1$	1	Output enable input (active LOW)
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	Data input
GND	10	Ground (0 V)
Y0 to Y7	18, 17, 16, 15, 14, 13, 12, 11	Data output
$\overline{OE}2$	19	Output enable input (active LOW)
V_{CC}	20	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control		Input	Output
$\overline{OE}1$	$\overline{OE}2$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
V_I	Input voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V [1]	-20		mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_O	output current	$V_O = -0.5$ V to ($V_{CC} + 0.5$ V)		±25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation			500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74AHC541			74AHCT541			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0		5.5	0		5.5	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	25	125	-40	25	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V			100				ns/V
		V_{CC} = 5.0 V ± 0.5 V			20			20	ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74AHC541								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5			1.5		V
		V_{CC} = 3.0 V	2.1			2.1		V
		V_{CC} = 5.5 V	3.85			3.85		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V			0.5		0.5	V
		V_{CC} = 3.0 V			0.9		0.9	V
		V_{CC} = 5.5 V			1.65		1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -50 µA; V_{CC} = 2.0 V	1.9			1.9		V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9			2.9		V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.48			2.40		V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.80			3.70		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 50 µA; V_{CC} = 2.0 V			0.1		0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V			0.1		0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V			0.44		0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V			0.44		0.55	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 0 V to 5.5 V			±1		±2	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} = 5.5 V ; V_O = V_{CC} or GND			±2.5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 5.5 V			20		40	µA
C_I	input capacitance	$\overline{OE}$1, $\overline{OE}$2 input		4.0				pF
		An input		7.7				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74AHCT541								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.1			2.1		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -50 µA;	4.4			4.4		V
		I_O = -8.0 mA;	3.84			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = 50 µA;			0.1		0.1	V
		I_O = 8.0 mA;			0.44		0.55	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 0 V to 5.5 V			±1		±2	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} = 5.5 V ; V_O = V_{CC} or GND			±5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	per pin ; V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V			500		520	µA
C_I	input capacitance	$\overline{OE}1$, $\overline{OE}2$ input		4.0				pF
		An input		7.7				pF

10. Dynamic Characteristics

Table 7. Dynamic characteristics

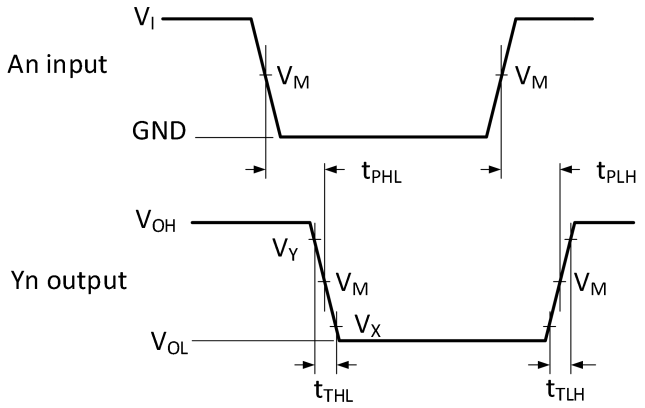
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8. Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74AHC541								
t_{pd}	propagation delay	An to Yn; see Fig. 6 [1]						
		V_{CC} = 3.0 V to 3.6 V, C_L = 15 pF	1.0		10	1.0	12	ns
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0		8	1.0	10	ns
t_{en}	enable time	$\overline{OE}$ n to Yn; see Fig. 7 [2]						
		V_{CC} = 3.0 V to 3.6 V, C_L = 15 pF	1.0		20	1.0	25	ns
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0		15	1.0	20	ns
t_{dis}	disable time	$\overline{OE}$n to Yn; see Fig. 7 [3]						
		V_{CC} = 3.0 V to 3.6 V, C_L = 15 pF	1.0		20	1.0	25	ns
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0		15	1.0	20	ns
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} [4]		18				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74AHCT541								
t_{pd}	propagation delay	An to Yn; see Fig. 6 [1]						
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0		8	1.0	10	ns
t_{en}	enable time	$\overline{OE}$n to Yn; see Fig. 7 [2]						
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0		17	1.0	20	ns
t_{dis}	disable time	$\overline{OE}$n to Yn; see Fig. 7 [3]						
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0		17	1.0	20	ns
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} [4]		18				pF

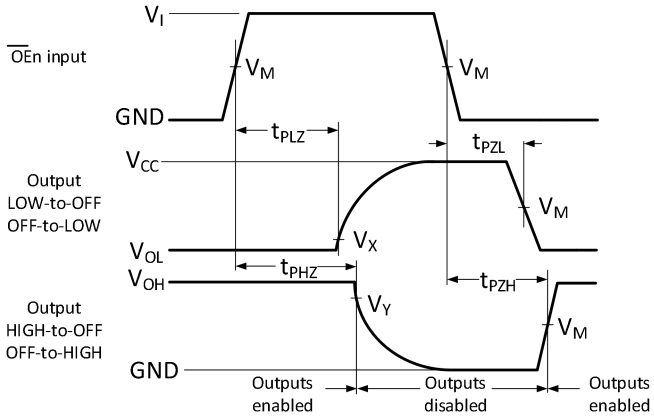
[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Input to output propagation delays

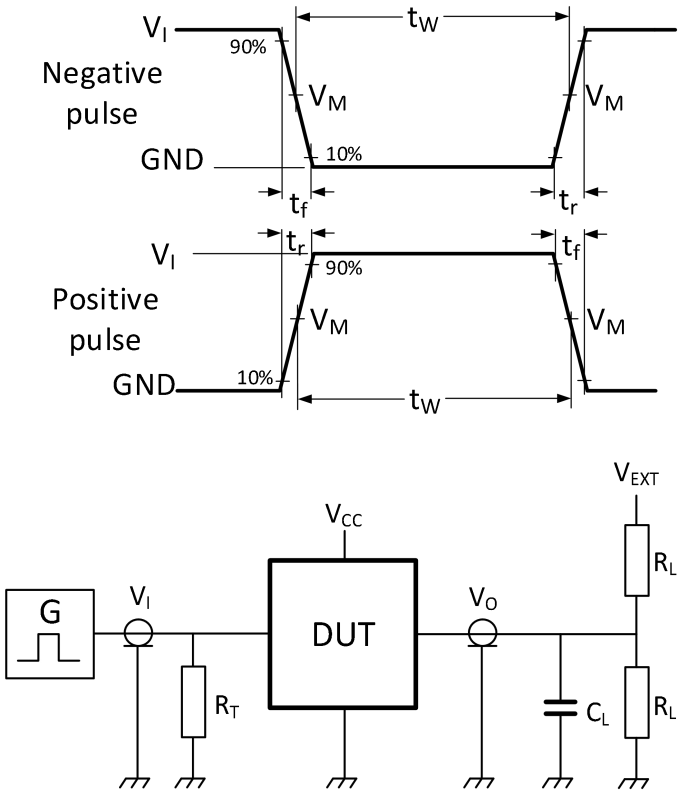


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC541	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3V	V_{OH} – 0.3V
74AHCT541	1.5V	$0.5V_{CC}$	V_{OL} + 0.3V	V_{OH} – 0.3V



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

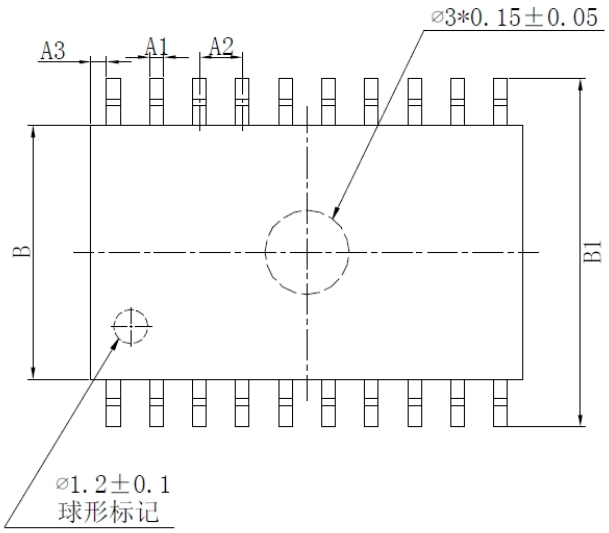
Fig. 8. Test circuit for measuring switching times

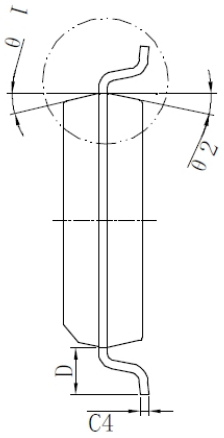
Table 9. Test data

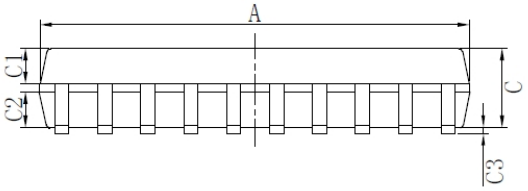
Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC541	V_{CC}	≤ 2.5 ns	15 pF	500Ω	open	GND	$2V_{CC}$
74AHCT541	3 V	≤ 2.5 ns	15 pF	500Ω	open	GND	$2V_{CC}$

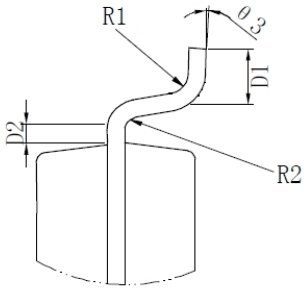
11. Package Outline

SOP-20L



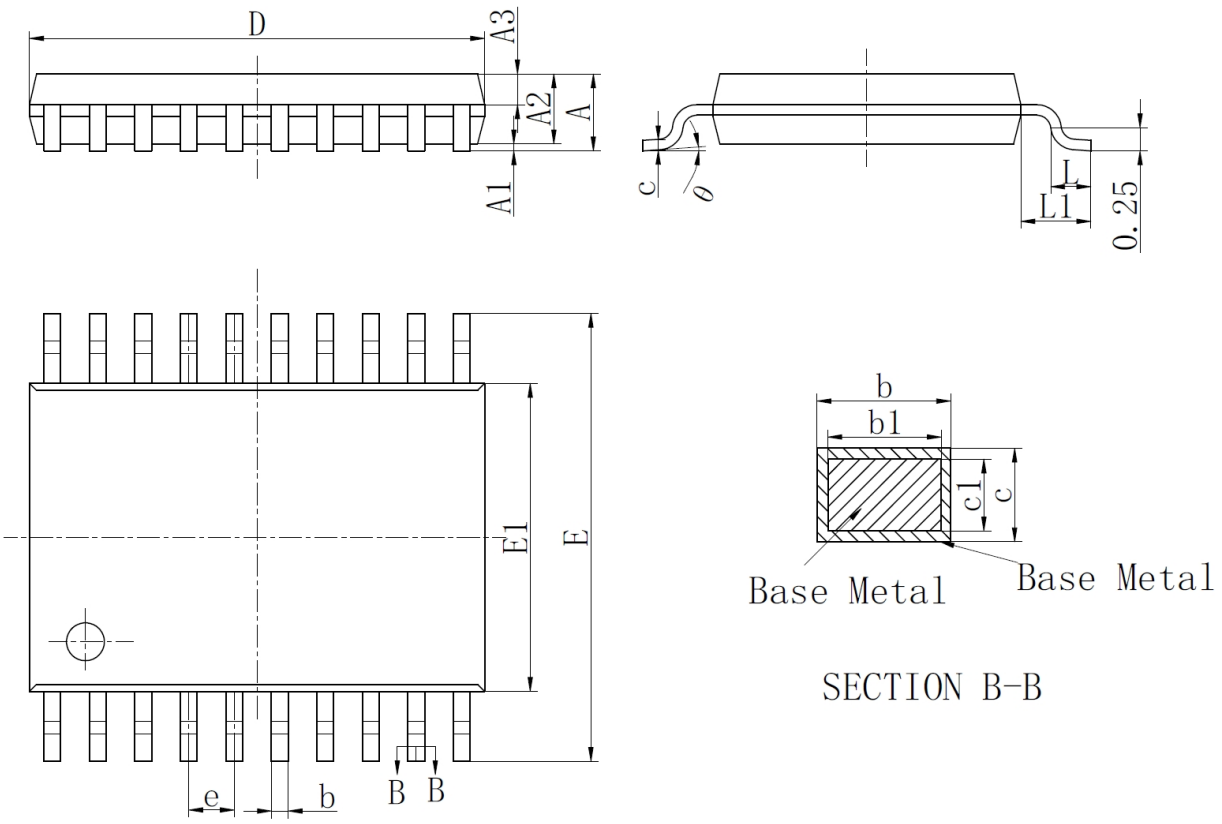






Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	12.600	12.900	C4	0.246	0.262
A1	0.381	0.431	D	1.353	1.453
A2	1.240	1.300	D1	0.764	0.964
A3	0.450	0.460	D2	0.18TYP	
B	7.400	7.600	R1	0.30TYP	
B1	10.206	10.406	R2	0.20TYP	
C	2.150	2.300	θ1	12° TYP	
C1	0.938	1.038	θ2	12° TYP	
C2	0.938	1.2038	θ3	0° ~ 8°	
C3	0.145	0.205			

TSSOP-20L



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	-	1.20	E	6.20	6.60
A1	0.05	0.15	e	0.65BSC	
A2	0.80	1.05	L	0.45	0.75
A3	0.39	0.49	L1	1.00REF	
b	0.20	0.28	θ	0°	8°
b1	0.19	0.25			
c	0.13	0.17			
c1	0.12	0.14			
D	6.40	6.60			
E1	4.30	4.50			

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 13. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74AHC_AHCT541 Rev. 1.0	Dec 15, 2025	Draft datasheet		