1.General Description

The 74HC595; 74HCT595 are 8-bit serial-in/serial or parallel-out shift registers with storage registers and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide operating voltage 2.7 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8C(2.7 V to 3.6 V)
  - JESD7A(2.7 V to 6.0 V)
- Input levels:
  - For 74HC595: CMOS level
  - For 74HCT595: TTL level
- ESD protection:

- HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
- CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V

■ Multiple package options

■ Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3.Applications

■ Serial-to-parallel data conversion

■ Remote control holding register

4.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC595D	SOP-16L	plastic small outline package; 16 leads; body width 3.9 mm	2500
74HCT595D			
74HC595PW	TSSOP-16L	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500
74HCT595PW			
74HC595DB	SSOP-16L	plastic small outline package; 16 leads; body width 5.3 mm	2000
74HCT595DB			

5.Function Diagram

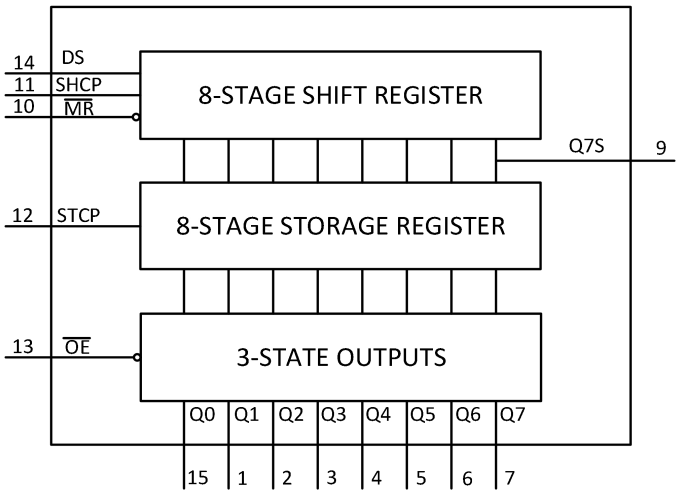


Fig. 1. Functional diagram

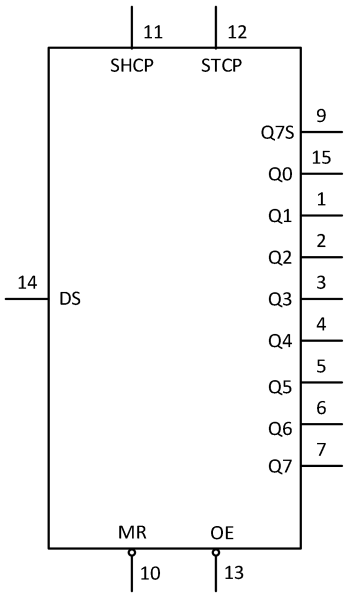


Fig. 2. Logic symbol

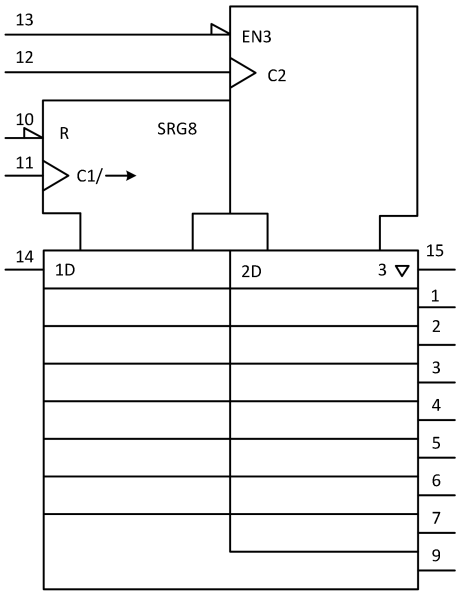


Fig. 3. IEC logic symbol

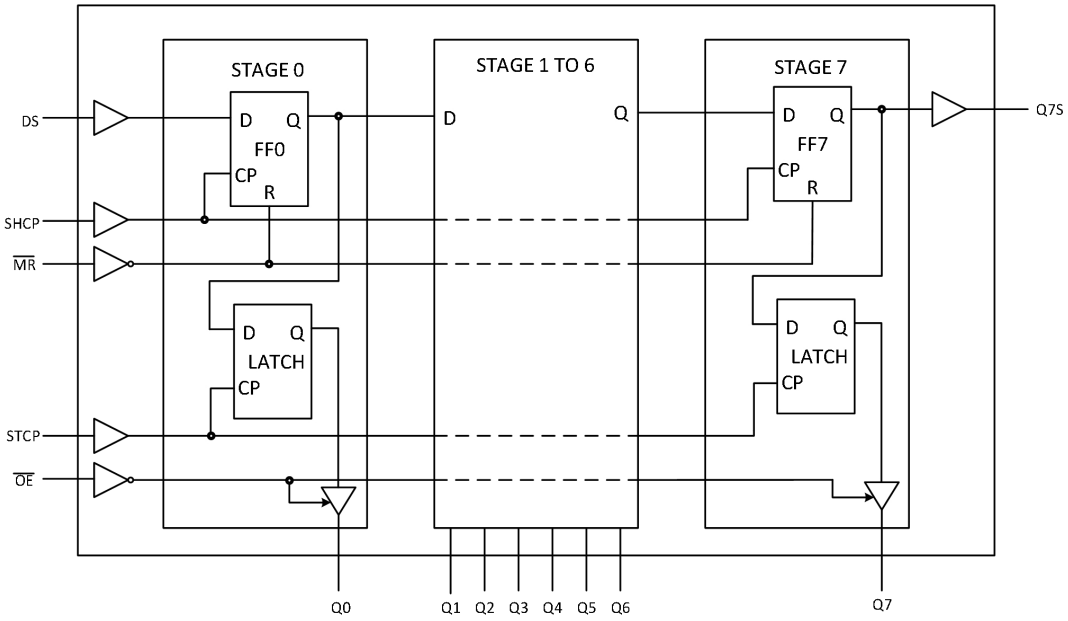


Fig. 4. Logic diagram

6.Pinning Information

6.1. Pinning

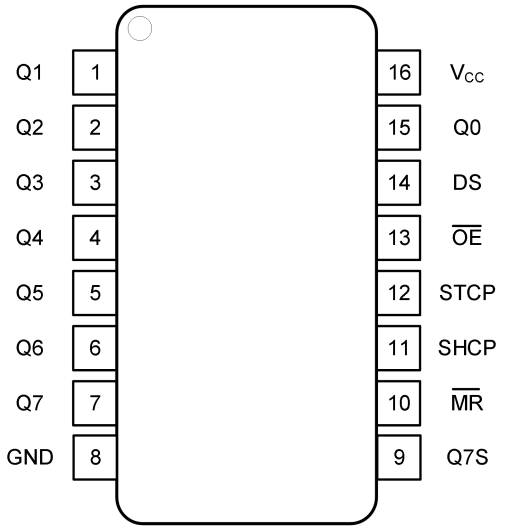


Fig. 5. Top view pin configuration SOP, SSOP and TSSOP

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	Parallel data output
GND	8	Ground (0V)
Q7S	9	Serial data output
$\overline{MR}$	10	Master reset (active LOW)
SHCP	11	Shift register clock input
STCP	12	Storage register clock input
$\overline{OE}$	13	Output enable input (active LOW)
DS	14	Serial data input
V_{CC}	16	Supply voltage

7.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH transition;

X = don't care; NC = no change; Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

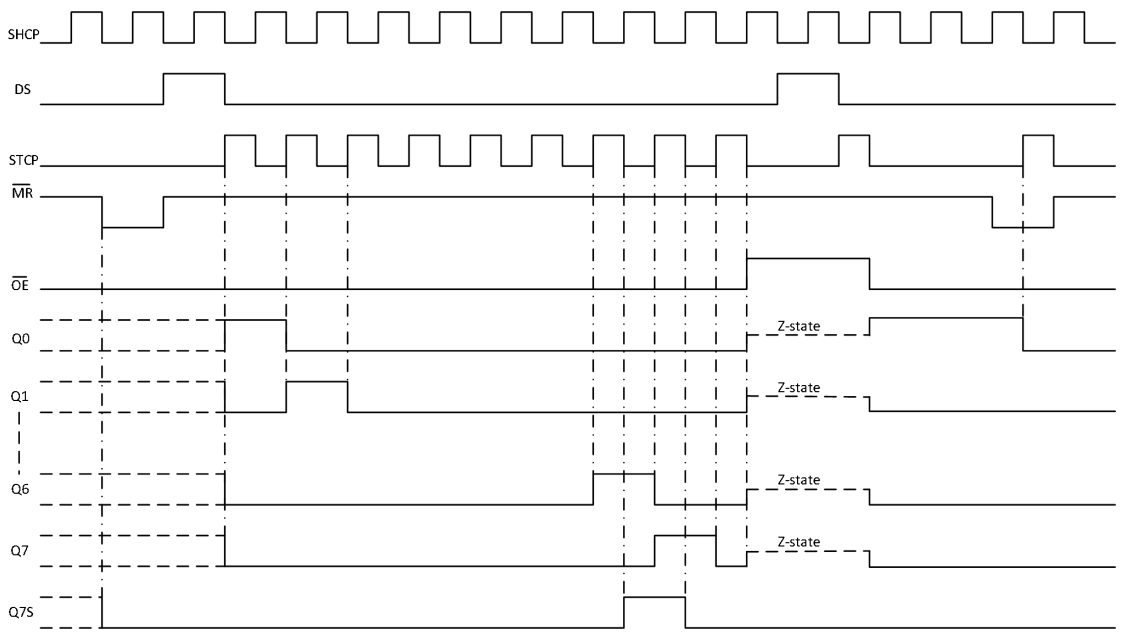


Fig. 6. Timing diagram

8.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V [1]		±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V [1]		±20	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V		±35	mA
I_{CC}	supply current			70	mA
I_{GND}	ground current		-70		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC595			74HCT595			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.7	5.0	6.0	2.7	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.0 V			371			371	ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

10. Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC595								
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V	2.0			2.0		V
		V_{CC} = 4.5 V	3.15			3.15		V
		V_{CC} = 6.0 V	4.2			4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V			0.6		0.6	V
		V_{CC} = 4.5 V			1.35		1.35	V
		V_{CC} = 6.0 V			1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		all outputs						
		I_O = -20µA; V_{CC} = 3.0 V	2.9			2.9		V
		I_O = -20µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -20µA; V_{CC} = 6.0 V	5.9			5.9		V
		Q7S output						
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34			5.2		V
		Qn bus driver outputs						
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.34			5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		all outputs						
		I_O = 20µA; V_{CC} = 3.0 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 6.0 V			0.1		0.1	V
		Q7S output						
		I_O = 4.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V			0.33		0.4	V
		Qn bus driver outputs						
		I_O = 6.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V			0.33		0.4	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND ; V_{CC} = 6.0 V			±1		±1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; V_{CC} = 6.0V ; $V_O = V_{CC}$ or GND			±5		±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND ; I_O = 0A ; V_{CC} = 6.0 V			20		40	µA
C_I	input capacitance			6.5				pF
74HCT595								
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V	2.0			2.0		V
		V_{CC} = 4.5 V	2.0			2.0		V
		V_{CC} = 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V			0.6		0.6	V
		V_{CC} = 4.5 V			0.8		0.8	V
		V_{CC} = 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		all outputs						
		I_O = -20µA; V_{CC} = 3.0 V	2.9			2.9		V
		I_O = -20µA; V_{CC} = 4.5 V	4.4			4.4		V
		Q7S output						
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		Qn bus driver outputs						
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		all outputs						
		I_O = 20µA; V_{CC} = 3.0 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 4.5 V			0.1		0.1	V
		Q7S output						
		I_O = 4.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		Qn bus driver outputs						
		I_O = 6.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND ; V_{CC} = 5.5 V			±1		±1	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; V_{CC} = 5.5 V ; $V_O = V_{CC}$ or GND			±5		±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND ; I_O = 0 A ; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	per pin ; $V_I = V_{CC}$ - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V			450		490	µA
C_I	input capacitance			6.5				pF

[1]All typical values are measured at T_{amb} = 25°C.

11. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC595								
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 7 [2]						
		V_{CC} = 3.0 V			30		35	ns
		V_{CC} = 4.5 V			20		25	ns
		V_{CC} = 6.0 V			15		18	ns
		STCP to Qn; see Fig. 8 [2]						
		V_{CC} = 3.0 V			45		50	ns
		V_{CC} = 4.5 V			25		30	ns
		V_{CC} = 6.0 V			20		25	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 10						
		V_{CC} = 3.0 V			30		35	ns
		V_{CC} = 4.5 V			19		22	ns
		V_{CC} = 6.0 V			16		19	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 11 [3]						
		V_{CC} = 3.0 V			22		25	ns
		V_{CC} = 4.5 V			14		17	ns
		V_{CC} = 6.0 V			13		16	ns

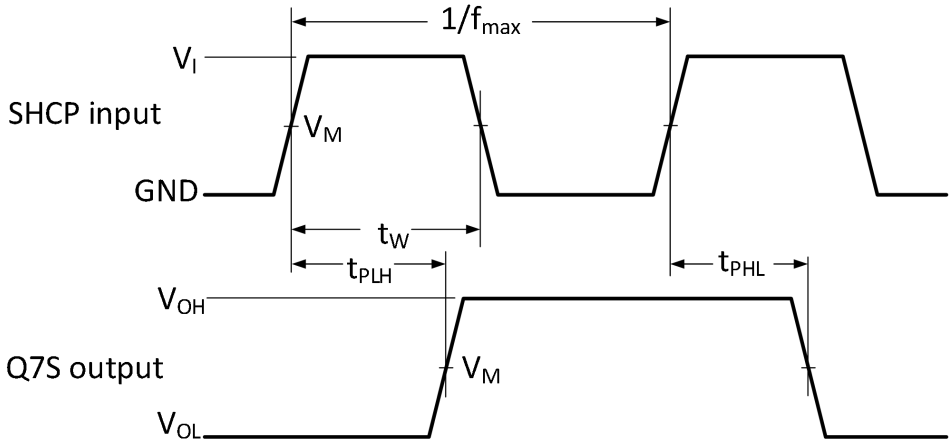
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 11 [4]						
		V_{CC} = 3.0 V			22		25	ns
		V_{CC} = 4.5 V			15		18	ns
		V_{CC} = 6.0 V			13		15	ns
t_W	pulse width	SHCP HIGH or LOW; see Fig. 7						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	19			22		ns
		V_{CC} = 6.0 V	16			19		ns
		STCP HIGH or LOW; see Fig. 8						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	19			22		ns
		V_{CC} = 6.0 V	16			19		ns
		$\overline{MR}$ LOW; see Fig.10						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	19			22		ns
		V_{CC} = 6.0 V	16			19		ns
t_{SU}	set up time	DS to SHCP; see Fig.9						
		V_{CC} = 3.0 V	16			20		ns
		V_{CC} = 4.5 V	13			15		ns
		V_{CC} = 6.0 V	11			13		ns
		SHCP to STCP; see Fig.9						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	19			22		ns
		V_{CC} = 6.0 V	16			19		ns
t_h	hold time	DS to SHCP; see Fig.9						
		V_{CC} = 3.0 V	3			3		ns
		V_{CC} = 4.5 V	3			3		ns
		V_{CC} = 6.0 V	3			3		ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 10						
		V_{CC} = 3.0 V	16			20		ns
		V_{CC} = 4.5 V	13			15		ns
		V_{CC} = 6.0 V	11			13		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
f_{max}	maximum frequency	SHCP or STCP; see Fig. 7 and Fig. 8						
		V_{CC} = 3.0 V	20			16		MHz
		V_{CC} = 4.5 V	24			20		MHz
		V_{CC} = 6.0 V	28			24		MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}; [5][6]		115				pF
74HCT595								
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 7 [2]						
		V_{CC} = 4.5 V			25		30	ns
		STCP to Qn; see Fig. 8 [2]						
		V_{CC} = 4.5 V			25		30	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 10						
		V_{CC} = 4.5 V			25		30	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 11 [3]						
		V_{CC} = 4.5 V			20		25	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 11 [4]						
		V_{CC} = 4.5 V			20		25	ns
t_W	pulse width	SHCP HIGH or LOW; see Fig. 7						
		V_{CC} = 4.5 V	19			22		ns
		STCP HIGH or LOW; see Fig. 8						
		V_{CC} = 4.5 V	19			22		ns
		$\overline{MR}$ LOW; see Fig.10						
		V_{CC} = 4.5 V	19			22		ns
t_{SU}	set up time	DS to SHCP; see Fig.9						
		V_{CC} = 4.5 V	13			15		ns
		SHCP to STCP; see Fig.9						
		V_{CC} = 4.5 V	19			22		ns
t_h	hold time	DS to SHCP; see Fig.9						
		V_{CC} = 4.5 V	3			3		ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 10						
		V_{CC} = 4.5 V	13			15		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
f_{max}	maximum frequency	SHCP or STCP; see Fig. 7 and Fig. 8						
		V_{CC} = 4.5 V	24			20		MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}; [5][6]		115				pF

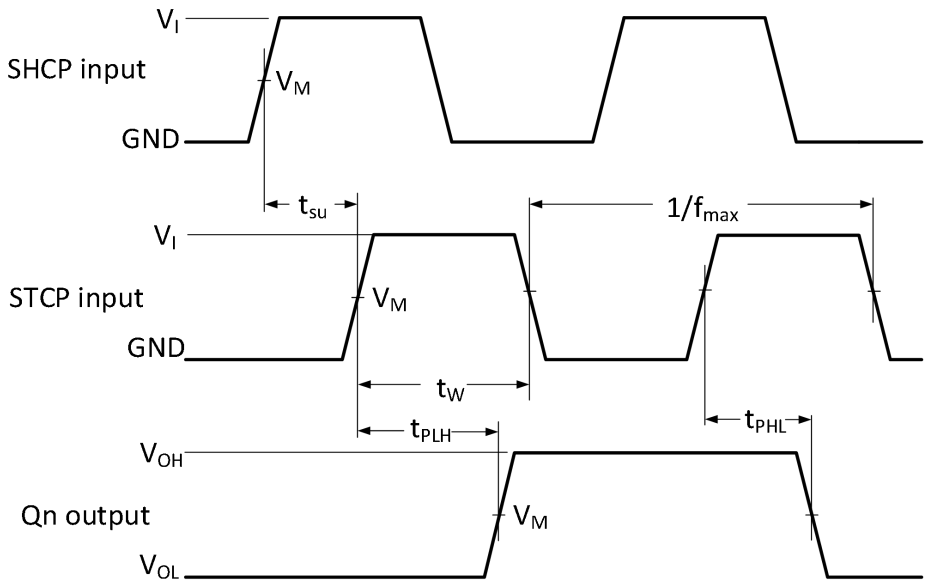
[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
[6] All 9 outputs switching.

11.1. Waveforms and test circuit



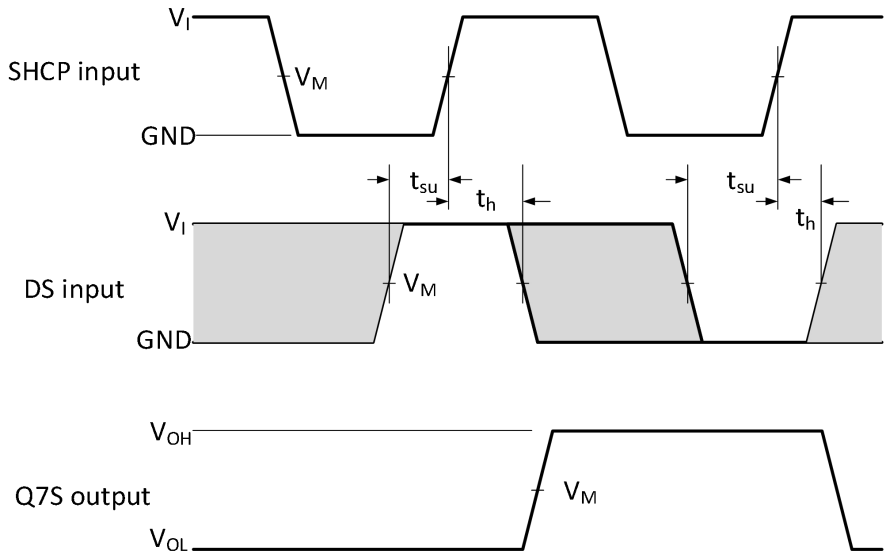
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Shift clock pulse, maximum frequency and input to output propagation delays



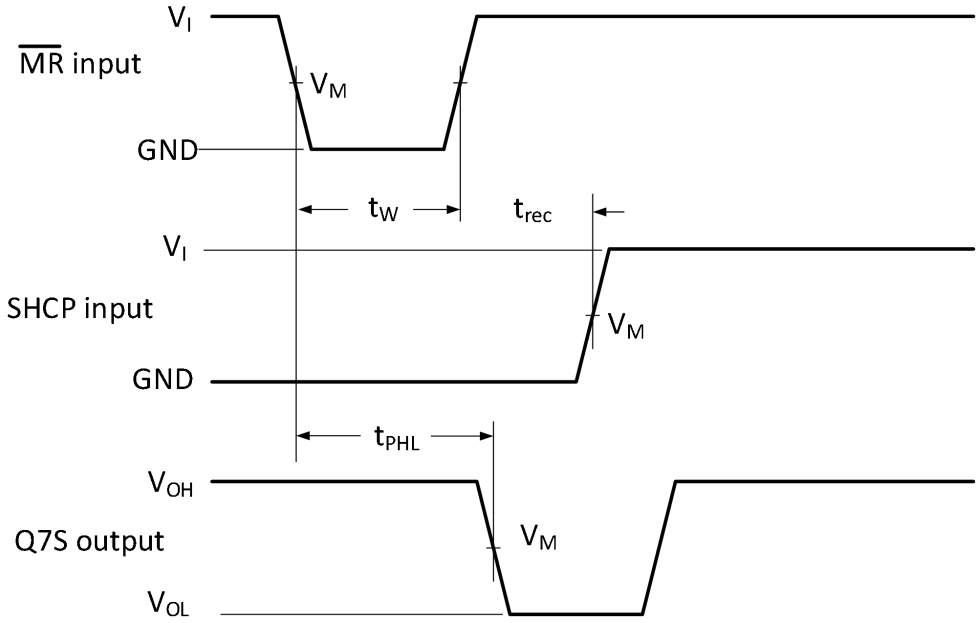
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Storage clock to output propagation delays



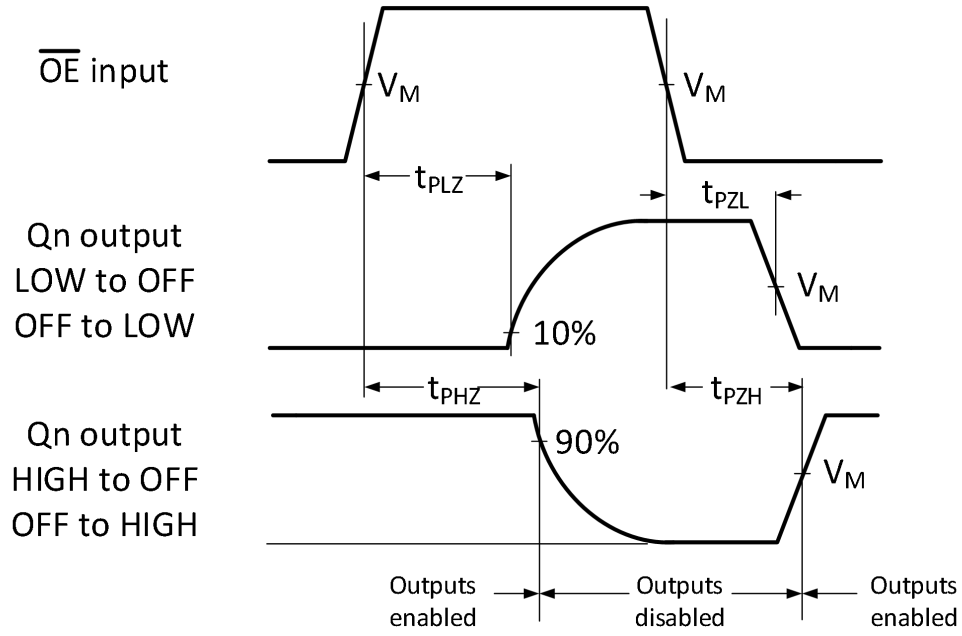
Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Data set up and hold times



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. Master reset to output propagation delays

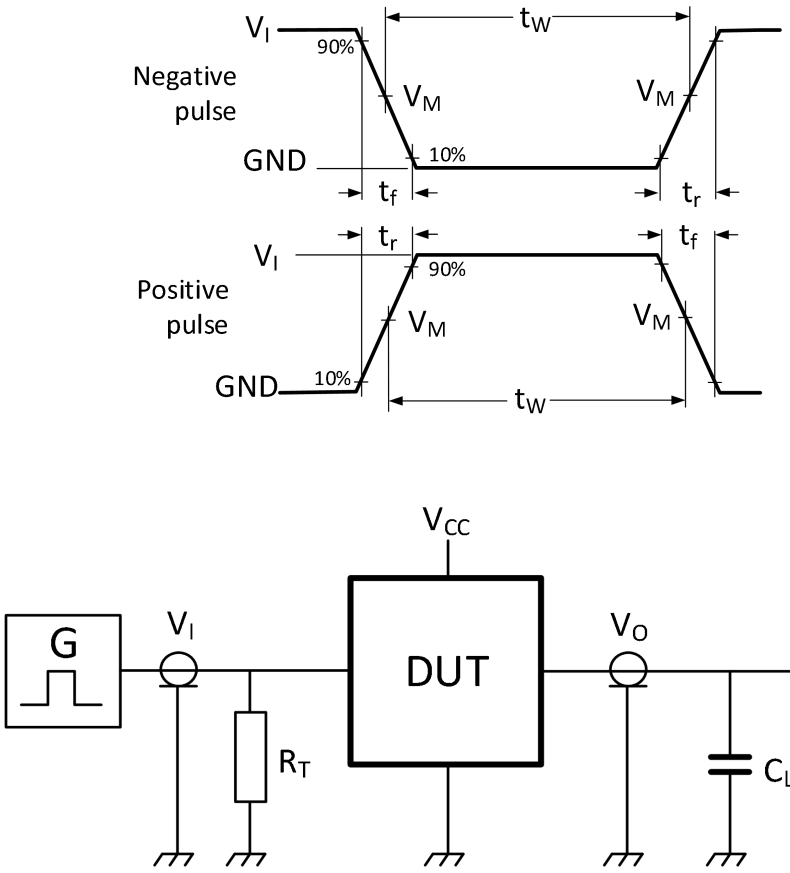


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 11. Enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC595	$0.5V_{CC}$	$0.5V_{CC}$
74HCT595	1.3 V	1.3 V



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

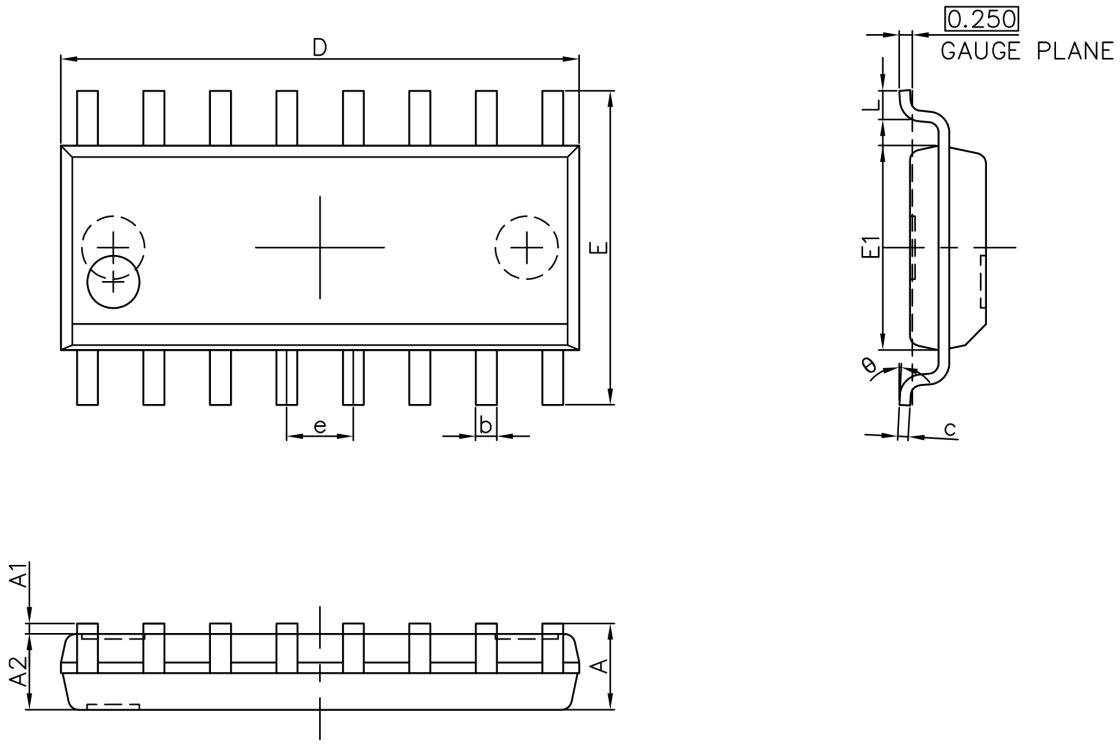
Fig. 12. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PZL}, t_{PLZ}	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}
74HC595	V_{CC}	2.5 ns	15 pF	500Ω	V_{CC}	Open	GND
74HCT595	3 V	2.5 ns	15pF	500Ω	V_{CC}	Open	GND

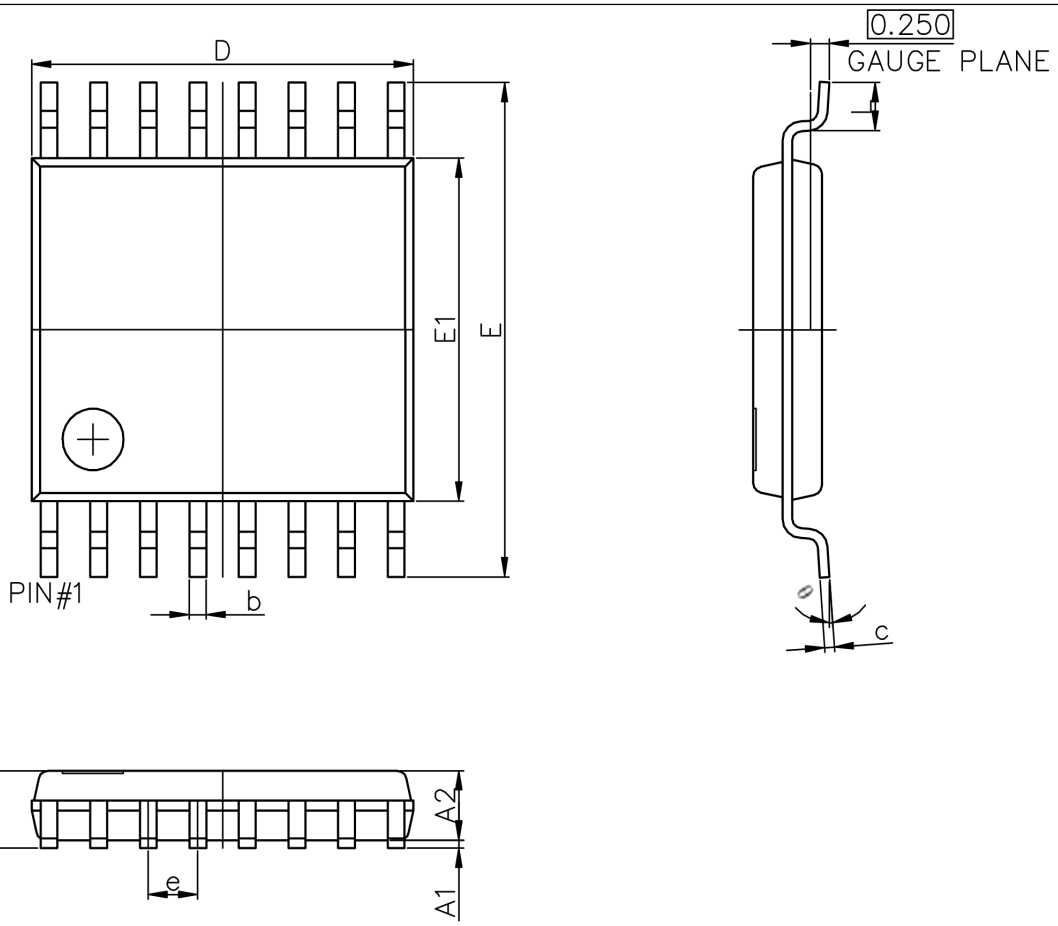
12. Package Outline

SOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.750	——	0.069
A1	0.150	0.250	0.006	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
e	1.270(BSC)		0.050(BSC)	
E	5.900	6.100	0.232	0.240
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.200	——	0.047
A1	0.020	0.100	0.001	0.004
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
e	0.650(BSC)		0.026(BSC)	
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

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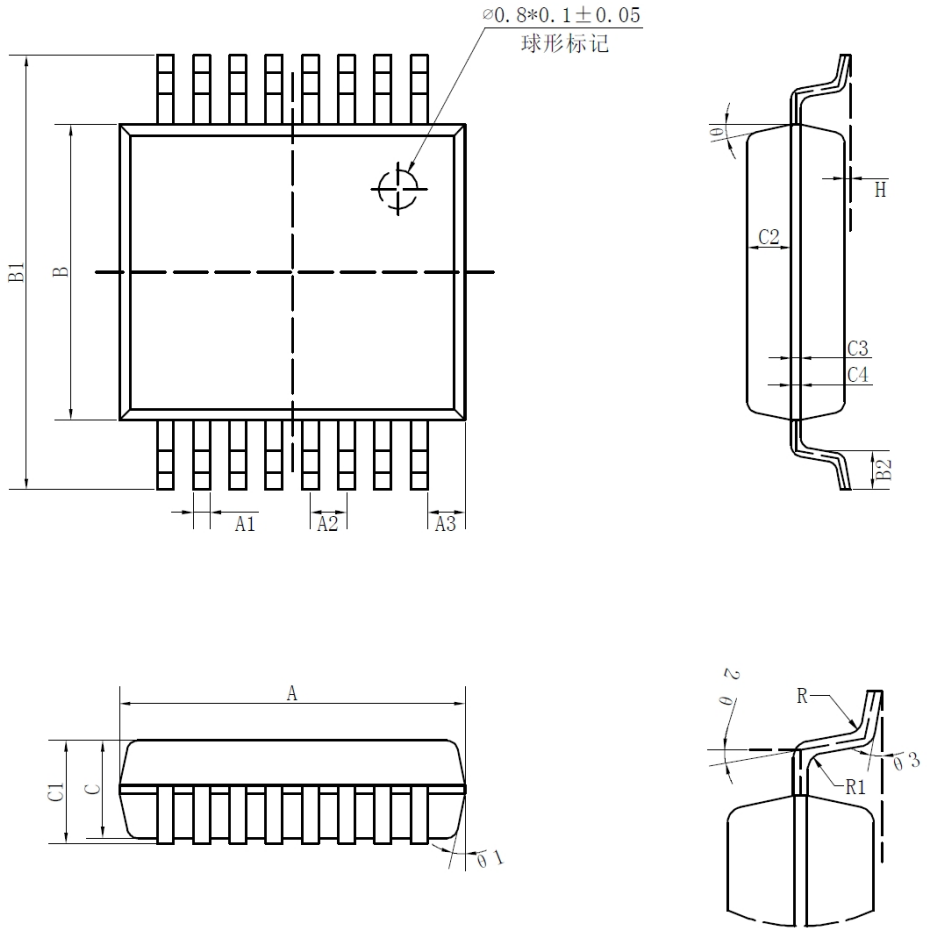

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	6.15	6.25	C3	0.152	
A1	0.30TYP		C4	0.172	
A2	0.65TYP		H	0.05	0.15
A3	0.675TYP		θ	12° TYP4	
B	5.25	5.35	θ1	12° TYP4	
B1	7.65	7.95	θ2	10° TYP	
B2	0.60	0.80	θ3	0° ~ 8°	
C	1.70	1.80	R	0.20TYP	
C1	1.75	1.95	R1	0.15TYP	
C2	0.799				

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT595 Rev. 1.0	Aug 08, 2024	Product datasheet		