1.General Description

The 74HC259; 74HCT259 is an 8-bit addressable latch. The device features four modes of operation. In the addressable latch mode, data on the D input is written into the latch addressed by the inputs A0 to A3. The addressed latch will follow the data input, non-addressed latches will retain their previous states. In memory mode, all latches retain their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the D input and all other outputs are LOW. In the reset mode, all outputs are forced LOW and unaffected by the data or address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Combined demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Input levels:
  - For 74HC259: CMOS level
  - For 74HCT259: TTL level

■ ESD protection:

- HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3500 V
- CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V

■ Multiple package options

■ Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC259D	SOP-16L	plastic small outline package; 16 leads; body width 3.9 mm	2500
74HCT259D			
74HC259PW	TSSOP-16L	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500
74HCT259PW			

4. Function Diagram

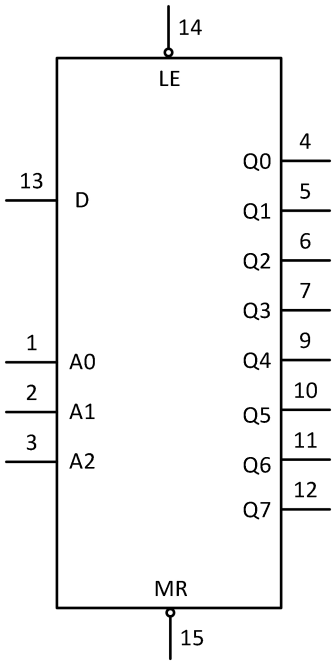


Fig. 1. Logic symbol

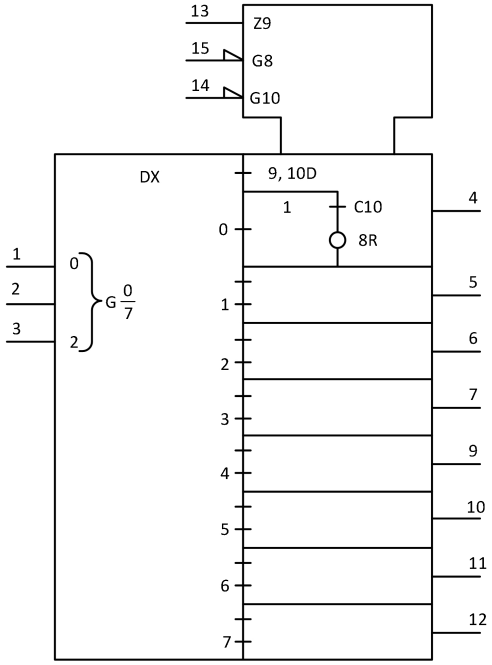


Fig. 2. IEC logic symbol

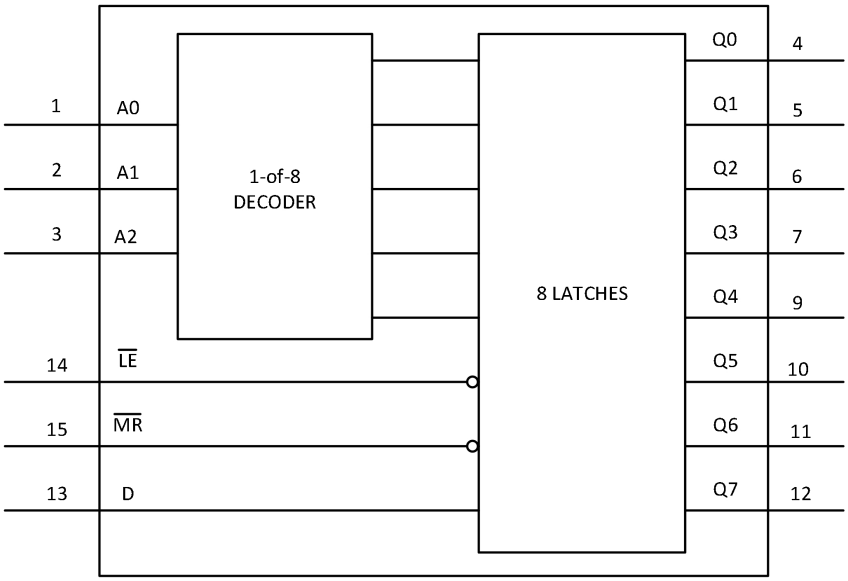


Fig. 3. Functional diagram

5.Pinning Information

5.1. Pinning

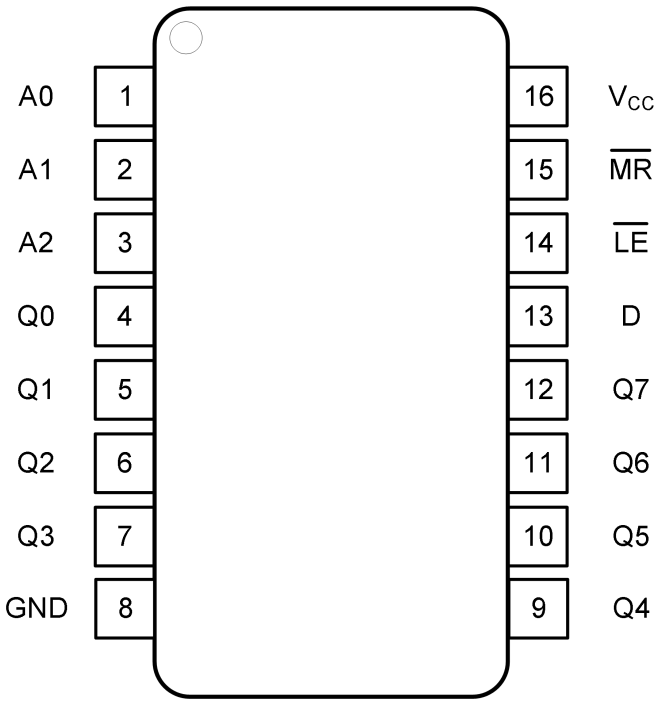


Fig. 4. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	Address input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	4, 5, 6, 7, 9, 10, 11, 12	Latch output
GND	8	Ground (0 V)
D	13	Data input
$\overline{LE}$	14	Latch enable input (active LOW)
$\overline{MR}$	15	Conditional reset input (active LOW)
V_{CC}	16	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH LE transition;

q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

Operating mode	Input						Output							
	$\overline{MR}$	$\overline{LE}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset(clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Memory (no action)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	H	L	q_0	q_1	q_2	Q=d	q_4	q_5	q_6	q_7
	H	L	d	L	L	H	q_0	q_1	q_2	q_3	Q=d	q_5	q_6	q_7
	H	L	d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q=d	q_6	q_7
	H	L	d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q=d	q_7
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

Table 4. Operating mode select table

H = HIGH voltage level; L = LOW voltage level.

$\overline{LE}$	$\overline{MR}$	Mode
L	H	Addressable latch mode
H	H	Memory mode
L	L	Demultiplexer mode
H	L	Reset mode

7.Absolute Maximum Ratings

Stresses exceeding the absolut`e maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		±25	mA
I_{CC}	supply current			70	mA
I_{GND}	ground current		-70		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC259			74HCT259			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	25	125	-40	25	125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC} = 2.0 V			625				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC259								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5			1.5		V
		V_{CC} = 4.5 V	3.15			3.15		V
		V_{CC} = 6.0 V	4.2			4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V			0.5		0.5	V
		V_{CC} = 4.5 V			1.35		1.35	V
		V_{CC} = 6.0 V			1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 µA; V_{CC} = 2.0 V	1.9			1.9		V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9			5.9		V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34			5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 µA; V_{CC} = 2.0 V			0.1		0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V			0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V			±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 6.0 V			20		40	µA
C_I	input capacitance			6.5				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT259								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20 µA	4.4			4.4		V
		I_O = -4.0 mA	3.84			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = 20 µA			0.1		0.1	V
		I_O = 4.0 mA			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V			±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A			450		490	µA
C_I	input capacitance			6.5				pF

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

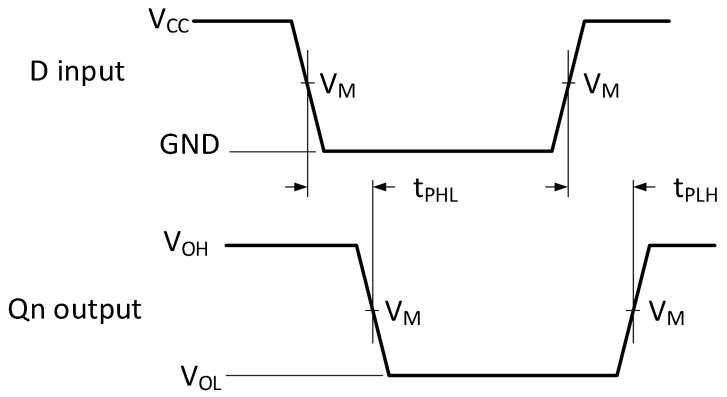
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC259								
t_{pd}	propagation delay	D to Qn; see Fig. 5 [2]						
		V_{CC} = 2.0 V			55		60	ns
		V_{CC} = 4.5 V			17		20	ns
		V_{CC} = 6.0 V			13		15	ns
		An to Qn; see Fig. 6 [2]						
		V_{CC} = 2.0 V			55		60	ns
		V_{CC} = 4.5 V			17		20	ns
		V_{CC} = 6.0 V			13		15	ns
		$\overline{LE}$ to Qn; see Fig. 7 [2]						
		V_{CC} = 2.0 V			55		60	ns
		V_{CC} = 4.5 V			17		20	ns
		V_{CC} = 6.0 V			13		15	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 8						
		V_{CC} = 2.0 V			55		60	ns
		V_{CC} = 4.5 V			17		20	ns
		V_{CC} = 6.0 V			13		15	ns
t_t	transition time	see Fig. 7 [3]						
		V_{CC} = 2.0 V			8		10	ns
		V_{CC} = 4.5 V			7		9	ns
		V_{CC} = 6.0 V			7		9	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_W	pulse width	$\overline{LE}$ HIGH or LOW; see Fig. 7						
		V_{CC} = 2.0 V	100			120		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
		$\overline{MR}$ LOW; see Fig. 8						
		V_{CC} = 2.0 V	75			90		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_{SU}	set-up time	D, An to $\overline{LE}$; see Fig. 9 and Fig. 10						
		V_{CC} = 2.0 V	75			90		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_h	hold time	D to $\overline{LE}$; see Fig. 9 and Fig. 10						
		V_{CC} = 2.0 V	5			5		ns
		V_{CC} = 4.5 V	5			5		ns
		V_{CC} = 6.0 V	5			5		ns
		An to $\overline{LE}$; see Fig. 9 and Fig. 10						
		V_{CC} = 2.0 V	5			5		ns
		V_{CC} = 4.5 V	5			5		ns
		V_{CC} = 6.0 V	5			5		ns
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} [4]		26				pF
74HCT259								
t_{pd}	propagation delay	D to Qn; see Fig. 5 [2]						
		V_{CC} = 4.5 V			17		20	ns
		An to Qn; see Fig. 6 [2]						
		V_{CC} = 4.5 V			17		20	ns
		$\overline{LE}$ to Qn; see Fig. 7 [2]						
		V_{CC} = 4.5 V			17		20	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 8						
		V_{CC} = 4.5 V			17		20	ns
t_t	transition time	see Fig. 7 [3]						
		V_{CC} = 4.5 V			7		9	ns
t_W	pulse width	$\overline{LE}$ HIGH or LOW; see Fig. 7						
		V_{CC} = 4.5 V	20			24		ns
		$\overline{MR}$ LOW; see Fig. 8						
		V_{CC} = 4.5 V	31			38		ns
t_{su}	set-up time	D, An to $\overline{LE}$; see Fig. 9 and Fig. 10						
		V_{CC} = 4.5 V	15			18		ns
t_h	hold time	D to $\overline{LE}$; see Fig. 9 and Fig. 10						
		V_{CC} = 4.5 V	5			5		ns
		An to $\overline{LE}$; see Fig. 9 and Fig. 10						
		V_{CC} = 4.5 V	5			5		ns
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} - 1.5 V [4]		28				pF

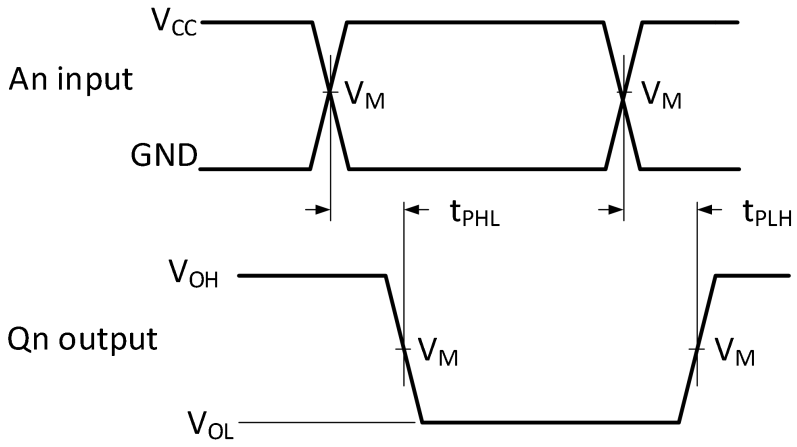
[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



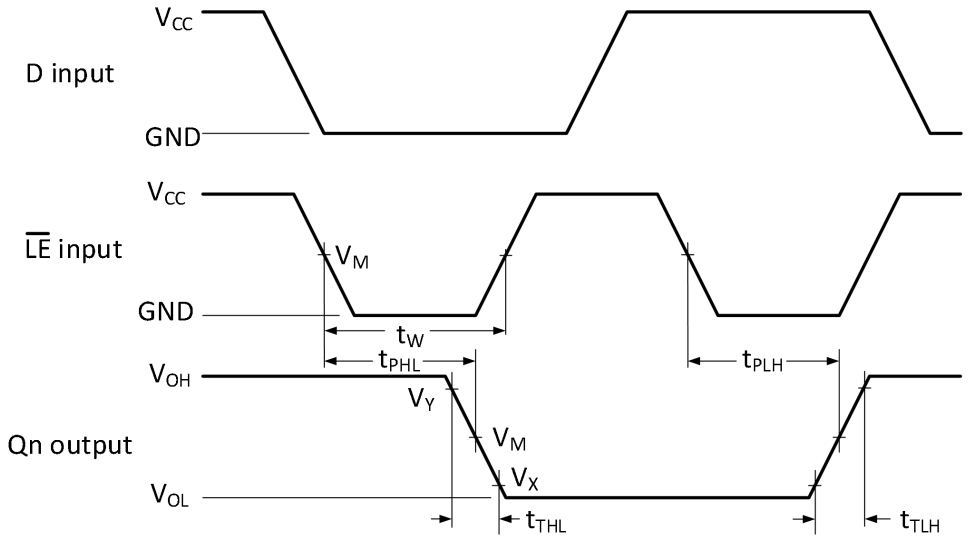
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Data input to output propagation delays



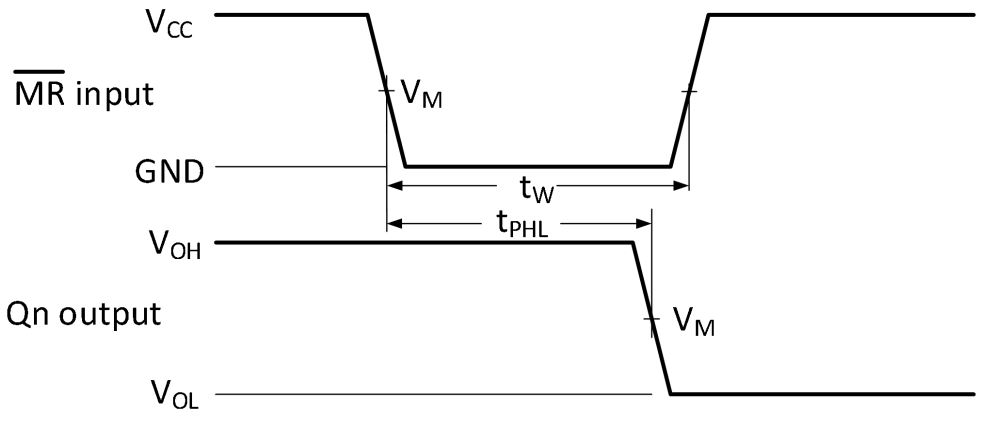
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Address input to output propagation delays



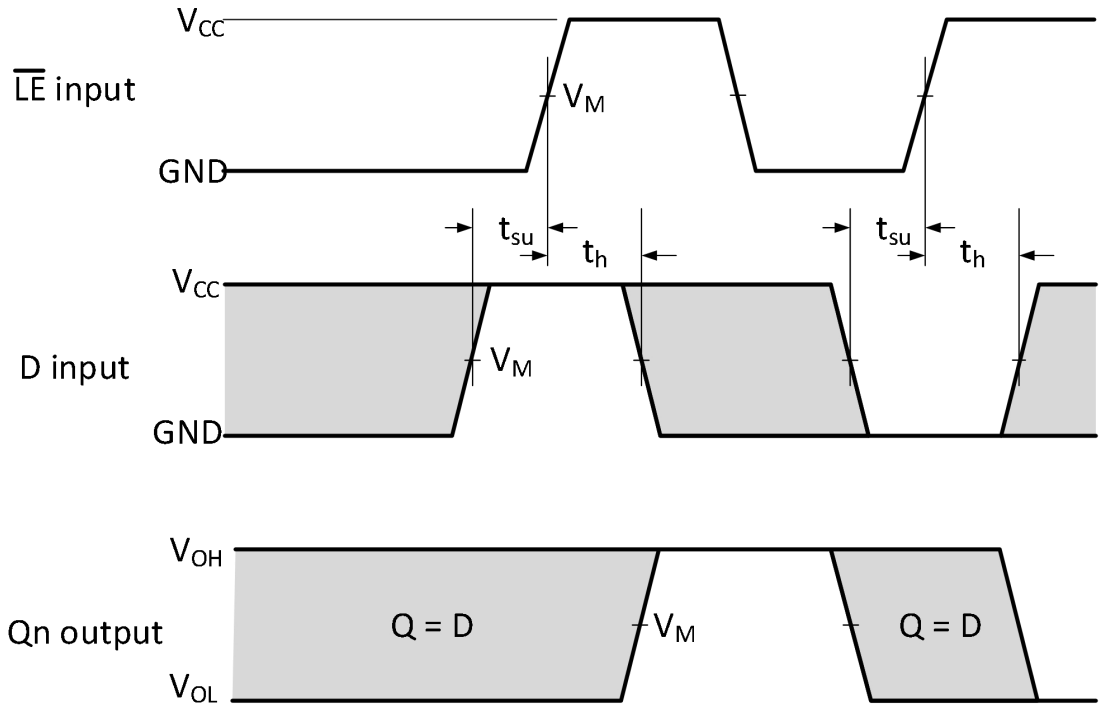
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Enable input to output propagation delays and pulse width



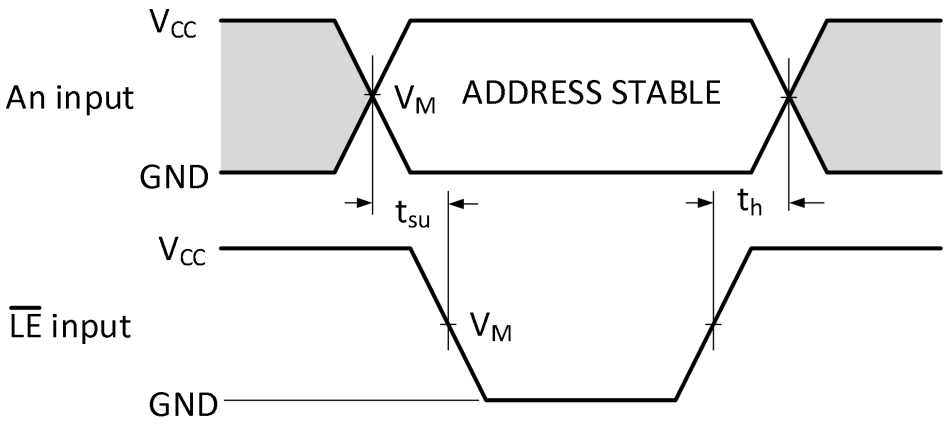
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Master reset input to output propagation delays



Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. Data input to latch enable input set-up and hold times

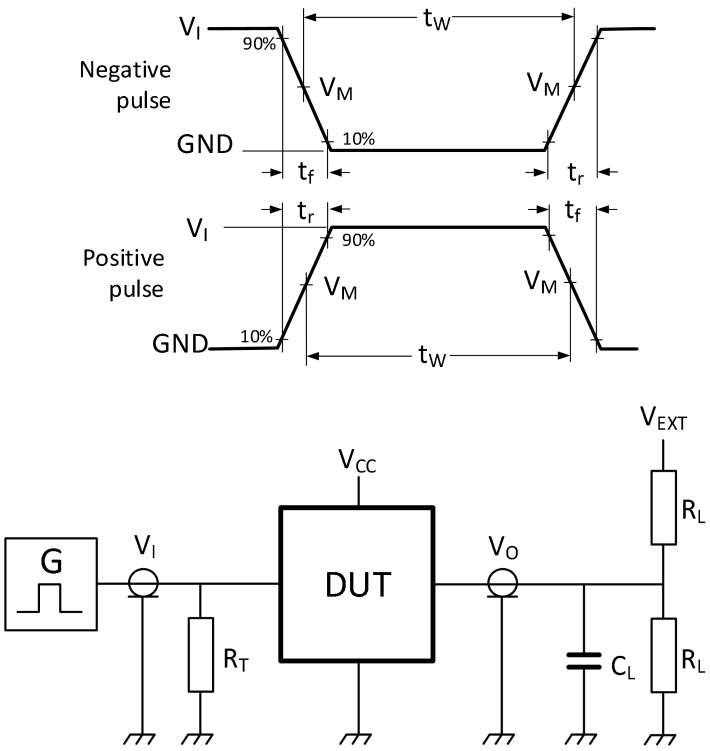


Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. Address input to latch enable input set-up and hold times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC259	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9\ V_{CC}$
74HCT259	1.3 V	1.3 V	$0.1\ V_{CC}$	$0.9\ V_{CC}$



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

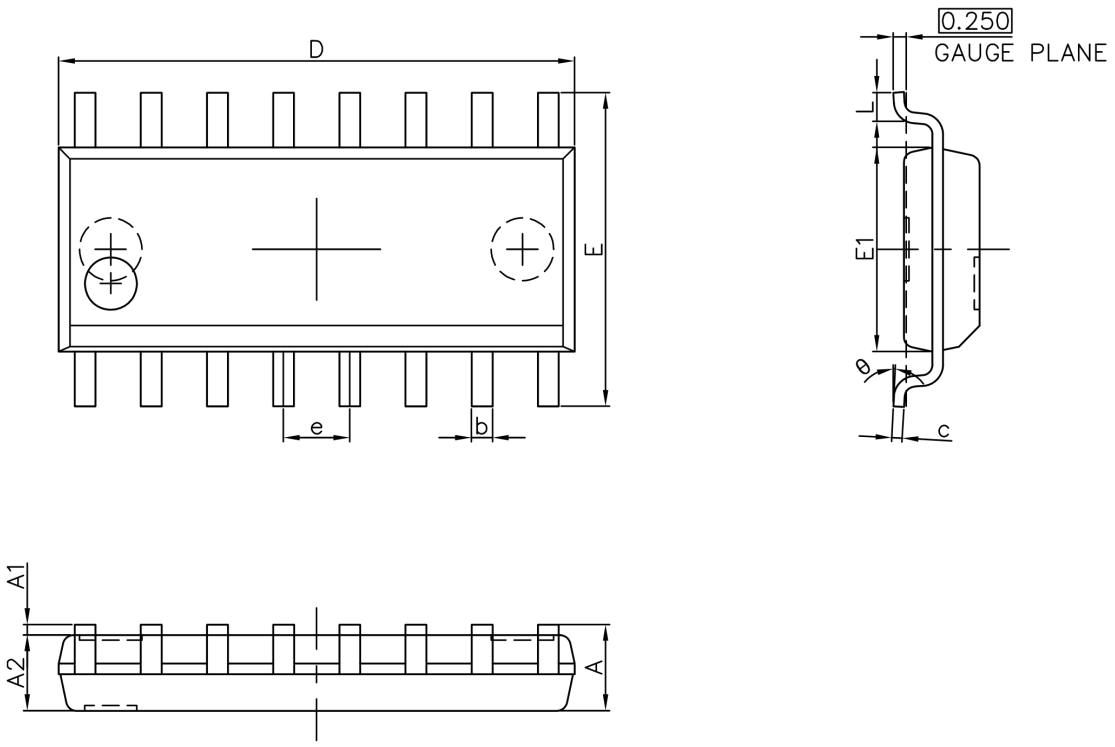
Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		V_{EXT}
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
74HC259	V_{CC}	2.0 ns	50 pF	500 Ω	open
74HCT259	3 V	2.0 ns	50 pF	500 Ω	open

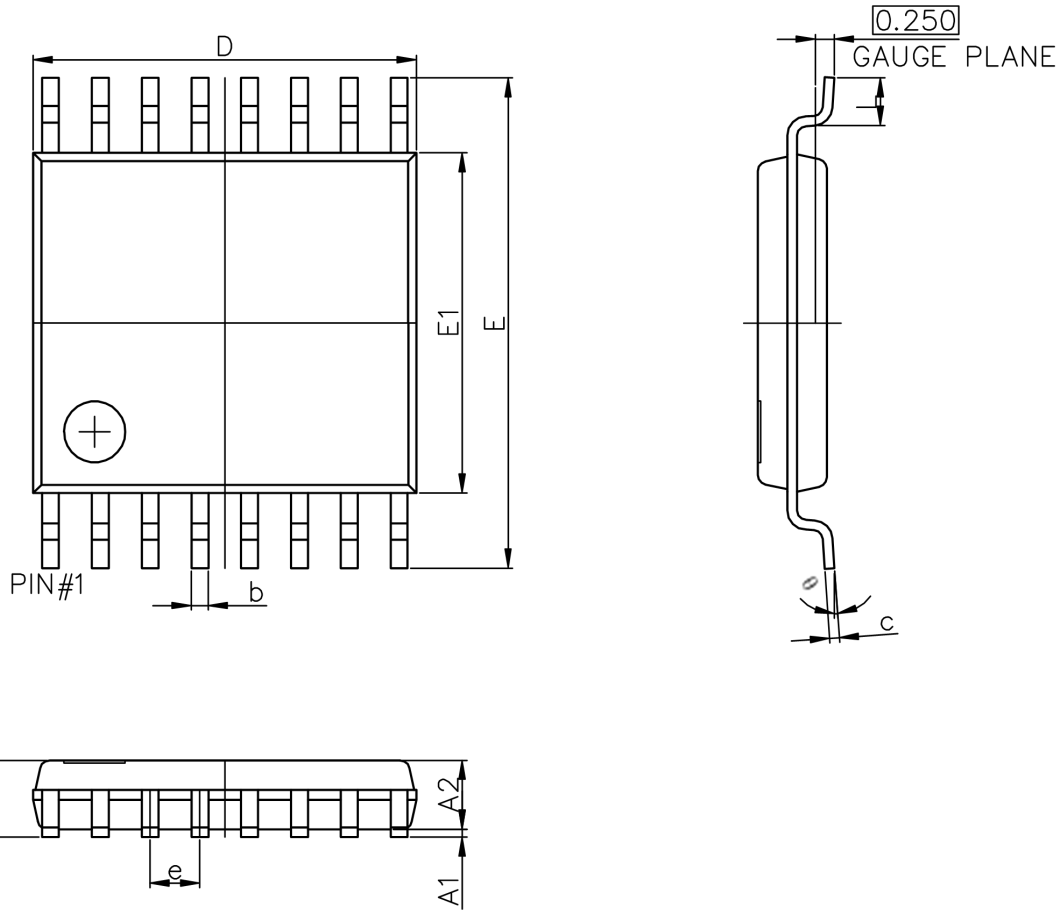
11. Package Outline

SOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.750	——	0.069
A1	0.150	0.250	0.006	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
e	1.270(BSC)		0.050(BSC)	
E	5.900	6.100	0.232	0.240
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	—	1.200	—	0.047
A1	0.020	0.100	0.001	0.004
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT259 Rev. 1.0	Aug 08, 2024	Product datasheet		