# Lens Driver IC for camcorder and security-camera

## Chip description：

The GC6208 is a lens motor driver IC for camcorder and security-camera .

This device integrates a DC motor driver for Iris which controlled by PID system， and also has two channels STM motor drivers for zoom and focus control。

## Chip application：

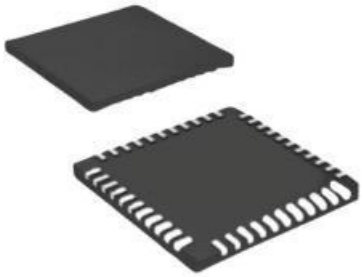
Camcorder

Security-camera

Consumer Products

Robotics

Medical Devices



## Chip features：

Built in DC motor driver for Iris controller

Built in 2 STM driver for zoom and focus

256 u-step driving technology for STM， features supper low noise

2 systems of open-drain for driving LED

Over temperature protection

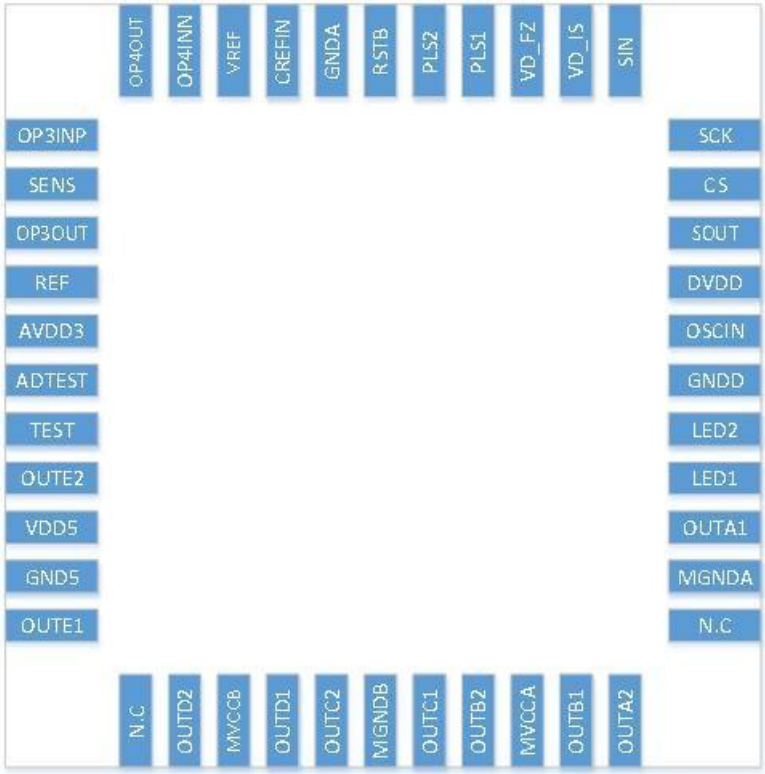
QFN44(06x06) Package

| Product name | Package Type | Detail description |
|---|---|---|
| GC6208 | QFN44 | 6.0*6.0， e=0.4 |

**Packaging Introduction**

| Per Tray | Per Box | Per Case |
|---|---|---|
| 4K | 8K | 64K |

## Pin Map：

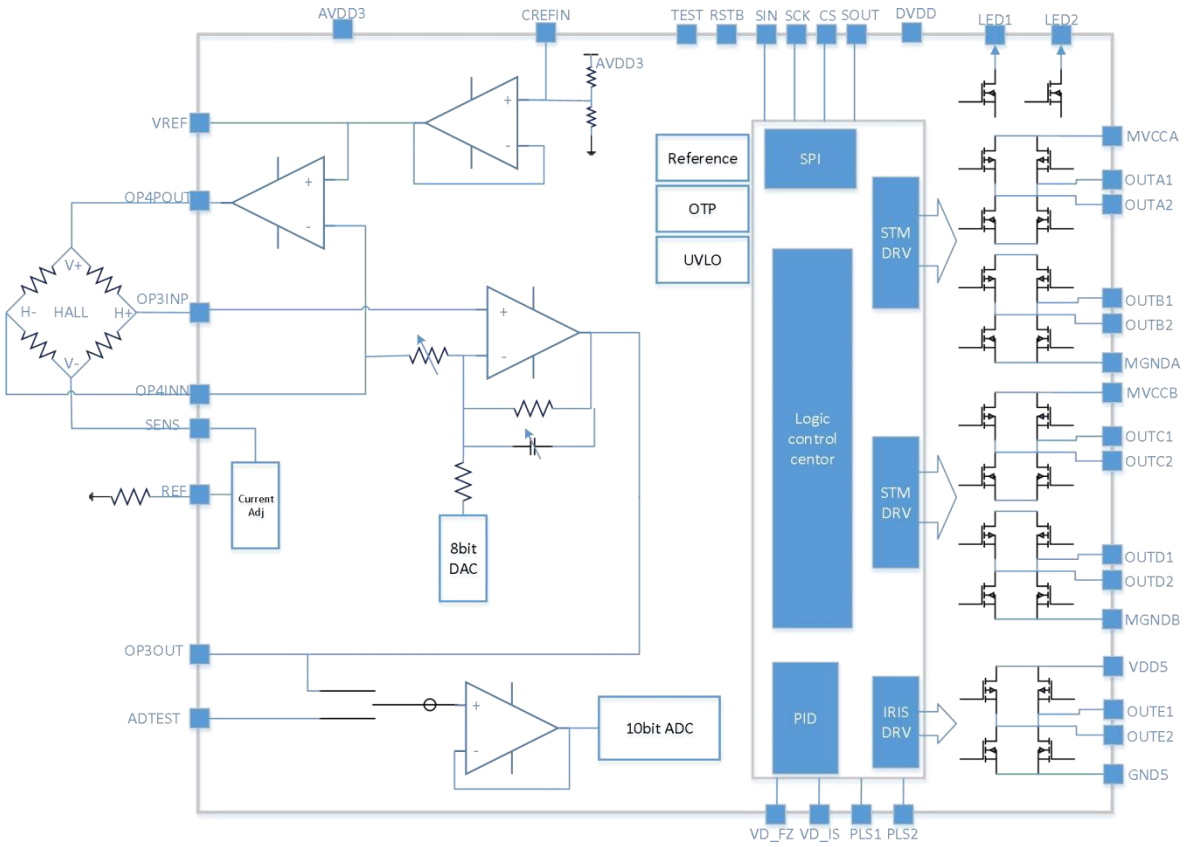



## Pin Description：

| Pin No. | Pin Name | I/O | Pin Function |
|---|---|---|---|
| 1 | OP3INP | I | Hall signal amplifier non-inverting input |
| 2 | SENS | O | Hall current bias |
| 3 | OP3OUT | O | Hall signal amplifier output |
| 4 | REF | IO | Hall current reference setting by resistor connection |
| 5 | AVDD3 | Power | 3.3V Analog power |
| 6 | ADTEST | I | ADC test input |
| 7 | TEST | I | Test mode input |
| 8 | OUTE2 | O | Motor output E2 |
| 9 | VDD5 | Power | Motor power supply |
| 10 | GND5 | gnd | Motor E ground |
| 11 | OUTE1 | O | Motor output E1 |
| 12 | N.C | N.c | No connection inside |
| 13 | OUTD2 | O | Motor output D2 |
| 14 | MVCCB | Power | Motor B supply |

| | | | |
|---|---|---|---|
| 15 | OUTD1 | O | Motor output D1 |
| 16 | OUTC2 | O | Motor output C2 |
| 17 | MGNDB | Gnd | Motor B ground |
| 18 | OUTC1 | O | Motor output C1 |
| 19 | OUTB2 | O | Motor output B2 |
| 20 | MVCCA | ground | Motor A ground |
| 21 | OUTB1 | O | Motor output B1 |
| 22 | OUTA2 | O | Motor output A2 |
| 23 | N.C | N.c | No connection inside |
| 24 | MGNDA | Gnd | Motor A ground |
| 25 | OUTA1 | O | Motor output A1 |
| 26 | LED1 | O | LED1 OUT (open drain) |
| 27 | LED2 | O | LED2 OUT (open drain) |
| 28 | GNDD | Gnd | Ground pin for digital circuit |
| 29 | OSCIN | I | System clock input |
| 30 | DVDD | Power | Digital power supply |
| 31 | SOUT | O | SPI output |
| 32 | CS | I | SPI chip select |
| 33 | SCK | I | SPI clock input |
| 34 | SIN | I | SPI data in |
| 35 | VD_IS | I | Sync signal input for Iris |
| 36 | VD_FZ | I | Sync signal input for zoom&focus |
| 37 | PLS1 | O | Pulse 1 output |
| 38 | PLS2 | O | Pulse 2 output |
| 39 | RSTB | I | Reset signal input |
| 40 | GNDA | Gnd | Ground pin for analog |
| 41 | CREFIN | IO | AVDD3/2 capacitor connection pin |
| 42 | VREF | O | Reference voltage for Hall sense |
| 43 | OP4INN | I | Amplifier 4 no-inverting input |
| 44 | OP4OUT | O | Amplifier 4 output |

## Block Diagram ：




## Absolute Maximum Ratings：

(over operating free-air temperature range (unless otherwise noted)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| AVDD3 | Analog supply voltage | -0.3~4.0 | V |
| DVDD | Digital supply voltage | -0.3~4.0 | V |
| MVCCA/B | STM motor supply voltage | -0.3~6.0 | V |
| VDD5 | DC motor supply voltage | -0.3~6.0 | V |
| Topr | Operating ambient temperature | -40~100 | ℃ |
| Tstg | Storage temperature | -55~125 | ℃ |
| Istm | STM motor current | 0.8 | A |
| Idc | DC motor current | 0.3 | A |
| LED | LED pull down current | 30 | mA |
| ESD | Human Body Model | 3000 | V |

## Electrical Characteristics：

Recommended Operating Conditions

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Motor power supply | MVCCA,MVCCB,VDD5 | | 3.0 | 5 | 5.5 | V |
| Analog&Logic power supply | AVDD3,DVDD | | 2.7 | 3.3 | 3.6 | V |
| Logic input Range | Vlogicin | TEST,OSCIN,CS,SCK,SIN,VD_IS,VD_FZ,RSTB | -0.3 | | DVDD+0.3 | V |
| Logic output Range | Vlogicout | PLS1,PLS2,SOUT | -0.3 | | DVDD+0.3 | V |
| Analog output Range | VAnalogout | OP3OUT,OP4OUT,SENS,VREF | -0.3 | | AVDD+0.3 | V |
| Motor current | ISTM | OUTA1,OUTA2,OUTB1,OUTB2,OUTC1,OUTC2,OUTD1,OUTD2 | -0.25 | | +0.25 | A |
| | IDC | OUTE1,OUTE2 | -0.15 | | 0.15 | A |
| External constants | CVREF | | | 100 | | pF |
| | CREFIN | | | 0.1 | | uF |
| | RREF | | | 10 | | kΩ |
| | COP3INP | | | 0.01 | | uF |
| | COP4OUT | | | 0.1 | | uF |

Electrical Characteristics：(unless otherwise specified , T=25℃， DVDD=AVDD=3.3V， MVCCx=VDD5=5V）

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| MVCC current on Reset | Ivreset | No load, no 27MHz inputs,RSTB=0 | | 0 | 2.0 | uA |
| MVCC current | Ivmon | Output open， RSTB=1 | | 0.5 | 15 | mA |
| DVDD,AVDD standby current | Ivddreset | no 27MHz inputs, RSTB=0 | | 0 | 10 | uA |
| DVDD,AVDD current | Ivddon | No load,RSTB=1 | | 7 | 20 | mA |
| VDD5 standby current | Ivdd5reset | no 27MHz inputs, RSTB=0 | | 0 | 10 | uA |
| VDD5 current | Ivdd5on | No load,RSTB=1 | | 0.3 | 1 | mA |
| **STM OUT H-bridge driver (focus&zoom)** | | | | | | |

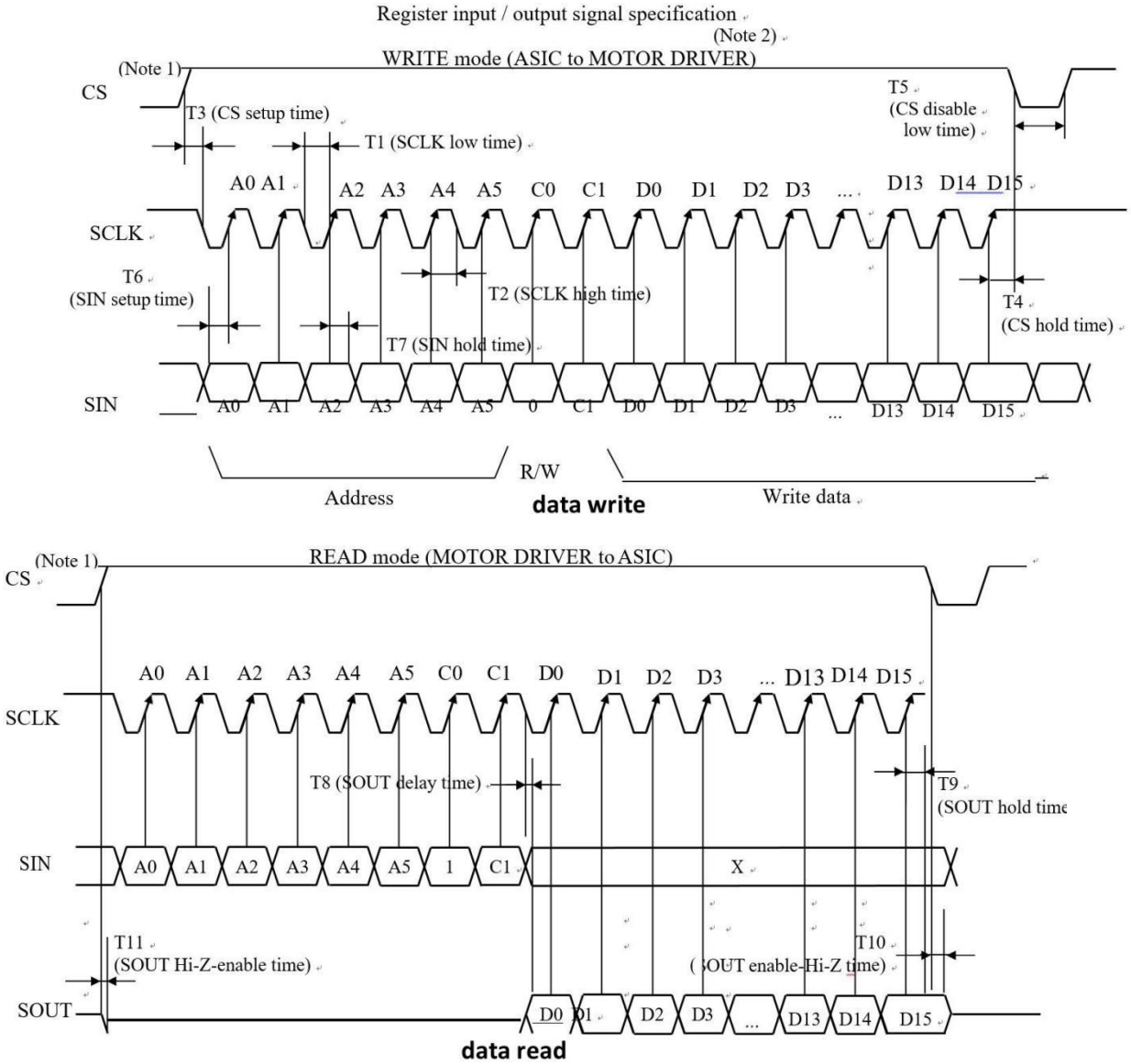
| | | | | | | |
|---|---|---|---|---|---|---|
| Rdson,up+down4 | RdsON1 | Io=100mA;T=25° | | 1.5 | 2.5 | Ω |
| When off leakage current | IOFF1 | Vout=0V | -10 | | 10 | uA |
| **DC OUT H-bridge driver (Iris)** | | | | | | |
| Rdson,up+down | RdsON2 | Io=100mA;T=25° | | 2.0 | 3.0 | Ω |
| When off leakage current | IOFF2 | Vout=0V | -10 | | 10 | uA |
| **LED DRIVERS** | | | | | | |
| Output on resistance | Rdson3 | | | | 5 | Ω |
| When off leakage current | IOFF2 | | -10 | | 10 | uAs |
| **Logic inputs/output** | | | | | | |
| Input logic-low voltage | $V_{IL}$ | TEST,OSCIN,CS,SCK,SIN ,VD_IS,VD_FZ,RSTB | -0.3 | 1.02 | 0.35*DV DD | V |
| Input logic-high voltage | $V_{IH}$ | TEST,OSCIN,CS,SCK,SIN ,VD_IS,VD_FZ,RSTB | 0.54*D VDD | 1.36 | DVDD+ 0.3 | V |
| output logic-l voltage | $V_{OH}$ | PLS1,PLS2,SOUT,1mA Sink | | | 0.5 | V |
| Outpu logic-high voltage | $V_{OL}$ | PLS1,PLS2,SOUT,1mA Source | 0.9*DV DD | | | |
| Pulldown resistance | $R_{pd}$ | RSTB | | 100 | | kΩ |
| **PROTECTION CIRCUITS** | | | | | | |
| Over temperature protection | TSD | | 155 | 169 | 180 | ℃ |
| Over temperature protection hysteresis | ΔTSD | | | 26 | | ℃ |
| Under voltage lockout | $V_{UVLO1}$ | DVDD,AVDD | | 2.27 | | V |
| Under voltage lockout hysteresis | $\Delta V_{UVLO1}$ | DVDD,AVDD | | 0.2 | | V |
| Under voltage lockout | $V_{UVLO2}$ | MVCCA,MVCCB,VDD5 | | 2.20 | | V |
| Under voltage lockout hysteresis | $\Delta V_{UVLO2}$ | MVCCA,MVCCB,VDD5 | | 0.2 | | V |
| **OPAMP3 (HALL Sensor amplifier for output amplifier)** | | | | | | |
| Input voltage range | Vinop3 | - | 0.5*AV DD-0.5 | 0.5*AV DD | 0.5*AV DD+0.5 | V |
| Input offset voltage | VOF3 | - | -15 | - | 15 | mV |
| Output voltage(low) | VOL3 | ILOAD=-100uA | - | 0.1 | 0.2 | V |
| Output voltage(high) | VOH3 | ILOAD=100uA | AVDD -0.2 | AVDD -0.1 | - | V |
| Gain | VOG | Gain register set value：0h | 19.7 | 21.9 | 24.1 | V/V |
| **OP4AMP4（HALL sensor amplifier for eliminating common-mode voltage）** | | | | | | |
| Input voltage range | Vinop4 | - | 0.5*AV DD-0.1 | 0.5*AV DD | 0.5*AV DD+0.1 | V |
| Input offset voltage | VOF4 | - | -10 | - | 10 | mV |
| Output voltage(low) | VOL4 | ILOAD=-100uA | - | 0.1 | 0.2 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| Output voltage(high) | $V_{OH4}$ | $I_{LOAD}$=100uA | AVDD -0.5 | AVDD -0.2 | - | V |
| **Reference output** | | | | | | |
| Output voltage 1 | VREF | VCREF=100pF；ILOAD=0A | 0.5*AVDD-0.1 | 0.5*AVDD | 0.5*AVDD+0.1 | V |
| Output voltage 1 | VREFL | VCREF=100pF；ILOAD=100uA | VREF -0.1 | VREF | VREF +0.1 | V |
| **Hall bias controller（SENS output）** | | | | | | |
| Minutes output current | $IB_L$ | REF=10kΩ，SENS=0.7V，set value:00h | - | 0 | 0.1 | mA |
| Output current accuracy1 | IB 40H | REF=10kΩ，SENS=0.7V，set value:40h | 0.9 | 1.02 | 1.14 | mA |
| Output current accuracy2 | IB BEH | REF=10kΩ，SENS=0.7V，set value:BEh | 2.66 | 3.02 | 3.38 | mA |
| **8bit DAC for Hall offset adjustment** | | | | | | |
| Adjustment range high | DAoutH | - | | AVDD3 | | V |
| Adjustment range high | DAoutL | - | | 0 | | V |
| **10bit ADC** | | | | | | |
| Input voltage range high | $V_{inhigh}$ | - | - | - | AVDD3 -0.2 | V |
| Input voltage range low | $V_{inlow}$ | - | 0.2 | - | - | V |
| Differential linearity error | DNL | - | - | 1.0 | - | LSB |
| Intergral linearity error | INL | | - | 2.0 | - | LSB |

# Function description

## (1) Serial interface

**Timing chart:**




TA = 25°C, VCC = 5 V, RL = 20 Ω

| Parametr | contidtion | range | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SPI Speed | Serial clock | 1 | 5 | MHz |
| T1 | SCLK low time | 100 | - | ns |
| T2 | SCLK high time | 100 | - | ns |
| T3 | CS setup time | 60 | - | ns |

| | | | | |
|---|---|---|---|---|
| T4 | CS hold time | 60 | | ns |
| T5 | CS disable low time | 100 | | ns |
| T6 | SIN setup time | 50 | | ns |
| T7 | SIN HOLD time | 50 | - | ns |
| T8 | SOUT delay time | - | 60 | us |
| T9 | SOUT hold time | 60 | | ns |
| T10 | SOUT enable-Hiz time | - | 60 | ns |
| T11 | SOUT Hiz-enable time | - | 60 | ns |
| Cload | SOUT Capacitor load | - | 40 | pF |

## (2) register map

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00H | | | | | | | IRS_TGT[9:0] | | | | | | | | | |
| 01H | DGAIN[6:0] | | | | | | | ASOUNDLPF_FC[2:0] | | | AS_FLT_OFF | DEC_AVE | OVER_LPF_FC_2ND[1:0] | | OVER_LPF_FC_1ST[1:0] | |
| 02H | PID_POLE[3:0] | | | | PID_ZERO[3:0] | | | | IRIS_ROUND[3:0] | | | | IRIS_CALC_NR[3:0] | | | |
| 03H | | | DT_ADJ_IRIS[1:0] | | PWM_IRIS[2:0] | | | PWM_LPF_FC[2:0] | | | PWM_FLTOFF | LMT_ENB | ARW[3:0] | | | |
| 04H | HALL_OFFSET_DAC[7:0] | | | | | | | | HALL_BIAS_DAC[7:0] | | | | | | | |
| 05H | | | | AAF_FC | HALL_GAIN[3:0] | | | | | | PID_INV | TGT_FLT_OFF | TGT_LPF_FC[3:0] | | | |
| 06H | | | | | | | START1[9:0] | | | | | | | | | |
| 07H | P1EN | | | | WIDTH1[11:0] | | | | | | | | | | | |
| 08H | | | | | | | START2[9:0] | | | | | | | | | |
| 09H | P2EN | | | | | | | | | | WIDTH2[5:0] | | | | | |
| 0AH | | | | | | DUTY_TEST | TGT_IN_TEST[9:0] | | | | | | | | | |
| 0BH | PID_CLIP[3:0] | | | | ADC_TEST | PDWNB | MODESEL_FZ | MODESEL_IRIS | TESTEN1 | | | ASWMODE[1:0] | | | | |
| 0CH | | | | | | | IRSAD[9:0] (Read Only) | | | | | | | | | |
| 0EH | | | | AVE_SPEED[4:0] | | | | | TGT_UPDATE[7:0] | | | | | | | |
| 20H | | PWMRES[1:0] | | PWMMODE[4:0] | | | | | DT1[7:0] | | | | | | | |
| 21H | | | | | | | | | TESTEN2 | | | FZTEST[4:0] | | | | |
| 22H | | | PHMODAB[5:0] | | | | | | DT2A[7:0] | | | | | | | |
| 23H | PPWB[7:0] | | | | | | | | PPWA[7:0] | | | | | | | |
| 24H | | | MICROAB[1:0] | | LEDB | ENDISAB | BRAKEAB | CCWCWAB | PSUMAB[7:0] | | | | | | | |
| 25H | INTCTAB[15:0] | | | | | | | | | | | | | | | |
| 27H | | | PHMODCD[5:0] | | | | | | DT2B[7:0] | | | | | | | |
| 28H | PPWD[7:0] | | | | | | | | PPWC[7:0] | | | | | | | |
| 29H | | | MICROCD[1:0] | | LEDA | ENDISCD | BRAKECD | CCWCWCD | PSUMCD[7:0] | | | | | | | |
| 2AH | INTCTCD[15:0] | | | | | | | | | | | | | | | |

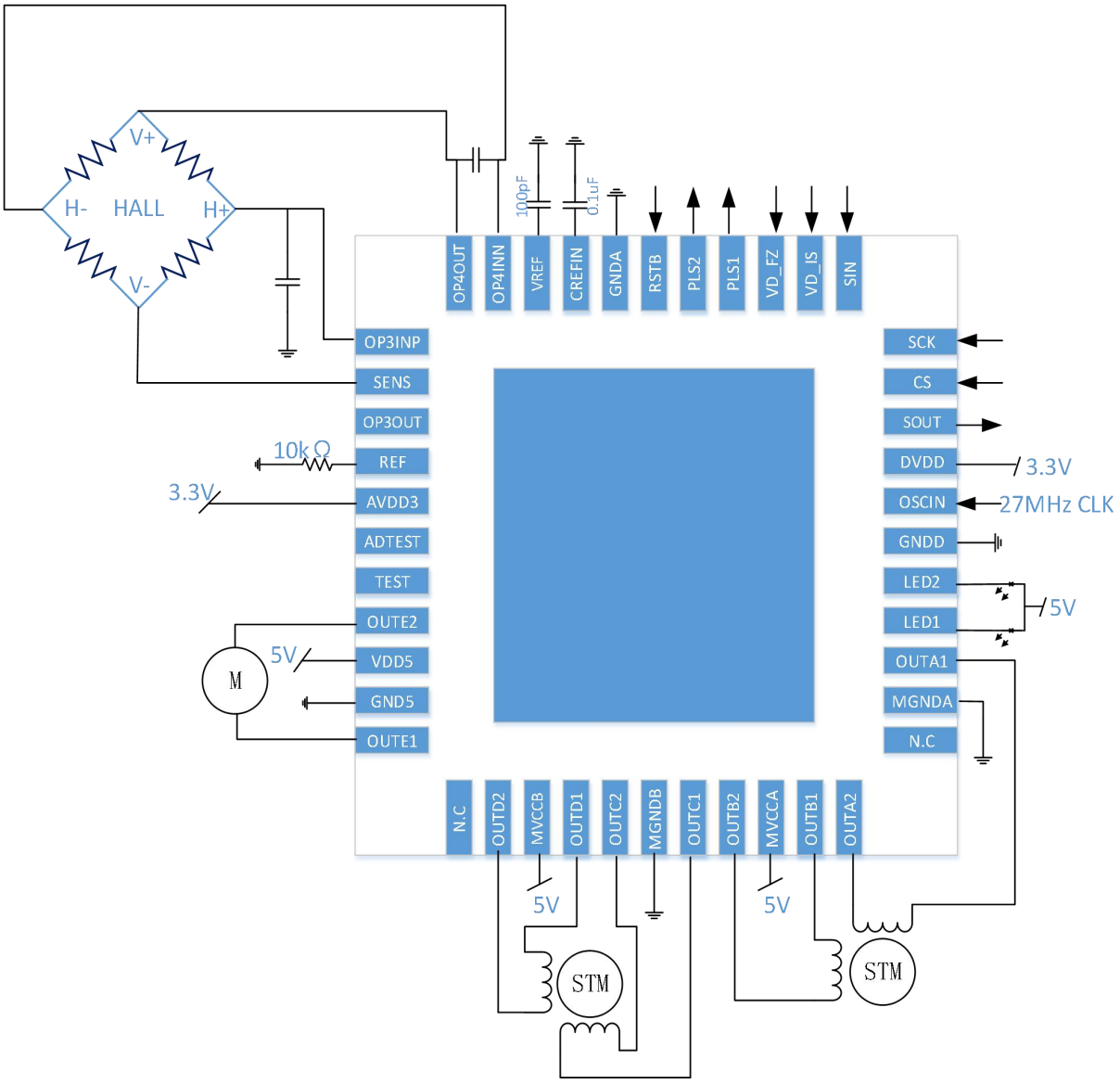
## (3) register description

| Address | Register | Function | |
|---|---|---|---|
| 00h | IRS_TGT[9:0] | Iris target positon Expressed in 10 bit digits | |
| 01h | OVER_LPF_FC_1ST[1:0 ] | ADC feedback filter (1) cut-off frequency | |
| | OVER_LPF_FC_2ND[1: 0] | ADC feedback filter (2) cut-off frequency | |
| | DEC_AVE | Moving average to Iris target position | |
| | AS_FLT_OFF | Filter before PID controller enable / disable | |
| | ASOUND_LPF_FC[2:0] | Filter cut-off frequency before PID controller | |
| | DGAIN[6:0] | PID controller digital gain | |
| 02h | IRIS_CALC_NR[3:0] | PID integral error cumulative prevention level | |
| | IRIS_ROUND[3:0] | PID differential error cumulative prevention level | |
| | PID_ZERO[3:0] | PID controller zero point | |
| | PID_POLE[3:0] | PID controller pole | |
| 03h | ARW[3:0] | Number of bits in PID controller integrator | |
| | LMT_ENB | PID controller integral stop | |
| | PWM_FLT_OFF | LPF after PID controller enable / disable | |
| | PWM_LPF_FC[2:0] | LPF cut-off frequency after PID controller | |
| | PWM_IRIS[2:0] | PWM frequency of Iris block output | |
| | DT_ADJ_IRIS[1:0] | Dead time correction of Iris block output | |
| 04h | HALL_BIAS_DAC[7:0] | Drive current value for hall element | |
| | HALL_OFFSET_DAC[7: 0] | Offset adjustment for hall element output amplifier | |
| 05h | TGT_LPF_FC[3:0] | Iris target value LPF cut-off frequency | |
| | TGT_FLT_OFF | Iris target value LPF function enable / disable | |
| | PID_INV | PID controller polarity | |
| | HALL_GAIN[3:0] | Hall element output amplifier gain | |
| | AAF_FC | Cut-off frequency of hall element output amplifier | |
| 06h | START1[9:0] | Pulse 1 start time | |
| 07h | WIDTH1[11:0] | Pulse 1 width | |
| | P1EN | Pulse 1 output enable | |
| 08h | START2[9:0] | Pulse 2 start time | |
| 09h | WIDTH2[5:0] | Pulse 2 width | |

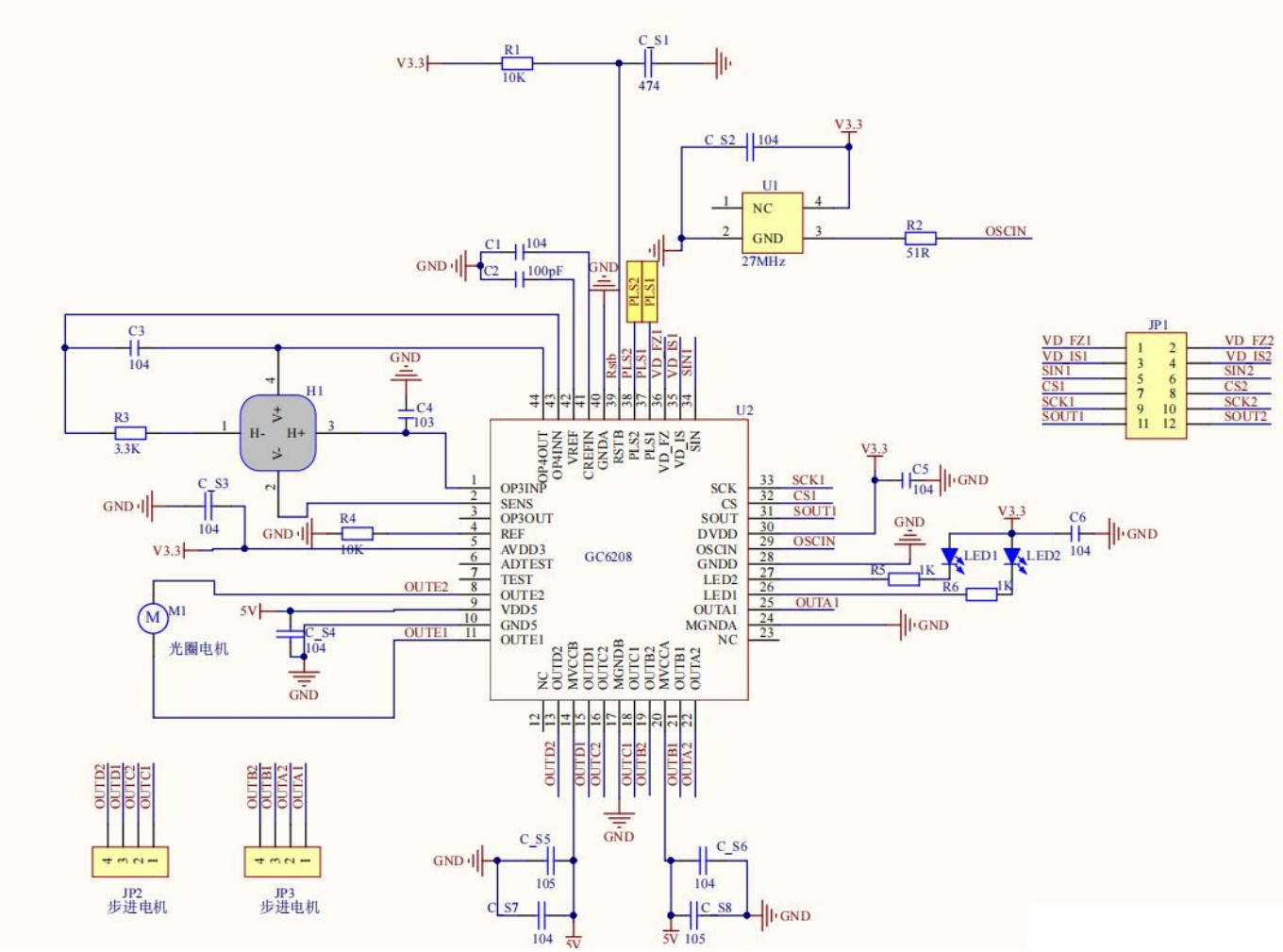
| | | | |
|---|---|---|---|
| | P2EN | Pulse 2 output enable | |
| 0Ah | TGT_IN_TEST[9:0] | Iris output duty direct specified value | |
| | DUTY_TEST | Iris output duty direct specification enable | |
| 0Bh | ASWMODE[1:0] | ADTESTIN pin connection selection | |
| | TESTEN1 | Test mode enable 1 | |
| | MODESEL_IRIS | VD_IS polarity selection | |
| | MODESEL_FZ | VD_FZ polarity selection | |
| | PDWNB | Power down of Iris block | |
| | ADC_TEST | ADC read value updated timing | |
| | PID_CLIP[3:0] | Iris output PWM maximum duty | |
| 0Ch | IRSAD[9:0] | ADC output for Iris (read only) | |
| 0Eh | TGT_UPDATE[7:0] | IRS_TGT (iris target) update delay time | |
| | AVE_SPEED[4:0] | Iris target moving average speed | |
| 20h | DT1[7:0] | Start point wait time | |
| | PWMMODE[4:0] | Micro step output PWM frequency | |
| | PWMRES[1:0] | Micro step output PWM resolution | |
| 21h | FZTEST[4:0] | PLS1/2 pin output signal selection | |
| | TESTEN2 | Test mode enable 2 | |
| 22h | DT2A[7:0] | α motor start point excitation wait time | |
| | PHMODAB[5:0] | αmotor phase correction | |
| 23h | PPWA[7:0] | Driver A peak pulse width | |
| | PPWB[7:0] | Driver B peak pulse width | |
| 24h | PSUMAB[7:0] | α motor step count number | |
| | CCWCWAB | α motor rotation direction | |
| | BRAKEAB | α motor brake | |
| | ENDISAB | α motor enable/disable control | |
| | LEDB | LED B output control | |
| | MICROAB[1:0] | α motor sine wave division number | |
| 25h | INTCTAB[15:0] | α motor step cycle | |
| 27h | DT2B[7:0] | β motor start point excitation wait time | |
| | PHMODCD[5:0] | β motor phase correction | |
| 28h | PPWC[7:0] | Driver C peak pulse width | |
| | PPWD[7:0] | Driver D peak pulse width | |
| 29h | PSUMCD[7:0] | β motor step count number | |
| | CCWCWCD | β motor rotation direction | |

| | | | |
|---|---|---|---|
| | BRAKECD | β motor brake | |
| | ENDISCD | β motor enable/disable control | |
| | LEDA | LED A output control | |
| | MICROCD[1:0] | β motor sine wave division number | |
| 2Ah | INTCTCD[15:0] | β motor step cycle | |

## Typical Application




GC6208 typical application



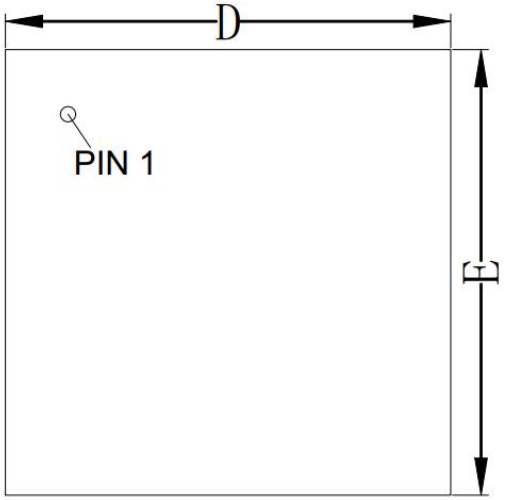

**GC6208 PCB schematic**

Note：R3 connected to pin 43 is used to reduce the gain of hall amplifier ：

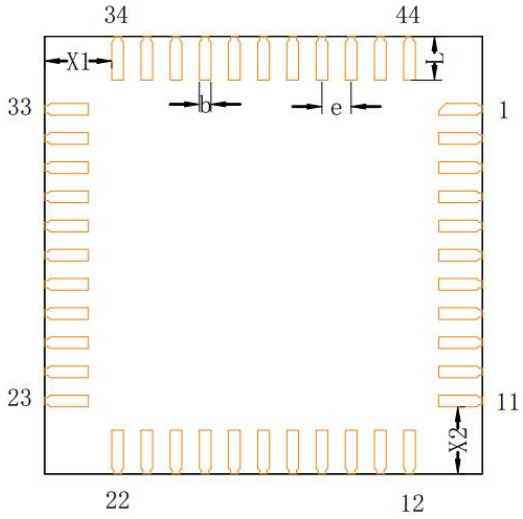
Real Gain=260/[（256/Gain_set）+R3]　　（R3 unit：KΩ）

This resistor is not recommended to be too large.

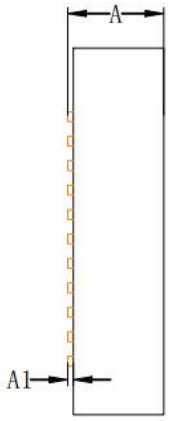
## Package Information




TOP view




Bottom view




Side view

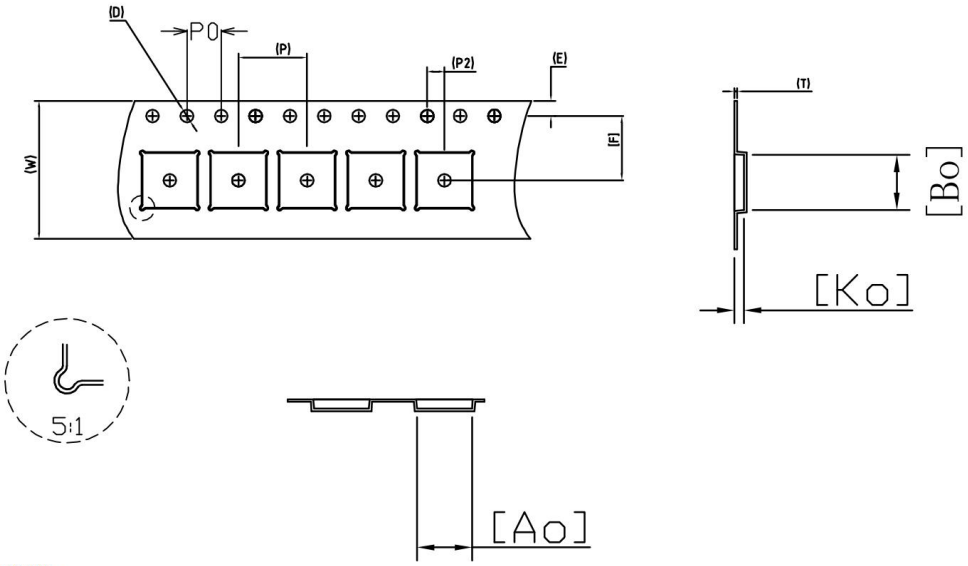
| SYMBOLS | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.700 | 0.750 | 0.800 |
| A1 | 0.007 | 0.012 | 0.017 |
| D | 5.900 | 6.000 | 6.100 |
| E | 5.900 | 6.000 | 6.100 |
| L | 0.550 | 0.600 | 0.650 |
| b | 0.110 | 0.160 | 0.210 |
| e | 0.350 | 0.400 | 0.450 |
| X1 | 0.870 | 0.920 | 0.970 |
| X2 | 0.870 | 0.920 | 0.970 |

## Package quantity

| | Per Tray | Per Box | Per Case |
|---|---|---|---|
| GC6208 | 4K | 8K | 64K |

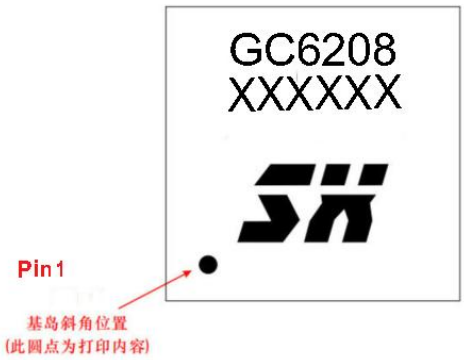
## Packaging Introduction for GC6208

| ITEM | W | A0 | B0 | D | E | F | K0 | P0 | P2 | P | T |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DIM | 16.0 | 6.30 | 6.30 | 1.5 | 1.75 | 7.50 | 1.10 | 4.0 | 2.0 | 8.0 | 0.30 |
| TOLE | +0.3 −0.3 | ±0.10 | ±0.10 | +0.1 −0.0 | ±0.1 | ±0.10 | ±0.10 | ±0.1 | ±0.1 | ±0.1 | ±0.05 |




NOTE:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE±0.2
2. CARRIER CAMBER IS 1MM IN 100MM
3. A0 AND B0 MEASURED ON A PLANCE 0.3MM ABOVE THE BOTTOM OF THE POCKET
4. K0 MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
5. ALL DIMENSIONS MEET EIA-481-B REQUIREMENTS
6. PACKING LENGTH PER 13″REEL : 1.1 METERS
7. COMPONENT LOAD PER 13″ REEL : 4625 PCS

## Description of Lot Code




Printing instructions：

1.The first line GC6208 represents the product model；

2.The second line represents the traceability code；

## Release Notes

| Revision | Description |
|---|---|
| 1.0 | Initial version； |
| 1.1 | Corrected ambiguity in some descriptions ; |
| 1.2 | Added packaging instructions and modified some parameters； |
| 1.3 | Add a note of the application diagram； |
| 1.4 | Changed Packaging Introduction |
| 1.5 | Changed to detail Packaging Introduction |