Lens driver for Digital Still Camera

Chip description：

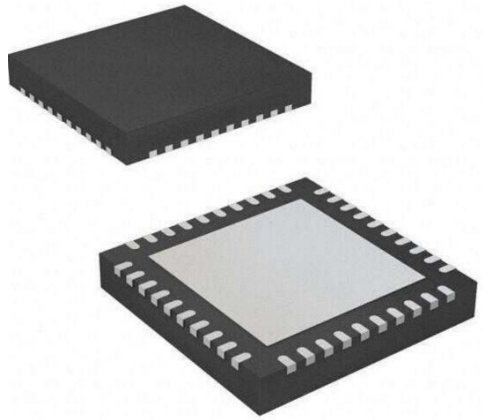
GC6236 is a system Lens Driver that uses μ-step driving to make the configuration of the sophisticated, high precision and low noise lens driver system possible. This IC has a built-in driver for both DC moor and voice coil motor and a μ -step controller that decreases CPU power. Therefore, multifunctional lens can be applied.

Chip application：

- Digital still Cameras
- Shaking head machine

Chip features：

- Built-in 6 Channel H bridge motor drivers
  1ch-4ch: Voltage control type H-bridge
  (Adaptable to STM 2systems)
  5ch: Voltage / Current control type H-bridge
  6ch: Current control type H-bridge
- 0.5A rms current per channel
- Built-in 2 channels PI driver
- Built-in FLL digital servo circuit
- Built-in PLL circuit for variety system clock
- Built-in STM control circuit: Autonomous control (cache / up down mode), Clock IN control

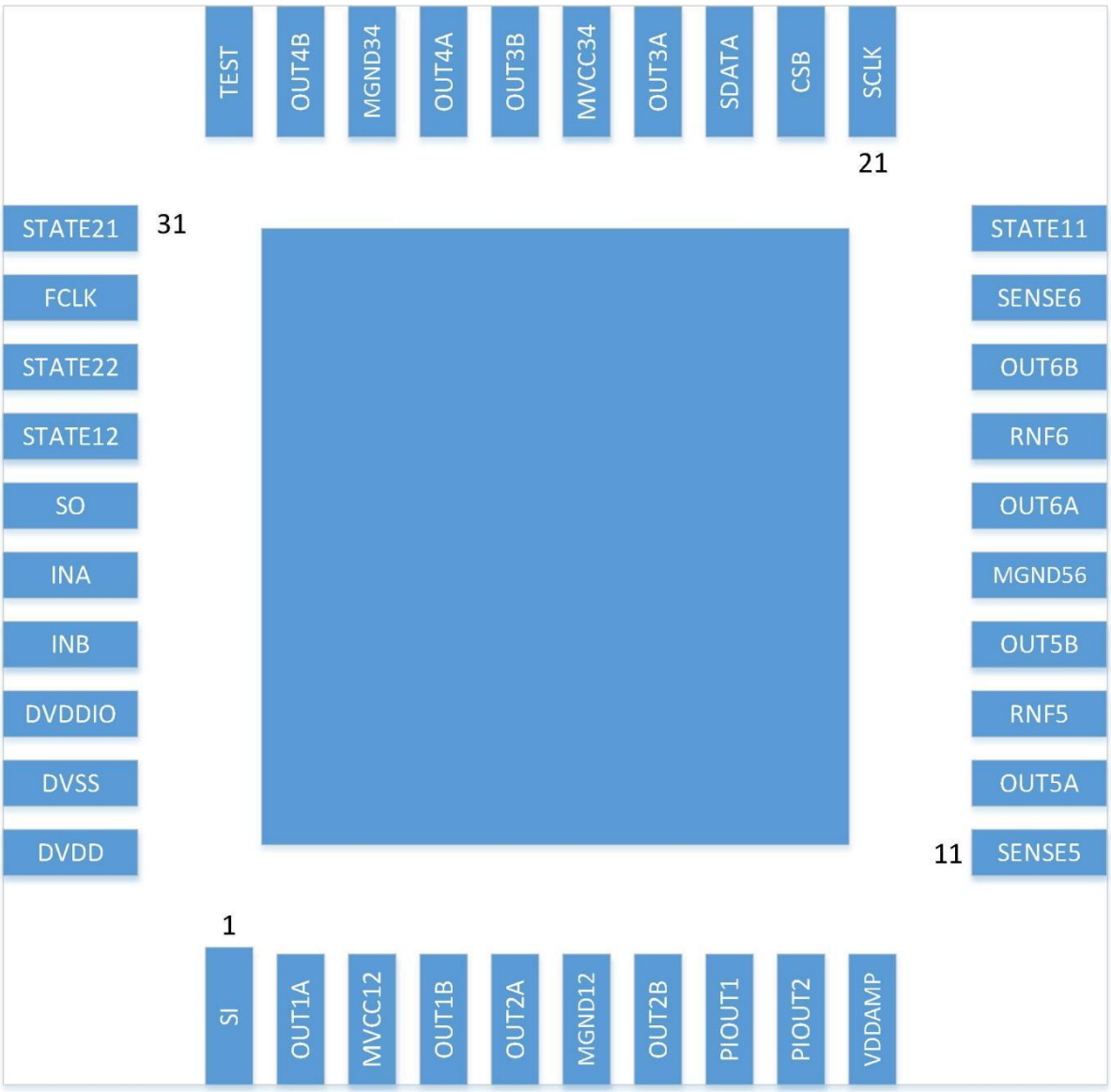


Product name	Package Type	Detail description
GC6236	QFN40	5.0*5.0，e=0.4

Packaging Introduction

Per Tray	Per Box	Per Case
4K	8K	64K

Pin Map:



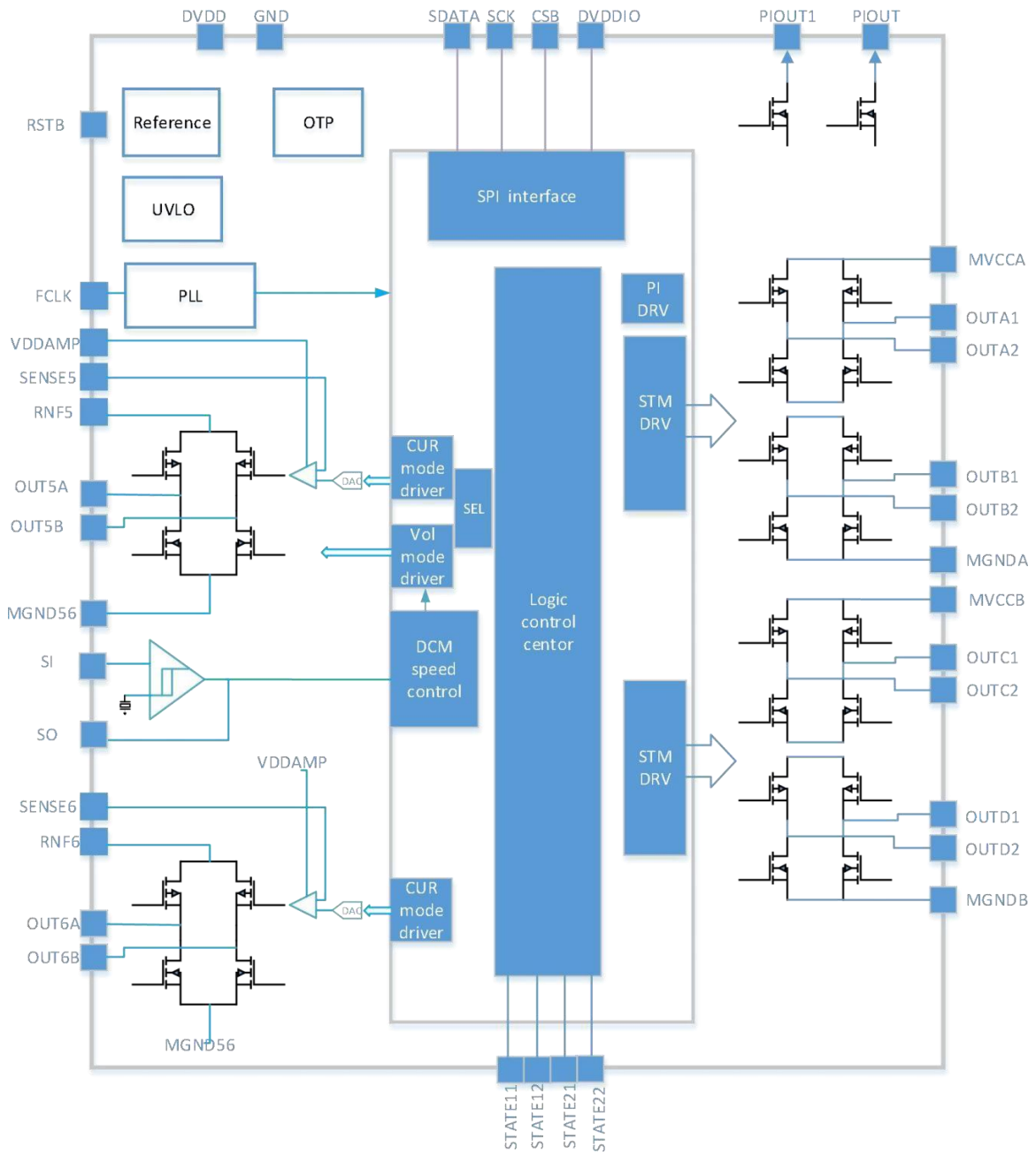
Pin Description:

Pin No.	Pin Name	I/O	Pin Function
1	SI	I	Wave input
2	OUT1A	O	1ch Driver A output
3	MVCC12	POWER	1，2ch power supply

4	OUT1B	O	1ch Driver B output
5	OUT2A	O	2ch Driver A output
6	MGND12	GND	1，2ch GND
7	OUT2B	O	2ch Driver B output
8	PIOUT1	O	PI driver output 1
9	PIOUT2	O	PI driver output 1
10	VDDAMP	POWER	5，6ch Analog power supply
11	SENS5	I/O	5ch sense resister connect
12	OUT5A	O	5ch Driver A output
13	RNF5	I/O	5ch power supply
14	OUT5B	O	5ch Driver B output
15	MGND56	GND	5，6ch GND
16	OUT6A	O	6ch Driver A output
17	RNF6	I/O	6ch power supply
18	OUT6B	O	6ch Driver B output
19	SENSE6	I/O	6ch sense resister connect
20	SATE11	I/O	State11 input/output
21	SCLK	I	SPI clock input
22	CSB	I	SPI CSB input
23	SDATA	I/O	SPI DATA input
24	OUT3A	O	3ch Driver A output
25	MVCC34	POWER	3，4ch power supply
26	OUT3B	O	3ch Driver B output
27	OUT4A	O	4ch Driver A output
28	MGND34	GND	3，4ch GND
29	OUT4B	O	4ch Driver B output
30	TEST	I	TEST logic input
31	STATE21	I/O	State21 input/output
32	FCLK	I	Reference clock input
33	STATE22	O	State22 output
34	STATE12	O	State12 output
35	SO	O	Wave output

36	INA	I	INA logic input
37	INB	I	INB logic input
38	DVDDIO	POWER	IO power supply
39	DVSS	GND	Ditital GND
40	DVDD	POWER	Digital power

Block Diagram ：



Absolute Maximum Ratings:

(over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Rating	Unit
DVDDIO，DVDD	Logic power supply range	-0.3~4.5	V
MVCC	Motor power supply range	-0.3~7	V
VIN	Logic input voltage range	-0.3~V_{DVDDIO}+0.3	V
Irms	Max Rms current，OUTxx	±800	mA
I_{PI}	PIOUTx current	+50	mA
Tjmax	Operating virtual junction temperatures	-40~150	℃
Tstg	Storage Temperature	-60~150	℃
ESD	ESD（HBM）	±4000	V

Electrical Characteristics:

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Motor power supply	MVCC		3.0		5.5	V
Logic power supply	DVDD		2.8		3.6	V
IO power supply	DVDDIO		1.60		3.6	V
Motor current	IOUT		0		0.5	A
Clock operating frequency	FCLK		1		28	MHz
Operating ambient temperature	Ta		-40		100	℃

Electrical Characteristics：(unless otherwise specified , T=25℃，DVDD=DVDDIO=3.3V，MVCCx=5V）

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DVDDIO quiescence current	I_{SSDO}	CMD_RS=0		0	10	uA
DVDD quiescence current	I_{SSD}	CMD_RS=0		50	95	uA
MVCC quiescence current	I_{SSDM}	CMD_RS=0		0	10	uA
DVDDIO operation current	I_{SSOO}	CMD_RS=0		0.1	1	mA
DVDD operation current	I_{SSOD}	CMD_RS=0		6	10	mA
OUT driver						
STM voltage driver 1ch~4ch						
Rdson,up+down	R_{dsON1}	Io=100mA;1ch,2ch		2.0		Ω
	R_{dsON2}	Io=100mA;3ch,4ch		1.5		Ω
When off leakage current	I_{OFF}	Vout=0V	-10		10	uA
Average voltage accuracy	Vdiff	Vdiff setting:2Bh	-5		+5	%

between different output pins						
5ch ,voltage/current driver						
Rdson,up+down	R_{dsON3}	Io=100mA		1.0		Ω
When off leakage current	I_{OFF5}	Vout=0V	-10		10	uA
Output current	I_{out}	At current mode,DAC setting:80h,R_{RNF}=1Ω		200		mA
6ch ,current driver						
Rdson,up+down	R_{dsON3}	Io=100mA		1.0		Ω
When off leakage current	I_{OFF5}	Vout=0V	-10		10	uA
Output current	I_{out}	At current mode,DAC setting:80h,R_{RNF}=1Ω		200		mA
Logic input/output						
Input logic-low voltage falling threshold	V_{IL}		0		0.3* DVDDIO	V
Input logic-high voltage rising threshold	V_{IH}		0.7* DVDDIO		DVDDIO	V
Input logic low current	I_{IL}	Vin=0	0		10	uA
Input logic high current	I_{IH}	Vin=DVDDIO	0		10	uA
Output logic-low	V_{OL}	I=1mA	0		0.2* DVDDIO	V
Output logic-hign	V_{OH}	I=1mA	0.8* DVDDIO		DVDDIO	V
PI Driving circuit						
Output voltage	PI_{VO}	I=30mA		0.15	0.5	V
Waveforming circuit						
Detective voltage error	Vth	Vth setting：20h		1.5		V

Function Description：

Stepping motor driver （1ch~4ch）

Built-in stepping motor driver of PWM driving type.

Maximum 2 stepping motors can be driven independently.

Built-in voltage feedback circuit of D-class type.

3ch/4ch drivers can also drive independently for DC motor or voice coil motor.

STM Control

It corresponds to both the Clock IN and the Autonomous control.

(1) Clock IN Control

Set the registers for the stepping motor control.

The stepping motor is rotated and synchronized with the input clock in the STATE pin.

It is possible to select the mode of stepping motor control from μ -step, 1-2 phase excitation, 2 phase excitation and the number of edge for electrical angle cycle from 4, 8, 32, 64, 128, 256, 512 or 1024.

(2) Autonomous Control

The stepping motor is rotated by setting the registers for the stepping motor control.

It is possible to select the mode of stepping motor control from μ -step (1024 portion), 1-2 phase excitation and 2 phase excitation.

Cache Method:

Built-in Cache registers.Cache registers enable the setting of subsequent process while the motor is in operation. Through these registers,operations are done continuously.The state of rotation command (ACT), state of Cache registers (BUSY), motor operation position (MO), and state ofexcitation (MO&EN) are synchronized with

the motor rotation and can be selected to be the output of the STATE pin.

Up Down Method:

It is possible to set Up, Constant and Down operation before the motor operates.

The state of rotation command (ACT), Cache register (BUSY), motor position (MO), and excitation (MO&EN) synchronized with the motor rotation are the output of the STATE pin.

Voltage / Current Driver (5ch Driver)

Built-in voltage driver of PWM driving type / constant current driver.

Built-in digital FLL speed control logic for voltage driver.

(1) Control

(1)Register Control

■ Voltage Driver (at speed control = OFF)

The PWM drive is executed by the PWM duty ratio, the PWM direction and the PWM ON/OFF which are controlled by the register settings.

■ Voltage Driver (at speed control = ON)

The speed control drive is executed by the target speed value, the direction, the coefficient value of PI filter and the turning ON/OFF which are controlled by the register settings.

The motor speed is adjusted by comparing the target speed with the motor speed detected at the signal of photo-interrupter.

■ Current Driver

The constant current drive is executed by the output current value, the current direction and the current ON/OFF which are controlled by the register settings.

(2)External Pin Control

■ Voltage Driver (only at speed control = OFF)

The PWM drive is executed by the PWM duty ratio which is controlled by the register setting. The PWM direction and PWM ON/OFF are controlled by INA/INB pin.

■ Current Driver

The constant current drive is executed by the output current value which is controlled by the register setting. Constant current driving direction and turning ON/OFF are controlled by INA/INB pin

Current Driver (6ch Driver)

Built-in constant current driver.

The voltage of RNF pin and the external resistor (R_{RNF}) determine the amount of output current. The internal high-precision amplifier (CMOS gate input) is used for the constant current control. If any resistance component exists in the wirings of RNF pin and the external resistor (R_{RNF}), the precision can be reduced. To avoid this, pay utmost attention to the wirings.

(1) Control

(a) Register Control

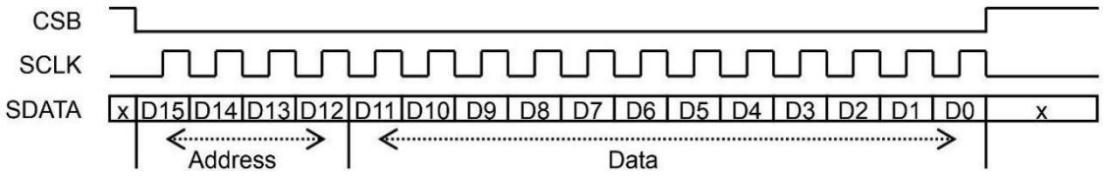
The constant current drive is executed by the output current value, the current direction and the current ON/OFF which are controlled by the register settings.

(b) External Pin Control

The constant current drive is executed by the output current value which is controlled by the register setting. Constant current driving direction and turning ON/OFF are controlled by INA/INB pin.

Serial interface

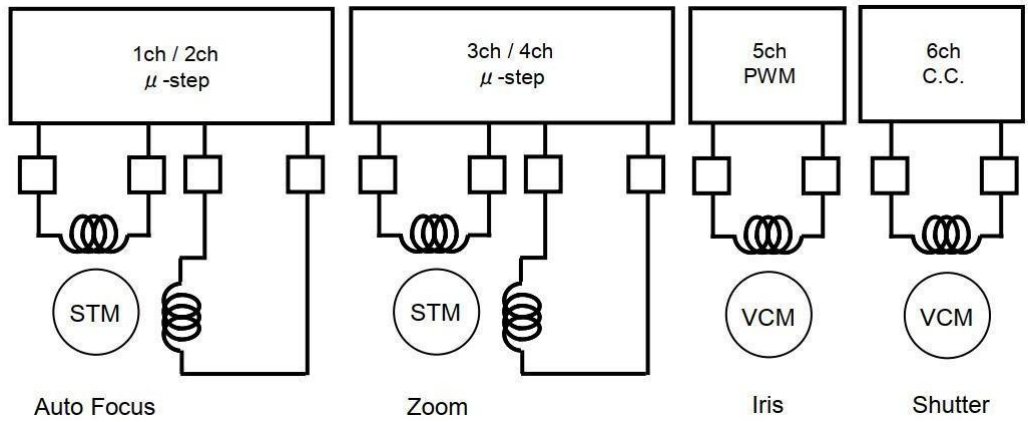
Control commands are framed by a 16-bit serial input (MSB first) and are sent through the CSB, SCLK, and SDATA pins. The 4 higher-order bits specify addresses, while the remaining 12 bits specify data. Data of every bit is sent through SDATA pin, which is retrieved during the rising edge of SCLK. Data becomes valid when CSB is Low and is registered during the rising edge of CSB.

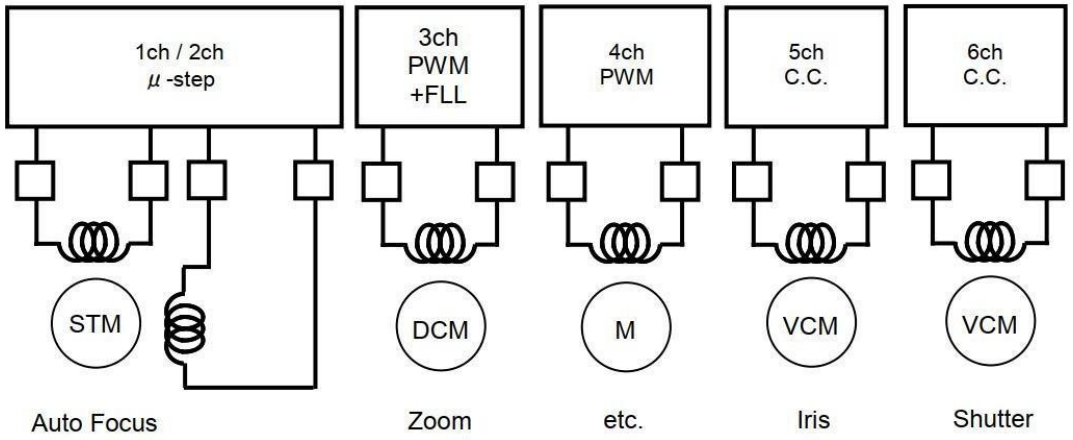


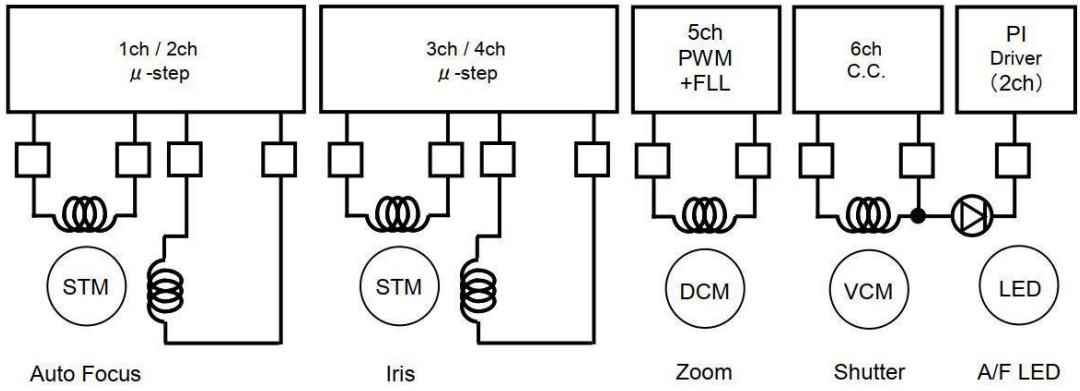
Register map

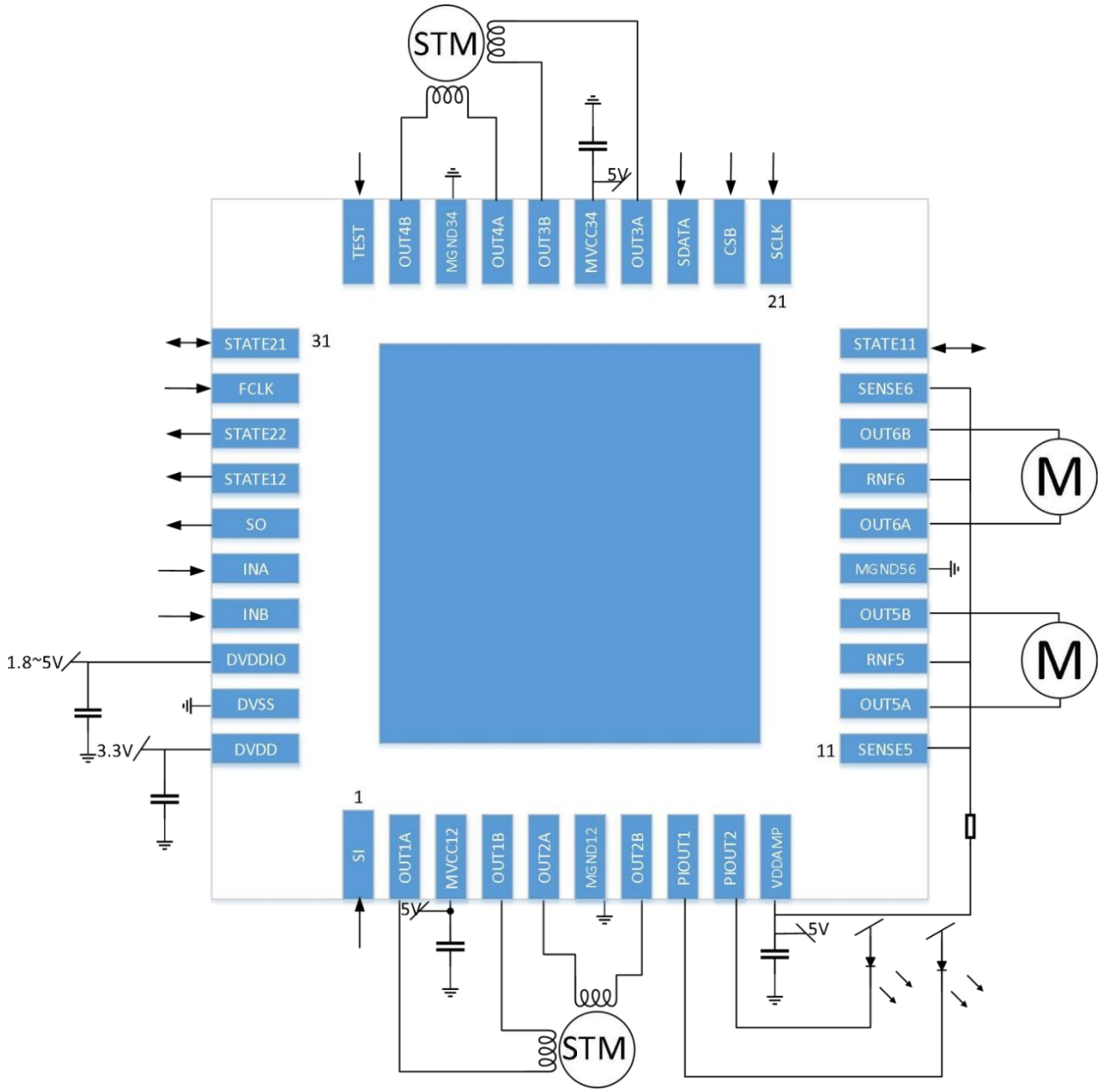
Address[3:0]				Data[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	A_Mode[1:0]		A_SEL[2:0]			A_different_output_voltage[6:0]						
0	0	0	1	0	0	0	0	A_Cycle[5:0]						0	0
				0	0	1	0	A_Cycle[13:6]							
				0	1	0	0	0	0	0	0	A_Start_POS[3:0]			
				0	1	1	0	A_BEXC	0	0	A_BSL	A_AEXC	0	0	A_ASL
				1	1	1	0	0	0	A_POS[1:0]		0	A_UPDW_Stop	A_PS	A_Stop
0	0	1	0	A_EN	A_RT	A_Pulse[9:0] / A_UPDW_Cycle[9:0]									
0	1	0	0	B_Mode[1:0]		B_SEL[2:0]			B_different_output_voltage[6:0]						
0	1	0	1	0	0	0	0	B_Cycle[5:0]						0	0
				0	0	1	0	B_Cycle[13:6]							
				0	1	0	0	0	0	0	0	B_Start_POS[3:0]			
				0	1	1	0	B_BEXC	0	0	B_BSL	B_AEXC	0	0	B_ASL
				1	0	0	0	0	0	3_CHOP[1:0]		0	0	4_CHOP[1:0]	
				1	0	1	3_State_CTL[1:0]		3_PWM_Duty[6:0]						
				1	1	0	4_State_CTL[1:0]		4_PWM_Duty[6:0]						
				1	1	1	0	0	0	B_POS[1:0]		0	B_UPDW_Stop	B_PS	B_Stop
0	1	1	0	B_EN	B_RT	B_Pulse[9:0] / B_UPDW_Cycle[9:0]									
1	0	1	1	0	0	0	0	B_ANSEL	A_ANSEL	Edge	0	0	0	B_CTL	A_CTL
				0	0	1	0	0	0	0	0	0	0	EXT_CTL[1:0]	
1	1	0	0	0	0	Chopping[1:0]		CacheM	0	5_Mode	CLK_EN	CLK_DIV[3:0]			
1	1	0	1	0	0	0	0	0	0	0	0	0	0	PI_CTL2	PI_CTL1
				0	0	1	0	DET_SEL	0	SPEN[1:0]		0	0	0	0
				0	1	1	0	TARSP[7:0]							
				0	1	1	1	0	PSP[2:0]			0	ISP[2:0]		
				1	0	0	0	SPC_Limit_Out	0	0	0	SPC_Limit[3:0]			
1	1	1	0	0	0	0	0	5_IOUT[7:0]							
				0	0	1	0	0	5_PWM_Duty[6:0]						
				0	1	0	0	0	0	5_CHOP[1:0]		0	0	5_State_CTL[1:0]	
				0	1	1	0	0	0	0	0	0	6_State_CTL[2:0]		
				1	0	0	0	6_IOUT[7:0]							
				1	0	1	0	0	0	Waveform_Vthh[5:0]					
				1	0	1	1	0	0	Waveform_Vthl[5:0]					
				1	1	0	0	0	0	0	STB	0	0	STM_RS	CMD_RS

Typical Application

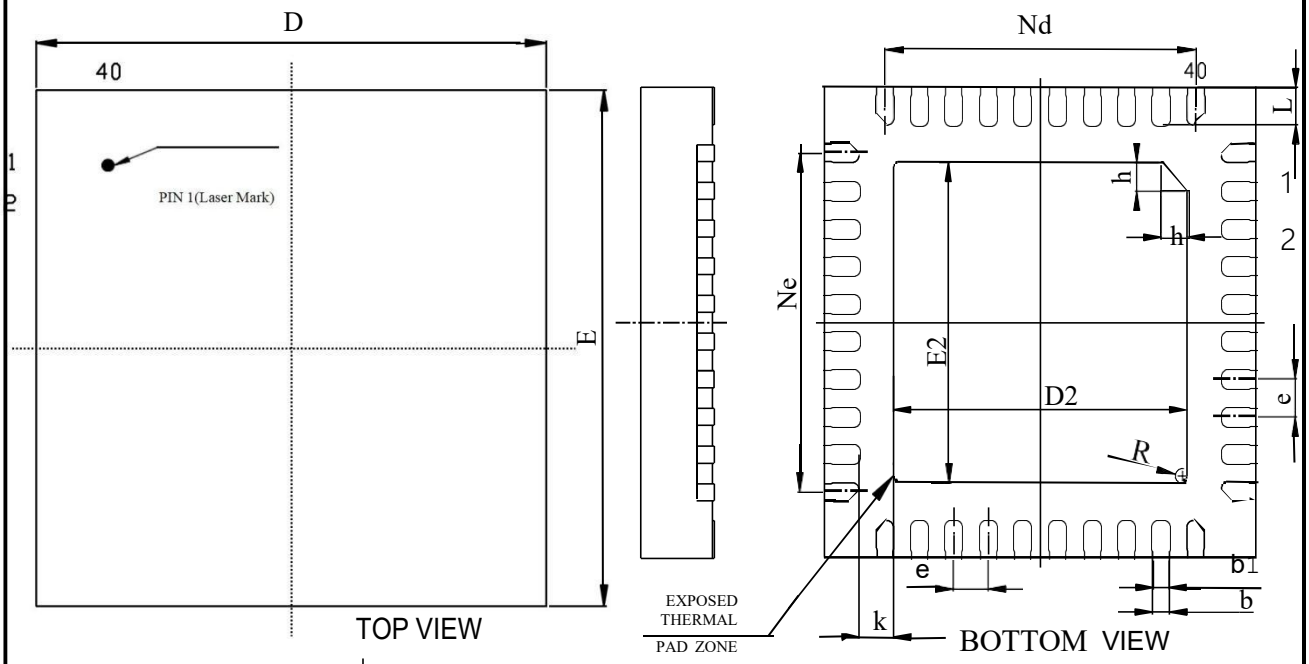


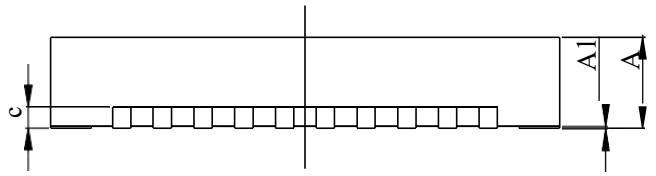





STM
5V
TEST
OUT4B
MGND34
OUT4A
OUT3B
MVCC34
OUT3A
SDATA
CSB
SCLK
21
STATE21
31
FCLK
STATE22
STATE12
SO
INA
INB
DVDDIO
DVSS
DVDD
1.8~5V
3.3V
STATE11
SENSE6
OUT6B
RNF6
OUT6A
MGND56
OUT5B
RNF5
OUT5A
11
SENSE5
M
M
1
SI
OUT1A
MVCC12
OUT1B
OUT2A
MGND12
OUT2B
PIOUT1
PIOUT2
VDDAMP
5V
5V
STM

Package InformationQFN40（5x5，e=0.4） **UNIT: mm**



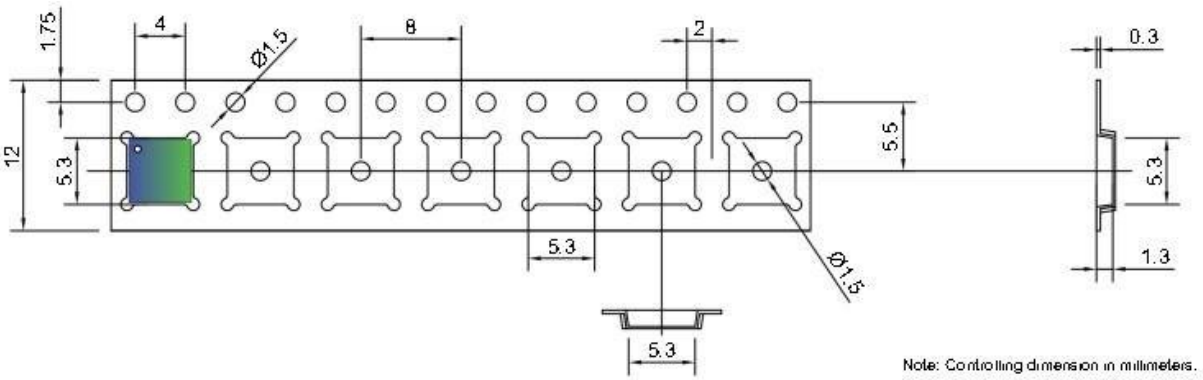


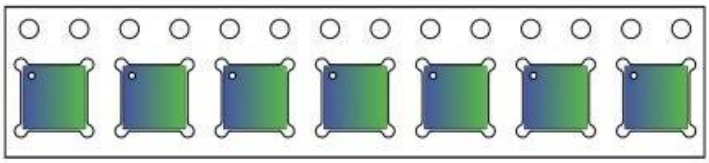
SIDE VIEW

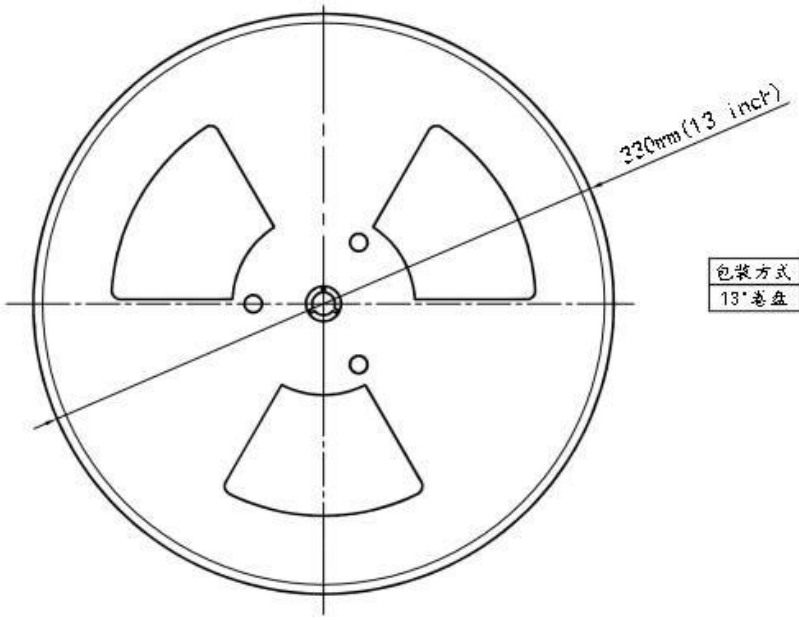
✻✻ 特殊设计：D2 和 E2 尺寸的公差是±0.05；
引脚根部缩小较少；

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 15	0. 20	0. 25
b1	0. 18REF		
c	0. 203REF		
D	4. 90	5. 00	5. 10
D2	3. 35	3. 40	3. 45
e	0. 40BSC		
Nd	3. 60BSC		
Ne	3. 60BSC		
E	4. 90	5. 00	5. 10
E2	3. 35	3. 40	3. 45
L	0. 35	0. 40	0. 45
h	0. 25	0. 30	0. 35
R	0. 075REF		
k	0. 35	0. 40	0. 45

Packaging Introduction for GC6236

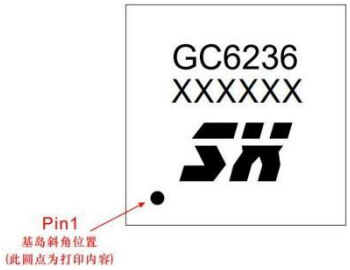






包装方式	封装形式	每盘数量	内盒盘数	装箱盒数	外箱总数
13"卷盘	QFN5*5	4000PCS	2	8	64000PCS

Description of Lot Code



Printing instructions：

1. The first line GC6236 represents the product model
2. The second line represents the traceability code

Release Notes

GC6236 datasheet V1.0	**Initial 1.0 version；**
GC6236 datasheet V1.1	**Corrected ambiguity in some descriptions ;**
GC6236 datasheet V1.2	**Added packaging instructions to enhance the clarity of packaging drawings；**