24bit, 192kHz stereo dual channel D/A converter

Description：

GC4344 is a stereo DAC chip with interpolation filter, multi-bit DAC and output analog filter.GC4344 supports most audio data formats.GC4344 is based on a fourth-order multi-bit modulator with a linear analog low-pass filter, and the sampling rate can be automatically adjusted between 2KHz and 200KHz by detecting the signal frequency and the main clock frequency.

GC4344 integrates an internal digital de-emphasis module that works under 3.3V and 5V.These features make it an ideal choice for audio devices such as DVD playback decoders, digital communication devices, etc.

GC4344 is packaged in MSOP10 and DFN10.

Features：

- Muti-bit modulator
- 24bit D/A Converter
- Automatic detection of signal frequencies up to 192KHz
- 105dB Dynamic Range
- -90dB Total Harmonic Distortion+SNR
- Low clock jitter sensitivity
- 3.3V or 5V operating voltage
- Linear filter output
- Integrated Digital De-emphasis
- Package: MSOP10, DFN10

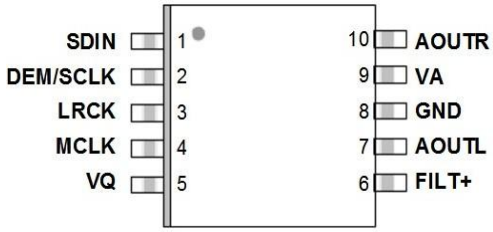
Application：

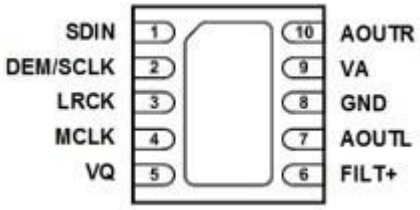
- DVD Player
- Digital Audio Device
- Other high precision audio conversion

Packaging Introduction

Per Tray	Per Box	Per Case
4K	8K	64K

PIN DESCRIPTIONS：





Pin#	Name	Pin Description
1	SDIN	Serial Audio Data Input
2	DEM /SCLK	External Serial Clock Input Port
3	LRCK	Left/Right Clock Port
4	MCLK	Primary Clock Port
5	VQ	Filter connection for internal quiescent voltage
6	FILT+	Positive reference voltage for the internal sampling circuits
7	AOUTL	Analog left channel output port
8	GND	ground
9	VA	Analog power supply
10	AOUTR	Analog right channel output port

ABSOLUTE MAXIMUM RATINGS：

Parameters	Min	Nom	Max	Recommended Scope
VA	-0.3V		6.0 V	3V-5.5V
Input Current, Any Pin Except Supplies			±10 mA	
Digital Input Voltage	-0.3V		VA+0.4 V	3V-5.5V
Operating Temperature	-55 ºC		125 ℃	-40 ºC—85 ºC
Storage Temperature	-65 ºC	-	150 ºC	

CHARACTERISTICS：

DAC ANALOG CHARACTERISTICS

(Full-Scale Output Sine Wave, 997 Hz, Fs = 48/96/192 kHz; Test load RL = 3 k , CL = 10 pF
Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

		5 V			3.3 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Dynamic Performance								
Dynamic Range	18 to 24-Bit A-weighted	99	105	-	97	103	-	dB
	18 to 24-Bit unweighted	96	102	-	94	100	-	
	16-Bit A-weighted	90	96	-	90	96	-	
	16-Bit unweighted	87	93	-	87	93	-	
Total Harmonic Distortion + Noise	18 to 24-Bit:-20 dB	-	-82	-76	-	-80	-74	dB
	18 to 24-Bit:-60 dB	-	-42	-36	-	-40	-34	
	16-Bit :-20 dB	-	-73	-67	-	-73	-67	
	16-Bit : -60 dB	-	-33	-27	-	-33	-27	

DAC ANALOG CHARACTERISTICS:

Parameter	symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		0.60•VA	0.65•VA	0.70•VA	Vpp
Quiescent Voltage	VQ	-	0.5•VA	-	VDC
Max DC Current from an AOUT pin	IOUTmax	-	10	-	uA
Max Load Capacitance	CL	-	100	-	pF
Output Impedance	ZOUT	-	100	-	Ω

ON-CHIP DIGITAL AND ANALOG FILTER RESPONSE

Parameter	symbol	Min	Typ	Max	Unit
Single-Speed Mode					
Passband to -0.1 dB corner		0	-	0.35	fs
Passband to -3 dB corner		0	-	0.499	fs
Frequency Response 10 Hz to 20 kHz		-0.175	-	+0.1	dB
StopBand		0.5465	-	-	fs
StopBand Attenuation		50	-	-	dB
Group Delay		-	10/Fs	-	s
De-emphasis Error Fs = 32 kHz		-	-	+1.5/+0	dB
De-emphasis Error Fs = 44.1 kHz		-	-	+.05/-.25	
De-emphasis Error Fs = 48 kHz		-	-	-.2/-.4	
Double-Speed Mode					
Passband to -0.1 dB corner		0	-	0.22	fs
Passband to -3 dB corner		0	-	0.501	fs
Frequency Response 10 Hz to 20 kHz		-0.15	-	+0.15	dB
StopBand		0.577	-	-	fs
StopBand Attenuation		55	-	-	dB
Group Delay		-	5/Fs	-	s
Quad-Speed Mode					
Passband to -0.1 dB corner		0	-	0.11	fs
Passband to -3 dB corner		0	-	0.469	fs
Frequency Response 10 Hz to 20 kHz		-0.12	-	0	dB
StopBand		0.7	-	-	fs
StopBand Attenuation		51	-	-	dB
Group Delay		-	2.5/Fs	-	s

DIGITAL INPUT CHARACTERISTICS：

Parameter	symbol	Min	Typ	Max	Unit
High-Level Input Voltage	VIH	0.6*VA	-	-	V
Low-Level Input Voltage	VIL	-	-	0.3*VA	V
Input Leakage Current	Iin	-	-	±10	uA
Input Capacitance		-	8	-	pF

POWER CHARACTERISTICS：

Parameter	symbol	Min	Typ	Max	Unit
normal operation Supply Current(5V)	IA	-	21	30	mA
normal operation Supply Current(3.3V)		-	15	20	mA
power-down state Supply Current(5V)		-	220	-	uA
power-down state Supply Current(3.3V)		-	100	-	uA

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE:

Parameter		symbol	Min	Typ	Max	Unit
MCLK Frequency			0.512	-	50	MHz
MCLK Frequency			45	-	55	%
Input Sample Rate	All MCLK/LRCK ratios combined	fs	2		200	KHz
	256x, 384x, 1024x		2		50	
	256x, 384x		84		134	
	512x, 768x		42		67	
	1152x		30		34	
	128x, 192x		50		100	
	64x, 96x		100		200	
	128x, 192x		168		200	
External SCLK Mode						
LRCK Duty Cycle (External SCLK only)			45	50	55	%
SCLK Pulse Width Low		tsclkl	20	-	-	ns
SCLK Pulse Width High		tsclkh	20	-	-	ns
SCLK Duty Cycle			45	50	55	%
SCLK rising to LRCK edge delay		tslrd	20	-	-	ns
SCLK rising to LRCK edge setup time		tslrs	20	-	-	ns
SDIN valid to SCLK rising setup time		tsdlrs	20	-	-	ns
SCLK rising to SDIN hold time		tsdh	20	-	-	ns
Internal SCLK Mode						
LRCK Duty Cycle (Internal SCLK only)			-	50	-	%
SCLK Period		tsclkw	10^9/SCLK	-	-	ns
SCLK rising to LRCK edge		tsclkr	-	Tsclkw/2	-	ns
SDIN valid to SCLK rising setup time		tsdlrs	10^9/(512*fs)+10	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK =1152, 1024, 512, 256, 128, or 64		tsdh	10^9/(512*fs)+15	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 768, 384, 192, or 96		tsdh	10^9/(512*fs)+15	-	-	ns

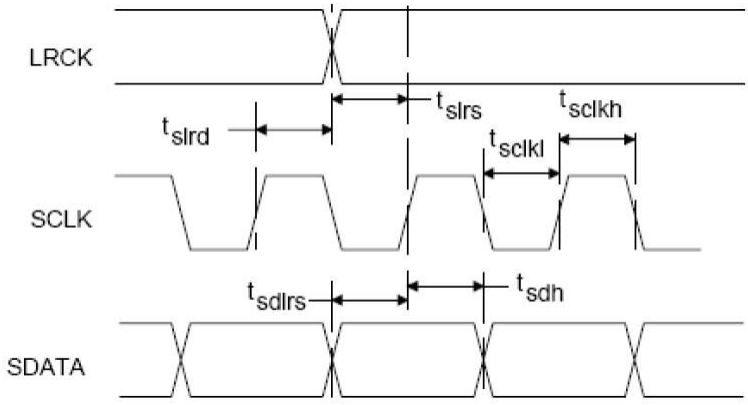


Figure 1. External Serial Mode Input Timing

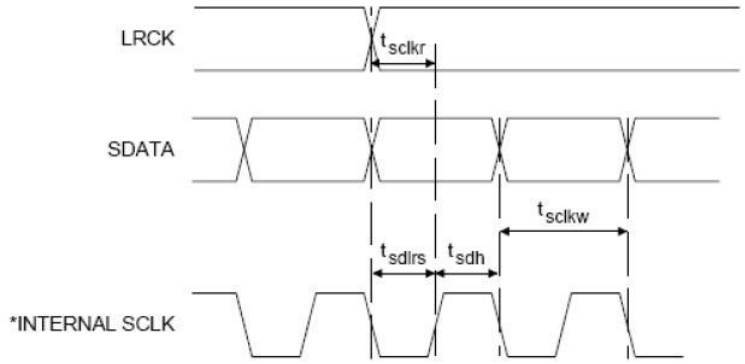
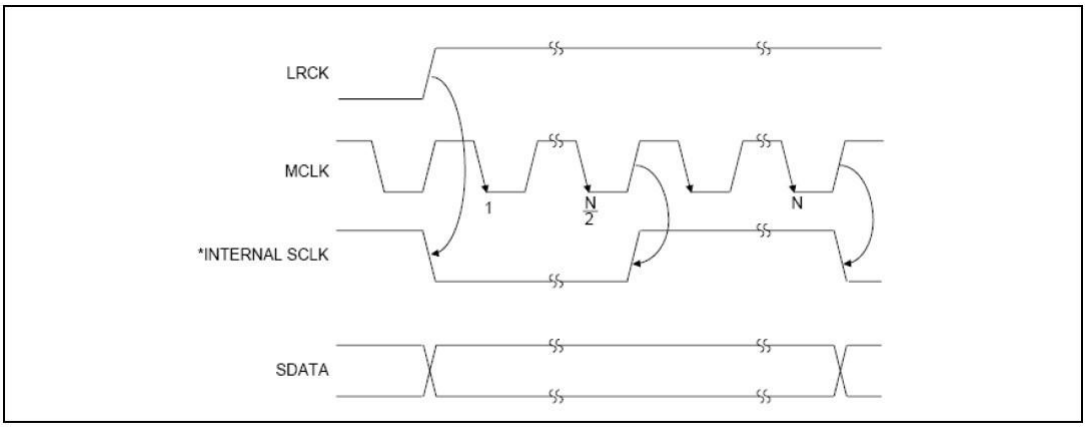


Figure 2. Internal Serial Mode Input Timing



N = MCLK /SCLK

Figure 3. Internal Serial Clock Generation

APPLICATIONS：

Audio sampling frequencies of GC4344 standard including 48, 44.1, 32 kHz in SSM mode, 96, 88.2, 64 kHz in DSM mode, 192, 176.4, 128kHz in QSM mode.Audio data is input through the serial input data end (SDIN).The left/right channel clock (LRCK) determines the channel for the current input data.A serial clock is a clock in which audio data enters the input data cache.The input data format of GC4344 is shown in Table 1.

Master Clock

The MCLK/LRCK ratio must be an integer, as shown in Table 1.The frequency of the LRCK is equal to the frequency Fs of the input data for each channel.The ratio and speed mode of MCLK to LRCK are determined by the number of MCLK cycles and the value of MCLK during an LRCK cycle when the chip is initialized.The built-in divider produces the right clock.Table 1 lists some audio sampling frequencies and the corresponding MCLK and LRCK frequencies.Note that there is no phase requirement here, but LRCK and SCLK must be synchronized.

LRCK (kHz)	MCLK (MHz)									
	64x	96x	128x	192x	256x	384x	512x	768x	1024x	1152x
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.1920	12.2880	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-
方式	QSM				DSM		SSM			

Table 1. Common Clock Frequencies

Serial Clock

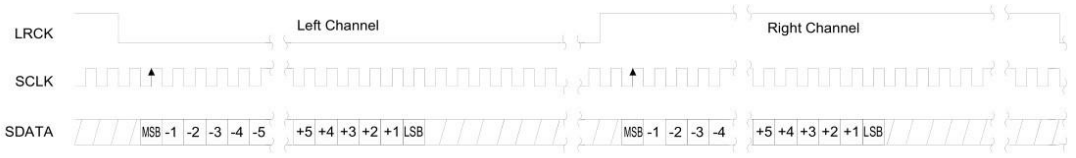
GC4344 has external and internal serial clock input modes.

External Serial Input Clock

During an LRCK cycle, when 16 rising edge pulses are continuously detected on the SCLK port, an external serial input clock is entered. In this mode, the internal serial mode and the de-emphasis mode are shielded.When no rising edge pulse is detected for two consecutive LRCK cycles on the SCLK port, the system enters the internal serial input clock mode.

Internal Serial Input Clock

In the internal serial input clock mode, the serial input clock is generated internally by the chip and synchronized with MCLK and LRCK.The SCLK/LRCK ratio can be 32, 48, 64, or 72, depending on the format of the input data.This mode allows the use of numbers to de-emphasize functionality.



Internal SCLK Mode	External SCLK Mode
I²S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 I²S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 I²S, Up to 24-Bit data and INT SCLK = 72 Fs if MCLK/LRCK = 1152	I²S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 4. Data Format (I2S)

De-emphasis

GC4344 contains on-chip digital de-emphasis, and Figure 5 shows the de-emphasis curve at Fs 44.1 kHz.The de-emphasis filter starts when the DEM/SCLK port keeps low level along five consecutive LRCK drops.This function is only valid in internal serial clock mode.

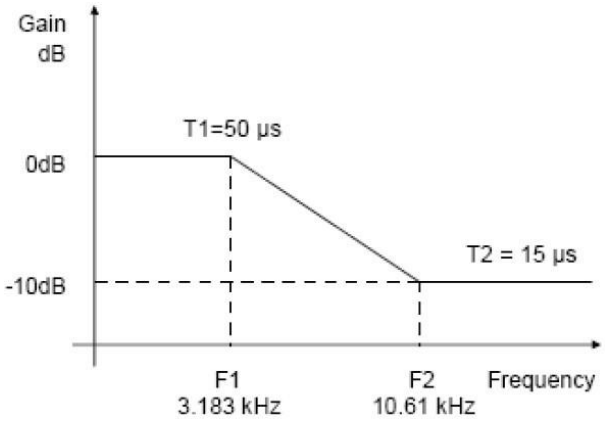
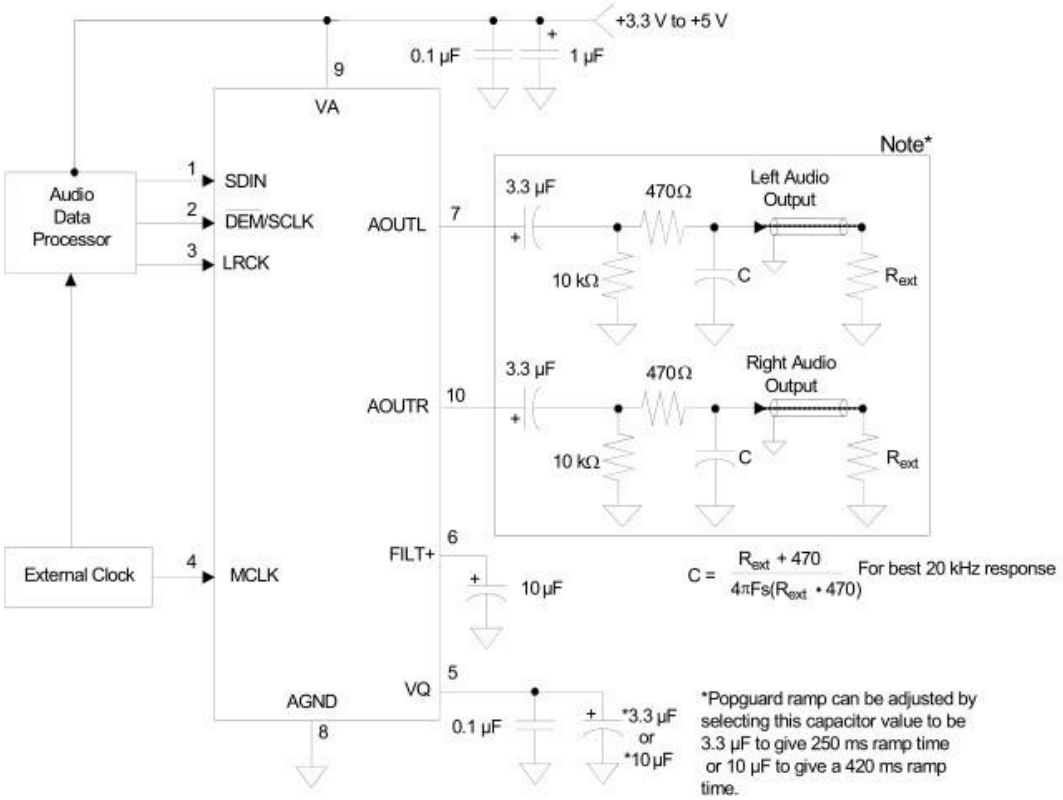


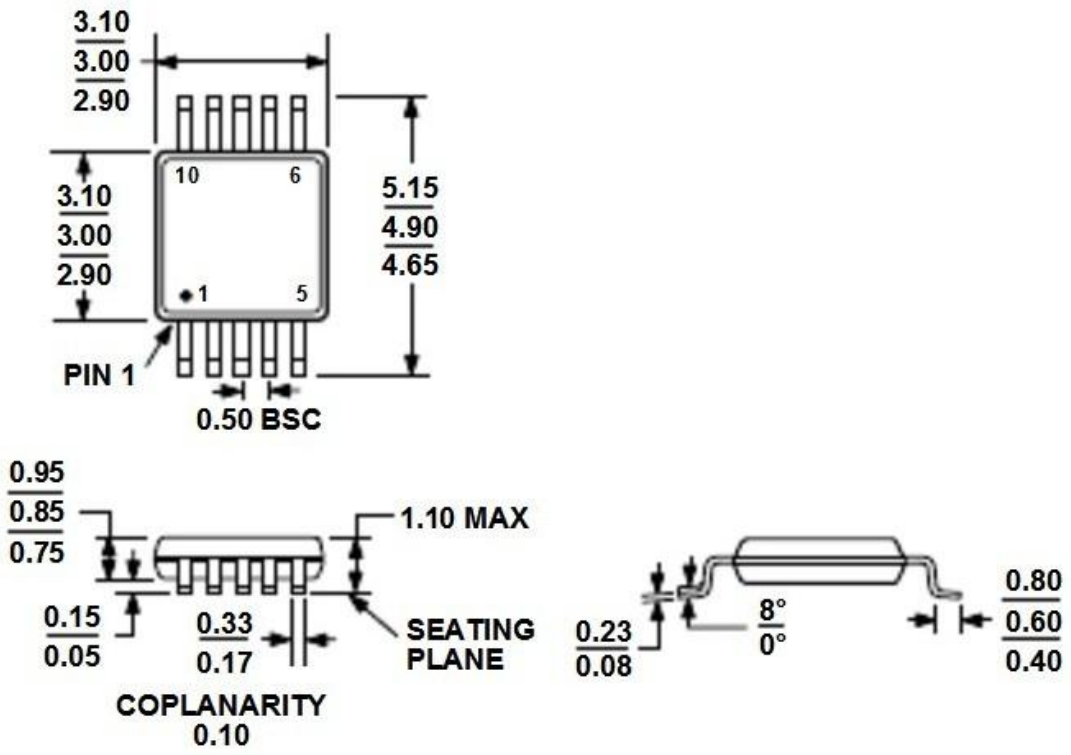
Figure 5. De-Emphasis Curve (Fs = 44.1kHz)

TYPICAL APPLICATION：

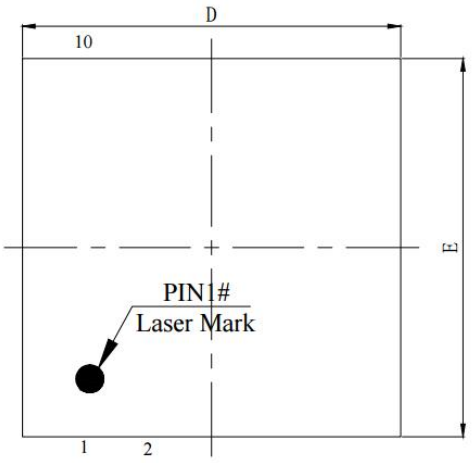


Package：

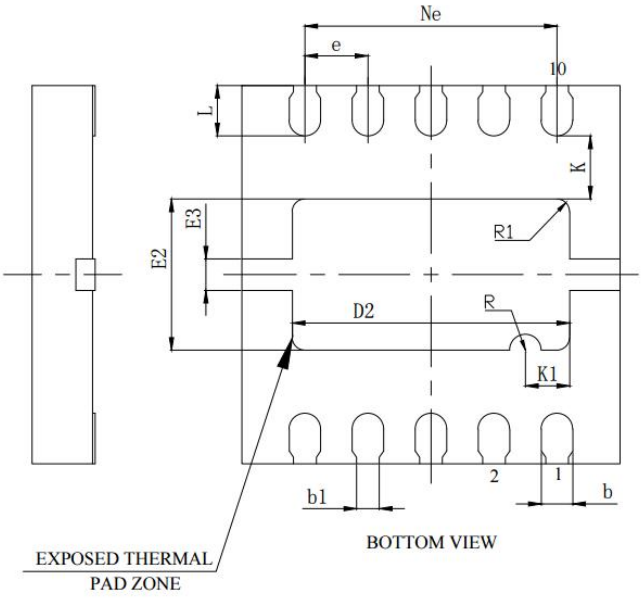
MSOP10



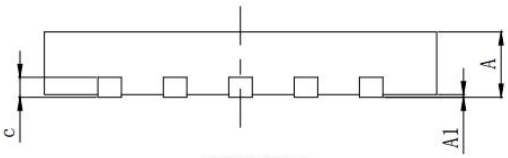
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.150REF		
D	2.95	3.00	3.05
D2	2.10	2.20	2.30
e	0.50BSC		
Ne	2.00BSC		
E	2.95	3.00	3.05
E2	1.10	1.20	1.30
E3	0.20	0.25	0.30
L	0.30	0.40	0.50
R	0.125REF		
R1	0.100REF		
K	0.45	0.50	0.55
K1	0.35REF		