

GENERAL DESCRIPTION

The LW58XX Series is a Sub- μ A power consumption, high accuracy, low drop-out voltage regulator with Chip Enable Pin, high ripple rejection and fast discharge function.

The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter for the output pin.

Output voltage is selectable from 1.0V to 5.0V which fixed by laser trimming technologies, Step=100mV.

The LW58XX is available in SOT23, SOT23-3L, SOT23-5L and DFN1x1-4L packages.

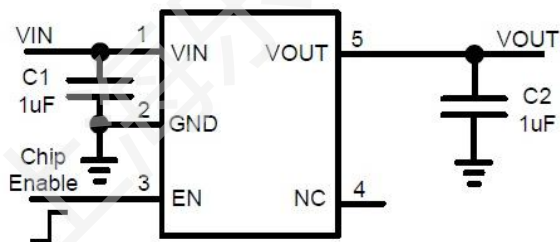
FEATURES

- Ultra-Low Power Consumption: 0.7 μ A(Typ.)
- Operating Voltage Range: from 1.5V to 6.0V
- Output Voltage Range: from 1.0V to 5.0V
- Maximum Output Current: 500mA
- Output Accuracy: $\pm 1.5\%$ @+25 $^{\circ}$ C
- Low Dropout Voltage:450mV@500mA/3.3V
- High PSRR: 80dB@1KHz, 10mA
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Fast Discharge Function
- Stable with 1 μ F Output Capacitor

APPLICATIONS

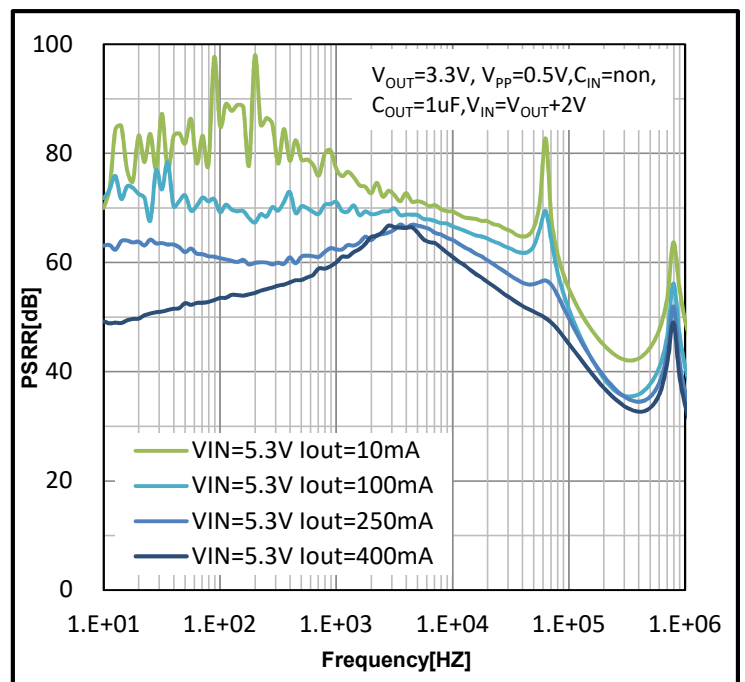
- Battery-Powered Devices
- Portable Consumer Equipment
- Ultra Low Power Applications

TYPICAL APPLICATION CIRCUIT



Note: EN must NOT be left floating.

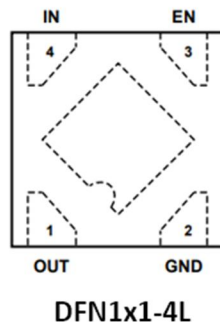
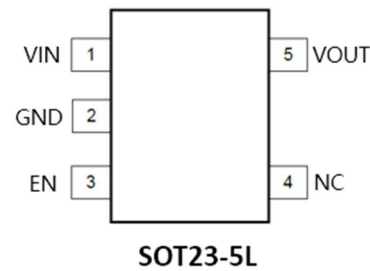
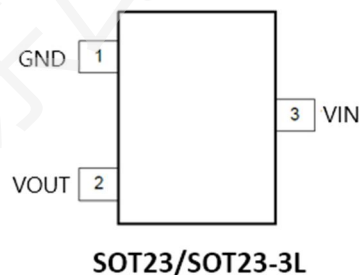
TYPICAL PERFORMANCE CHARACTERISTICS



PIN DESCRIPTION:

PIN No			SYMBOL	DESCRIPTION
SOT23/ SOT23-3L	SOT23-5L	DFN1x1-4L		
3	1	4	VIN	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Requirements section. Place the input capacitor as close to the output of the device as possible.
1	2	2	GND	Ground pin.
--	3	3	EN	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
--	4	--	NC	No internal connection. Ground this pin for better thermal performance.
2	5	1	VOUT	Regulated output voltage pin. Connect a low-equivalent series resistance (ESR) capacitor to this pin. For best transient response, use the nominal recommended value or larger capacitor from OUT to GND. An internal pulldown resistor prevents a charge from remaining on OUT when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$).
--	--	Thermal Pad	Pad	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

PIN ASSIGNMENT



MARK INFORMATION:

SOT23/ SOT23-3L

XX: VOLTAGE

58XXYY

YY: DATE CODE

SOT23-5L

XX: VOLTAGE

LW58XX
YYYYY

YY: DATE CODE

DFN1x1-4L

X: VOLTAGE

58X

1.0V	1.2V	1.5V	1.8V	2.5V	2.8V	3.0V	3.3V	3.6V	4.2V	5.0V
B	C	D	G	H	J	L	M	P	S	T

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾:

(T_A =25℃, unless otherwise specified.)

SYMBOL	ITEM	RATING	UNIT	
V _{IN}	Supply Voltage	-0.3~7.0	V	
V _{EN}	EN Pin Voltage	-0.3~7.0	V	
V _{OUT}	V _{OUT} Pin Voltage	-0.3~(V _{IN} +0.3)	V	
V _(ESD)	ESD Susceptibility, HBM ⁽²⁾	±4000	V	
P _D	Maximum Power Dissipation ⁽³⁾	SOT23	490	mW
		SOT23-3L	520	
		SOT23-5L	543	
		DFN1x1-4L	553	
R _{θJA}	Junction-to-ambient Thermal Resistance ⁽³⁾	SOT23	255	℃/W
		SOT23-3L	240	
		SOT23-5L	230	
		DFN1x1-4L	226	
T _J	Junction Temperature Range	-40~150	℃	
T _{STG}	Storage Temperature Range	-40~150	℃	
T _{SOLDER}	Lead Temperature (Soldering)	260℃, 10s		

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

2. per ANSI/ESDA/JEDEC JS-001

3. Device mounted on FR-4 PCB

RECOMMENDED OPERATING RANGE:

SYMBOL	ITEM	VALUE	UNIT
V _{IN}	V _{IN} Supply Voltage	1.5~6.0	V
V _{EN}	EN Pin Voltage	0~6.0	V
V _{OUT}	V _{OUT} Pin Voltage	1.0~5.0	V
I _{OUT}	Output Current	0~500	mA
T _J	Junction Temperature Range	-40~125	℃

ELECTRICAL CHARACTERISTICS:

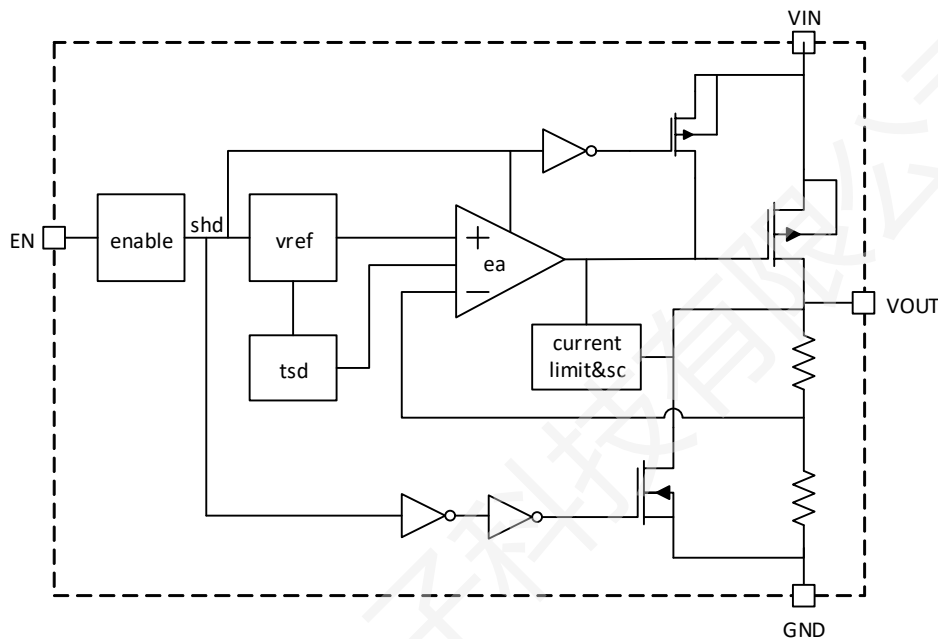
($V_{IN}=V_{OUT(NOM)}+1V$ or $2V$, whichever is greater, $C_{IN}=C_{OUT}=1\mu F$, unless otherwise specified, typical values are at $T_A = 25^\circ C$.)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Unit
V_{IN}	Input Voltage		1.5		6.0	V
V_{OUT}	Output Accuracy	$I_{OUT}=1mA$	-1.5		+1.5	%
I_{LIM}	Current Limit ⁽¹⁾		530	750		mA
I_Q	Quiescent Current	$V_{IN}=V_{EN}=V_{OUT}+1V$, No Load		0.7	1.0	μA
I_{SHD}	Shutdown Current	$V_{IN}=6.0V$, $V_{EN}=0V$			0.1	μA
V_{DROP}	Dropout Voltage ⁽¹⁾⁽²⁾	$I_{OUT}=100mA$	$V_{OUT}=3.3V$	80		mV
		$I_{OUT}=300mA$		255		
		$I_{OUT}=500mA$		450		
		$I_{OUT}=100mA$	$V_{OUT}=5.0V$	65		
		$I_{OUT}=300mA$		200		
		$I_{OUT}=500mA$		360		
$\frac{\Delta V_{OUT}}{(\Delta V_{IN} * V_{OUT(NOM)})}$	Line Regulation	$V_{IN}=V_{OUT}+1.0V$ to $6.0V$, $I_{OUT}=1mA$		0.1	0.25	%/V
ΔV_{OUT}	Load Regulation	$1mA \leq I_{OUT} \leq 500mA$		50	100	mV
I_{SHORT}	Short Current ⁽¹⁾	$V_{OUT}=0V$	LW5812	50		mA
			LW5833	80		
			LW5850	80		
V_{ENH}	EN High Voltage	$V_{IN}=1.5V$ to $6.0V$, $I_{OUT}=1mA$	1.5			V
V_{ENL}	EN Low Voltage				0.5	V
T_{STR}	Startup Time	From V_{EN} 'L' \rightarrow 'H' to $95% * V_{OUT}$, $C_{OUT}=1\mu F$, No Load		400		μs
PSRR	Power Supply Rejection Ratio	$V_{IN}=4.3V$, $V_{OUT}=3.3V$ $V_{PP}=0.5V$, $C_{IN}=None$, $I_{OUT}=10mA$	$f=217Hz$	83		dB
			$f=1KHz$	80		
			$f=10KHz$	69		
T_{SD}	Thermal Shutdown	Temperature rising		165		$^\circ C$
ΔT_{SD}	TSD Hysteresis	Temperature falling		30		$^\circ C$
R_{DSCHG}	R_{ON} of Discharge MOSFET	$V_{IN}=6V$, $V_{EN}=0V$		100		Ω

NOTES:

1. Guaranteed by design
2. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when $V_{OUT} = 95% * V_{OUT(NOM)}$

SIMPLIFIED BLOCK DIAGRAM:



DETAIL OPERATION DESCRIPTION:

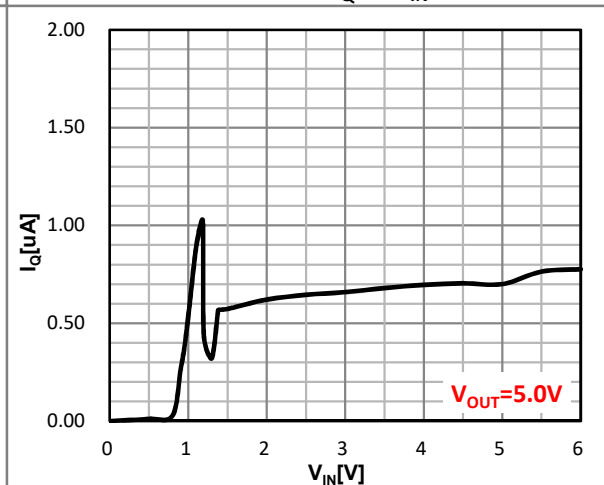
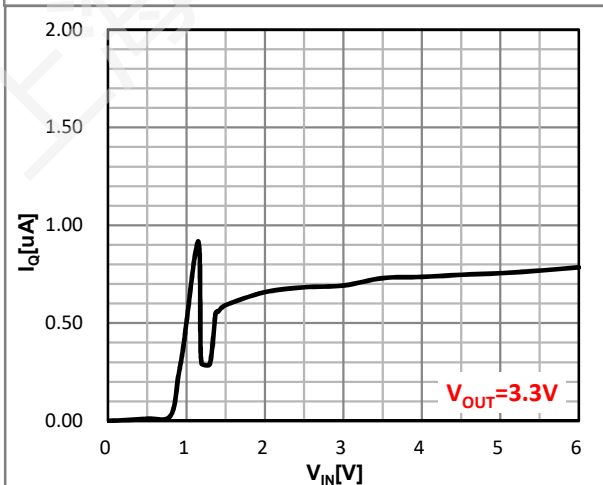
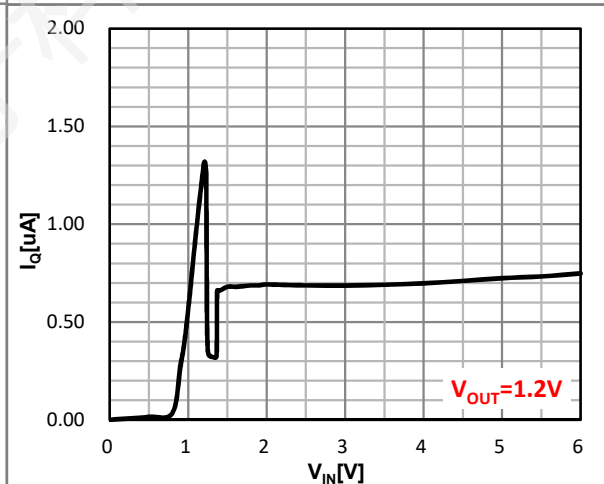
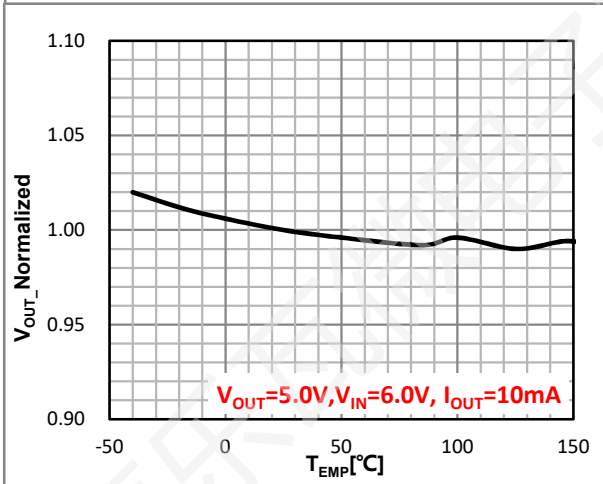
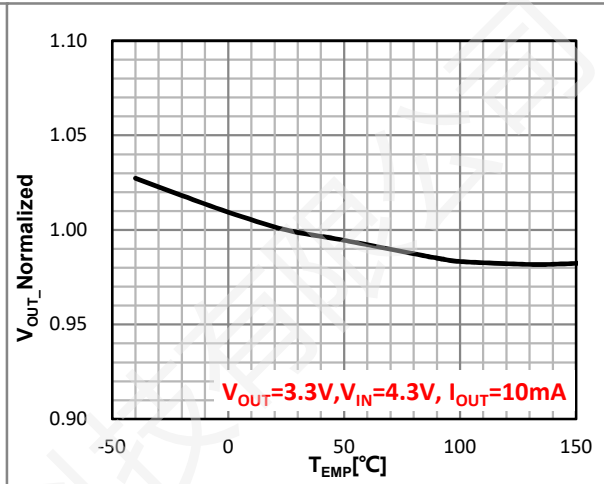
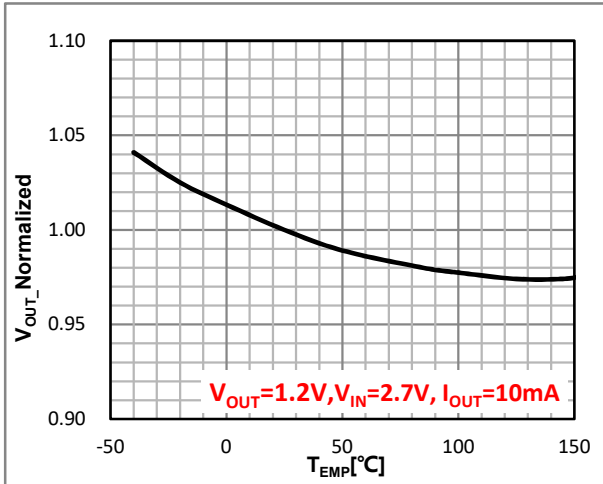
The LW58XX Series is a low power consumption low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision voltage reference and an error correction circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold through the switch. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

TYPICAL OPERATING CHARACTERISTICS:

(Tested under $T_A = 25^\circ\text{C}$, $C_{IN} = C_{OUT} = 1\mu\text{F}$, unless otherwise specified)



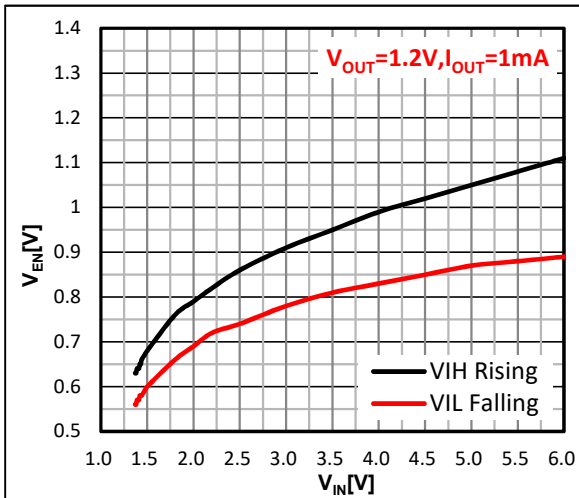


Figure 7. V_{EN} VS V_{IN}

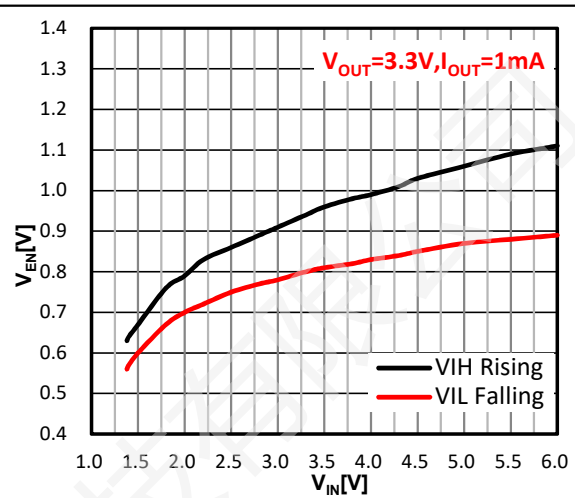


Figure 8. V_{EN} VS V_{IN}

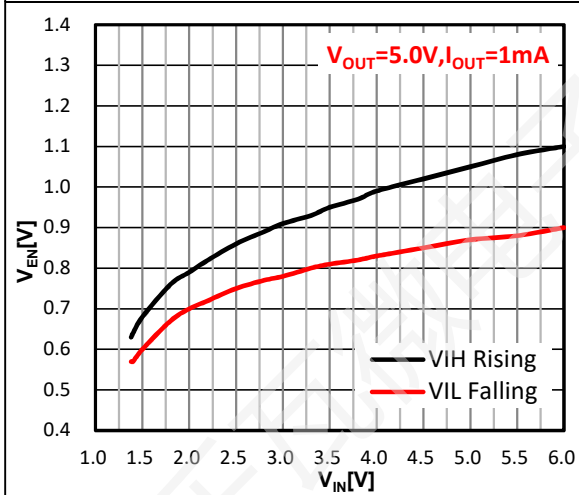


Figure 9. V_{EN} VS V_{IN}

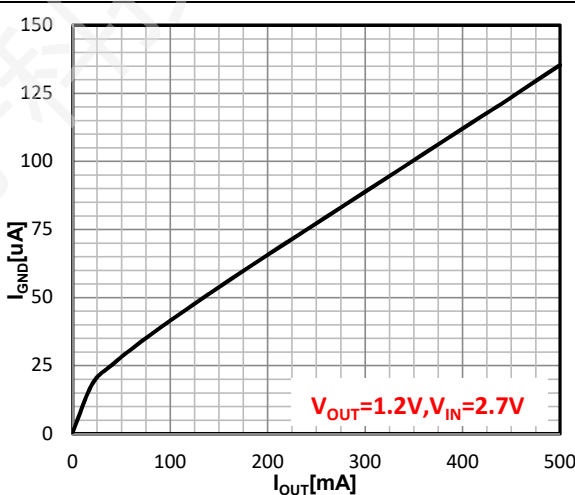


Figure 10. I_{GND} VS I_{OUT}

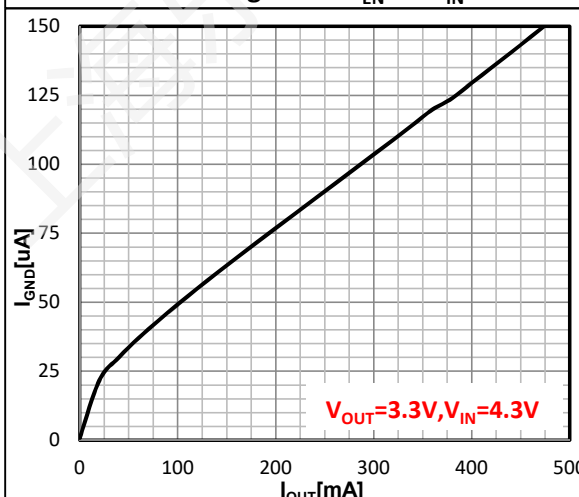


Figure 11. I_{GND} VS I_{OUT}

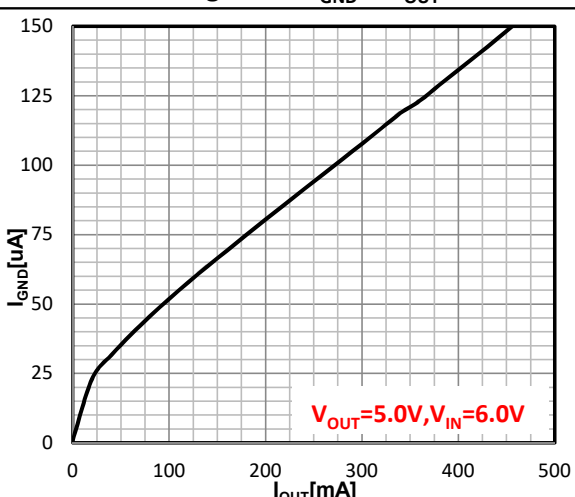


Figure 12. I_{GND} VS I_{OUT}

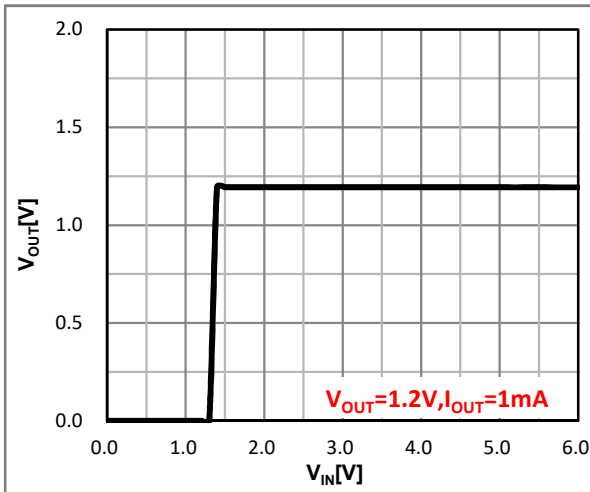


Figure 13. V_{OUT} vs V_{IN}

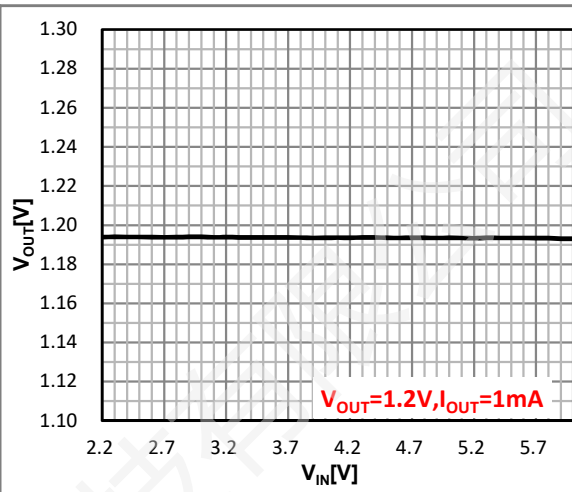


Figure 14. Line Regulation

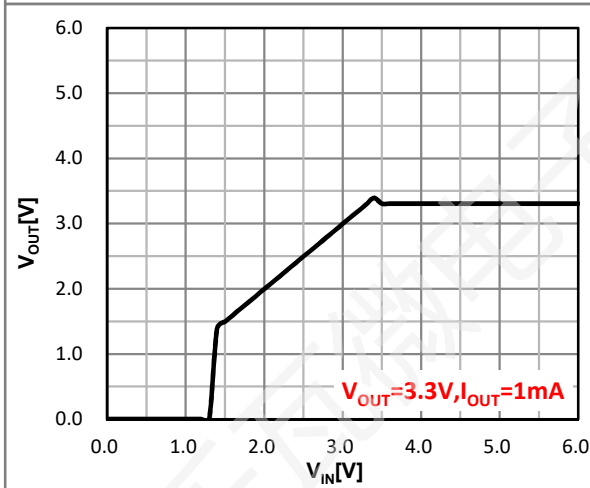


Figure 15. V_{OUT} vs V_{IN}

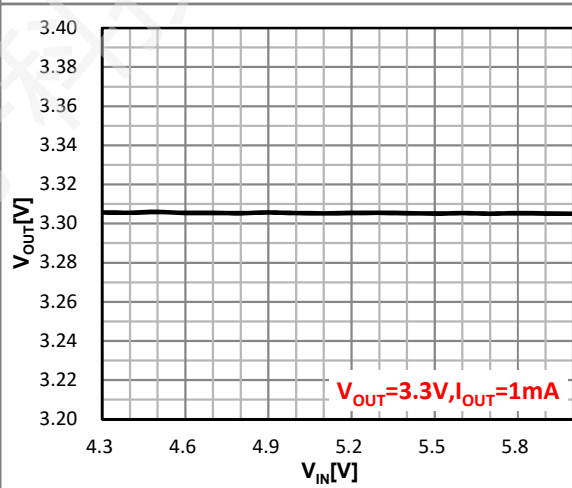


Figure 16. Line Regulation

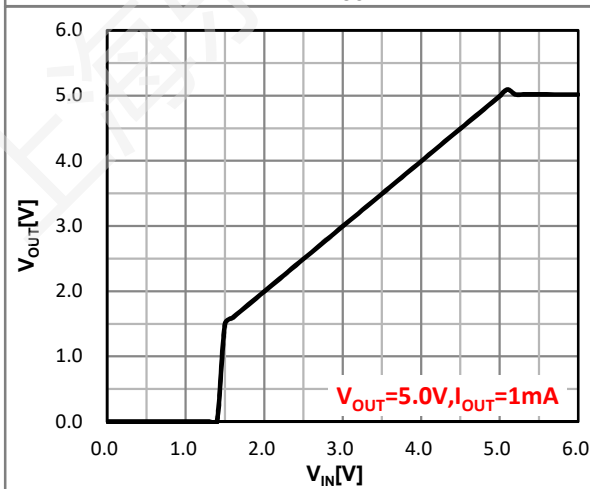


Figure 17. V_{OUT} vs V_{IN}

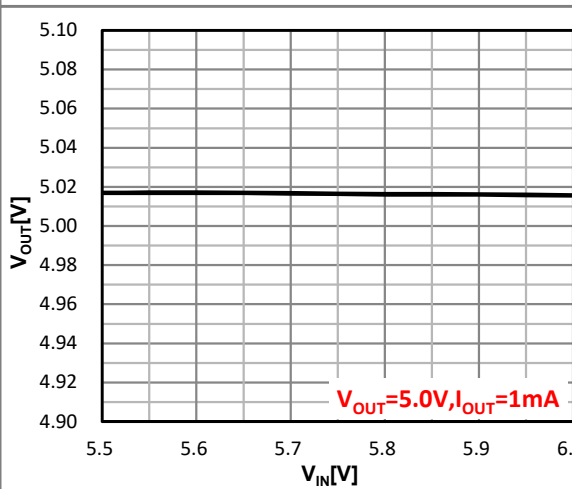


Figure 18. Line Regulation

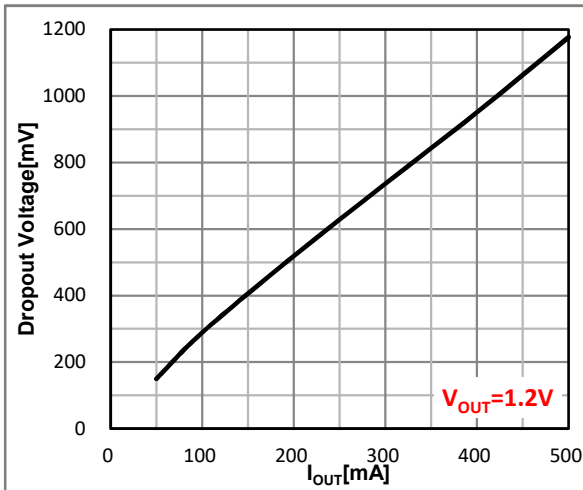


Figure 19. Dropout Voltage VS I_{OUT}

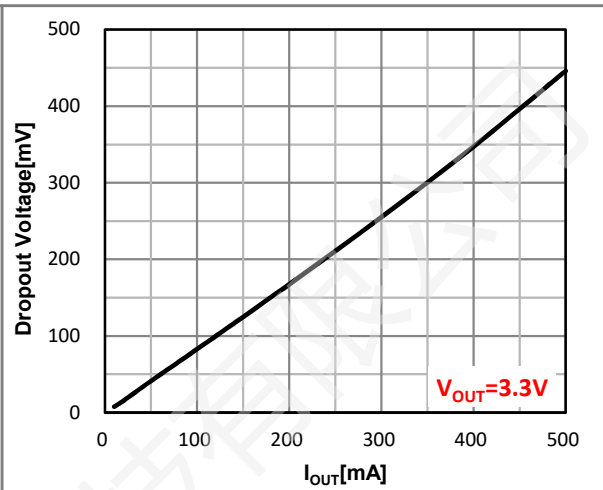


Figure 20. Dropout Voltage VS I_{OUT}

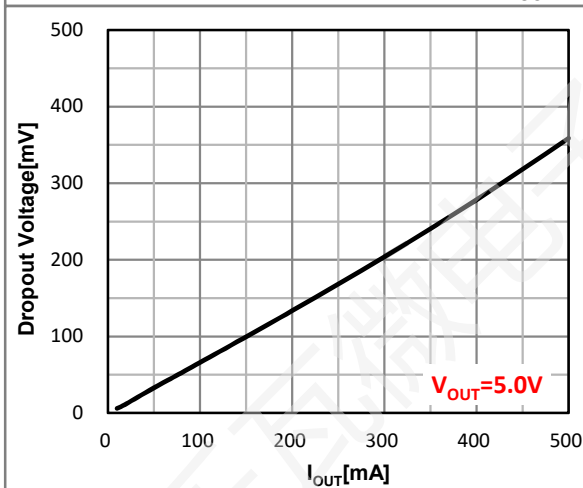


Figure 21. Dropout Voltage VS I_{OUT}

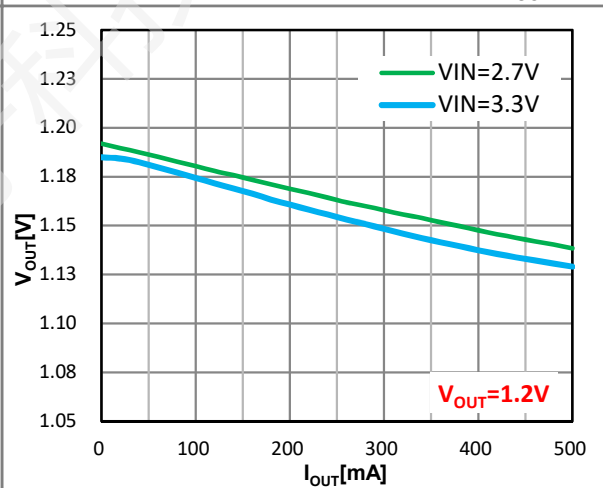


Figure 22. Load Regulation

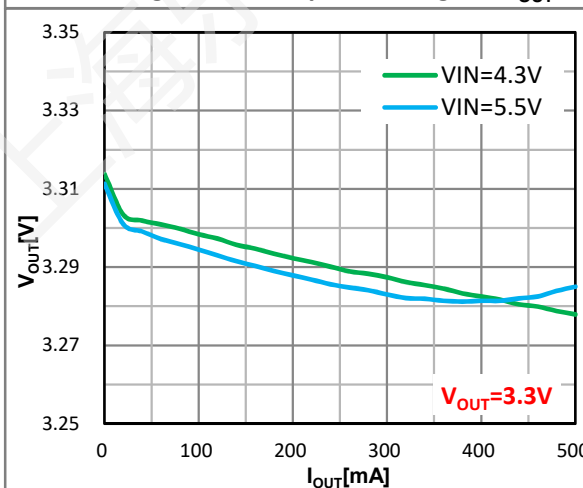


Figure 23. Load Regulation

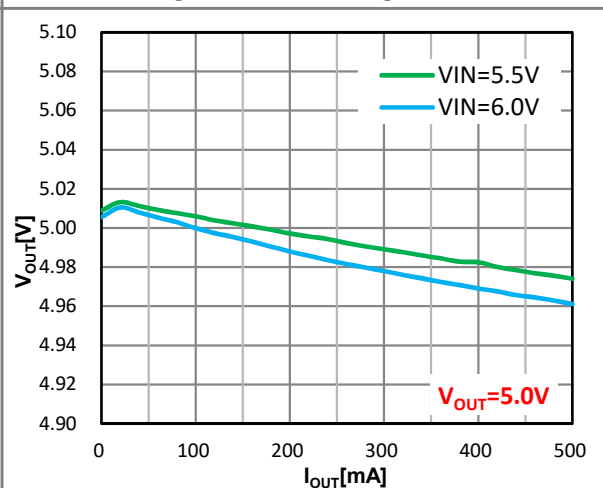
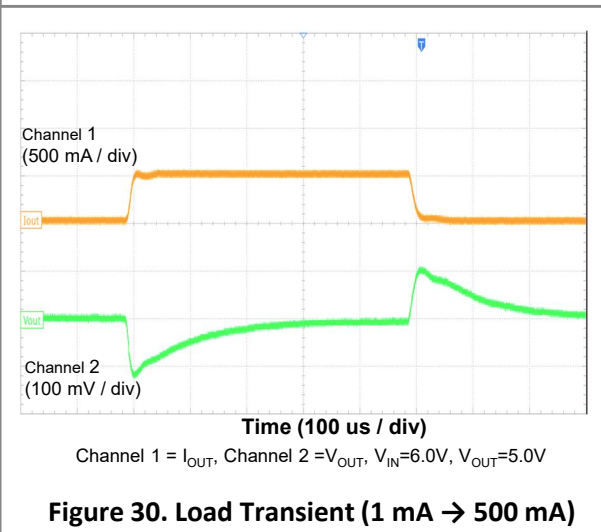
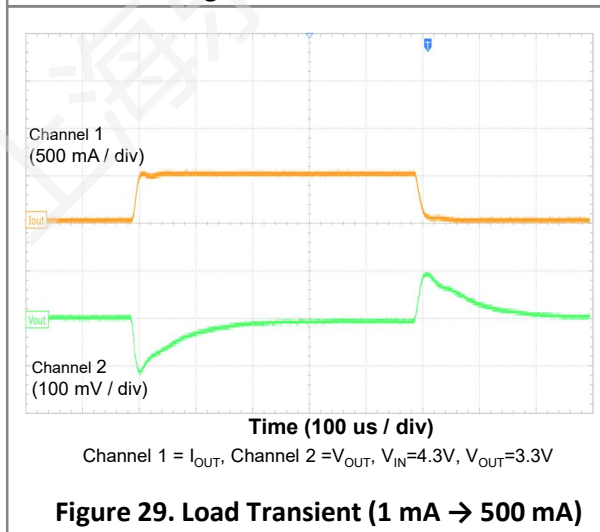
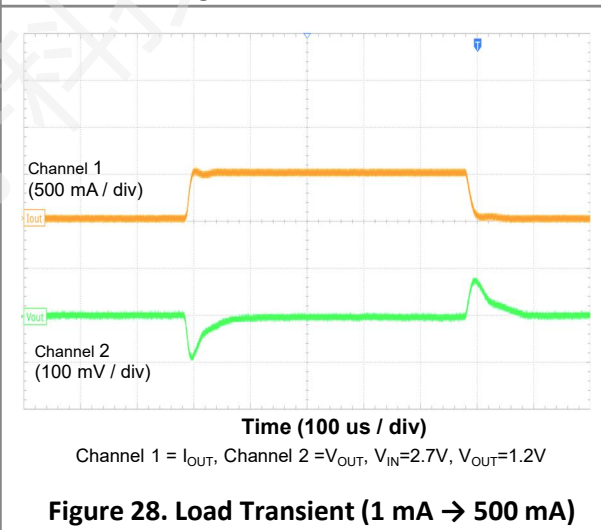
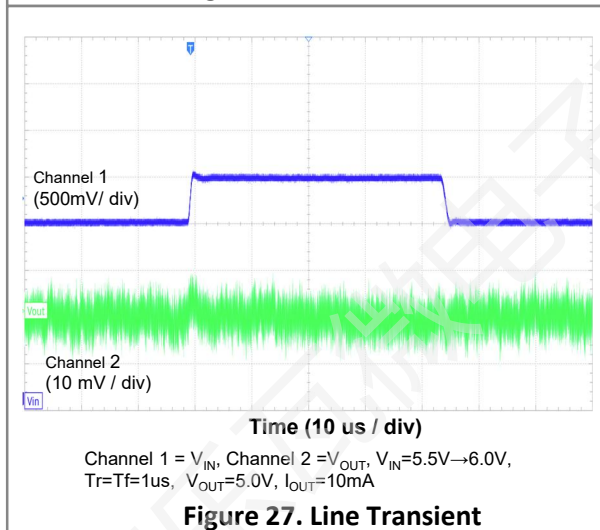
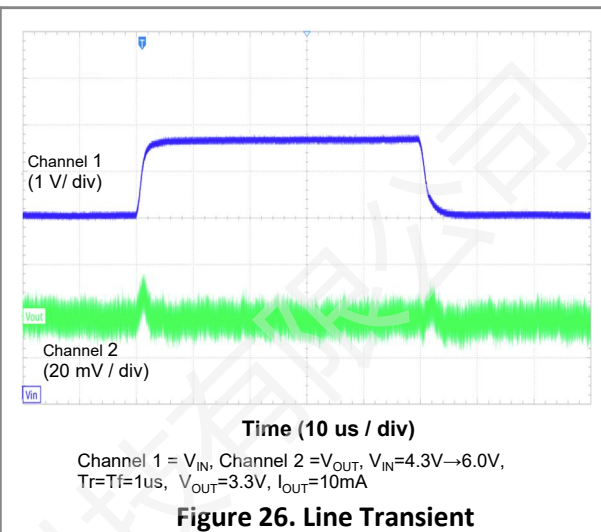
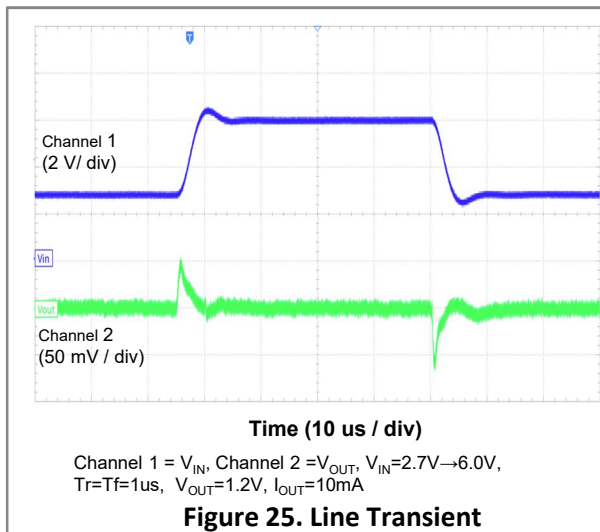
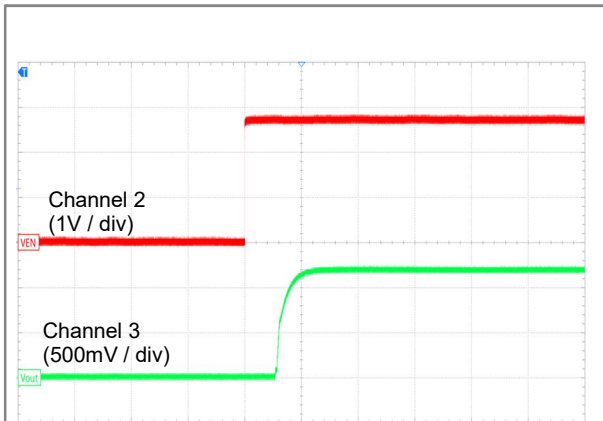


Figure 24. Load Regulation

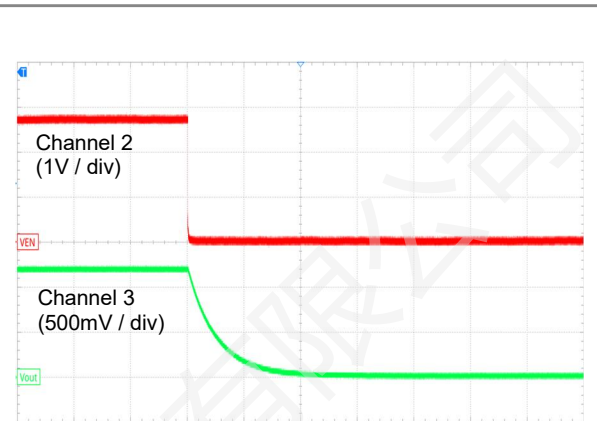




Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=2.7V, EN=0→2.7V, V_{OUT}=1.2V, No Load

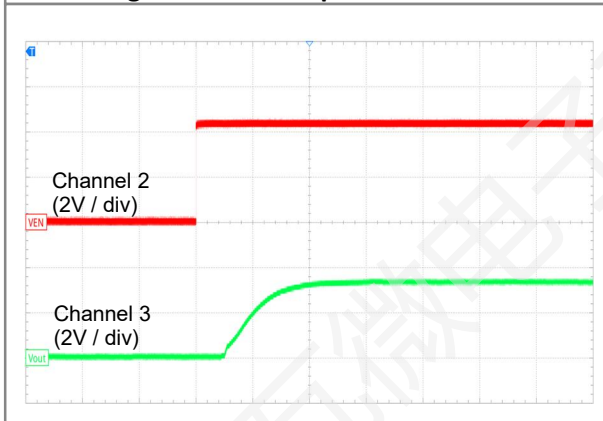
Figure 31. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=2.7V, EN=2.7→0V, V_{OUT}=1.2V, No Load

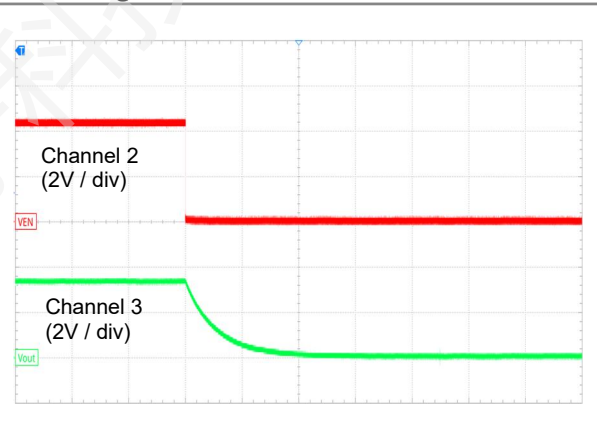
Figure 32. Shut-Down with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=0→4.3V, V_{OUT}=3.3V, No Load

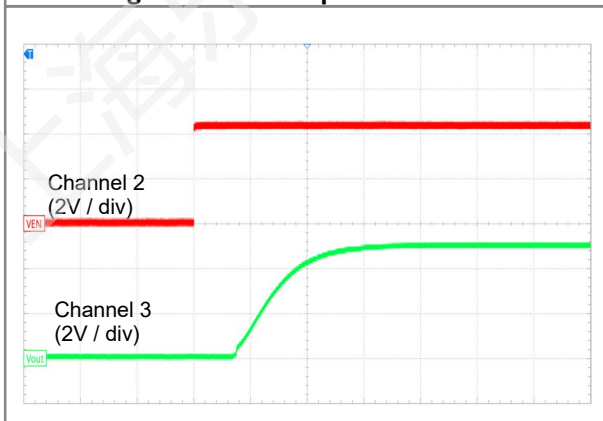
Figure 33. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=4.3→0V, V_{OUT}=3.3V, No Load

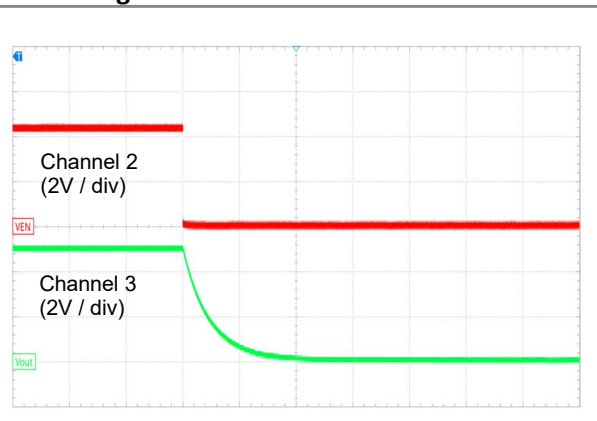
Figure 34. Shut-Down with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=6.0V, EN=0→6.0V, V_{OUT}=5.0V, No Load

Figure 35. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=6.0V, EN=6.0→0V, V_{OUT}=5.0V, No Load

Figure 36. Shut-Down with Enable

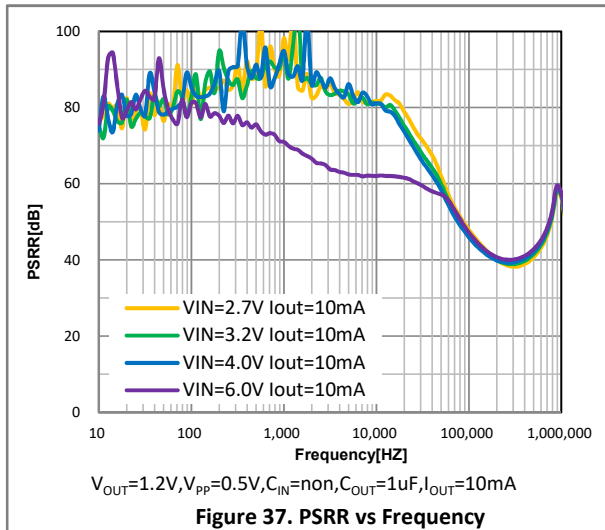


Figure 37. PSRR vs Frequency

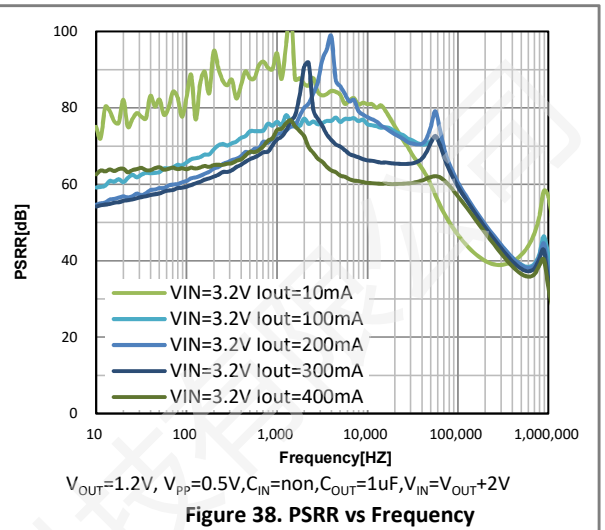


Figure 38. PSRR vs Frequency

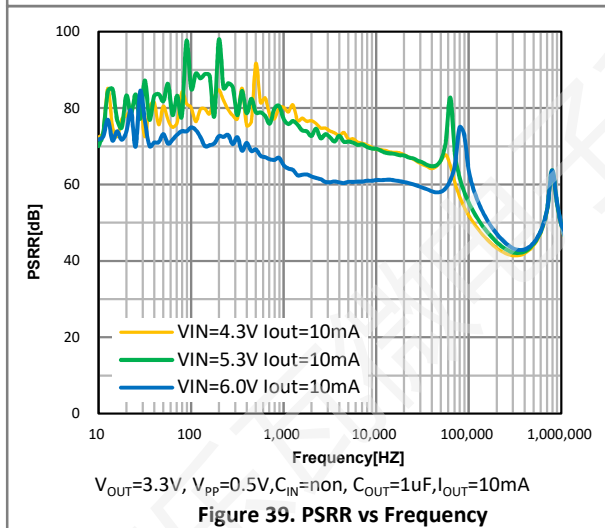


Figure 39. PSRR vs Frequency

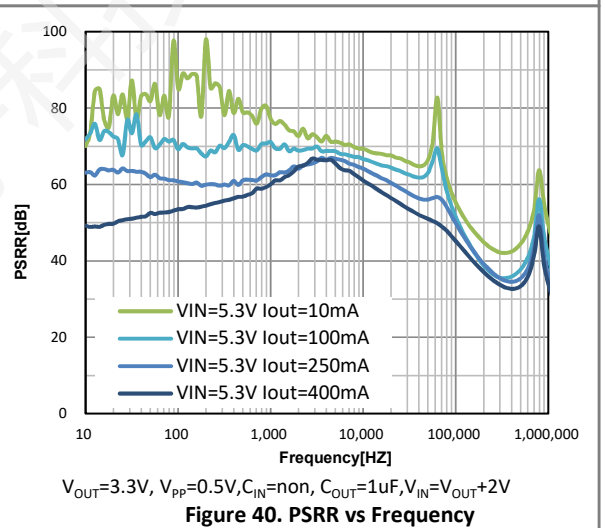


Figure 40. PSRR vs Frequency

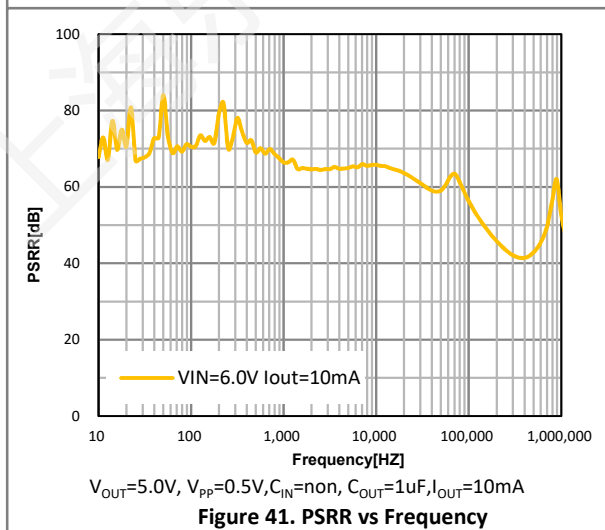


Figure 41. PSRR vs Frequency

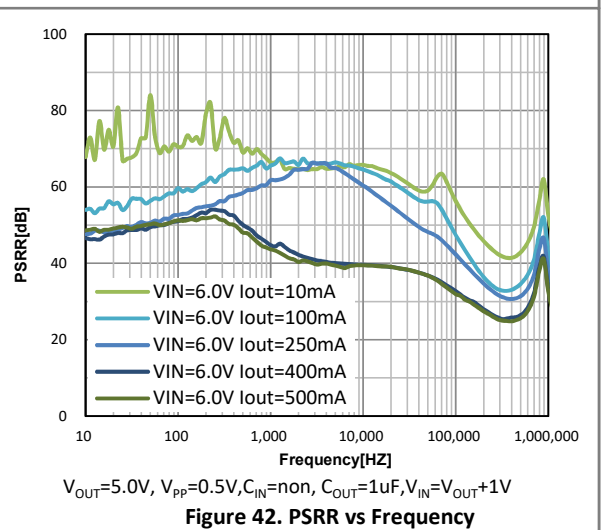


Figure 42. PSRR vs Frequency

APPLICATION INFORMATION:

- **Input Capacitor Selection**

Like any low-dropout regulator, the external capacitors used with the LW58XX Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is $\geq 1\mu\text{F}$ on the LW58XX Series input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

- **Layout considerations**

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device.

- **Output Capacitor Selection**

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW58XX Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ on the LW58XX Series output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LW58XX Series and returned to a clean analog ground.

ORDER INFORMATION:

LW58①②③④⑤⑥

Designator	Item	Symbol	Description
①②	Output Voltage	10~50	e.g. 2.8V → ①=2, ②=8
③④⑤⑥	Packages	N23C	SOT23
		N23D	SOT23-3L
		A23E	SOT23-5L
		N11E	DFN1x1-4L

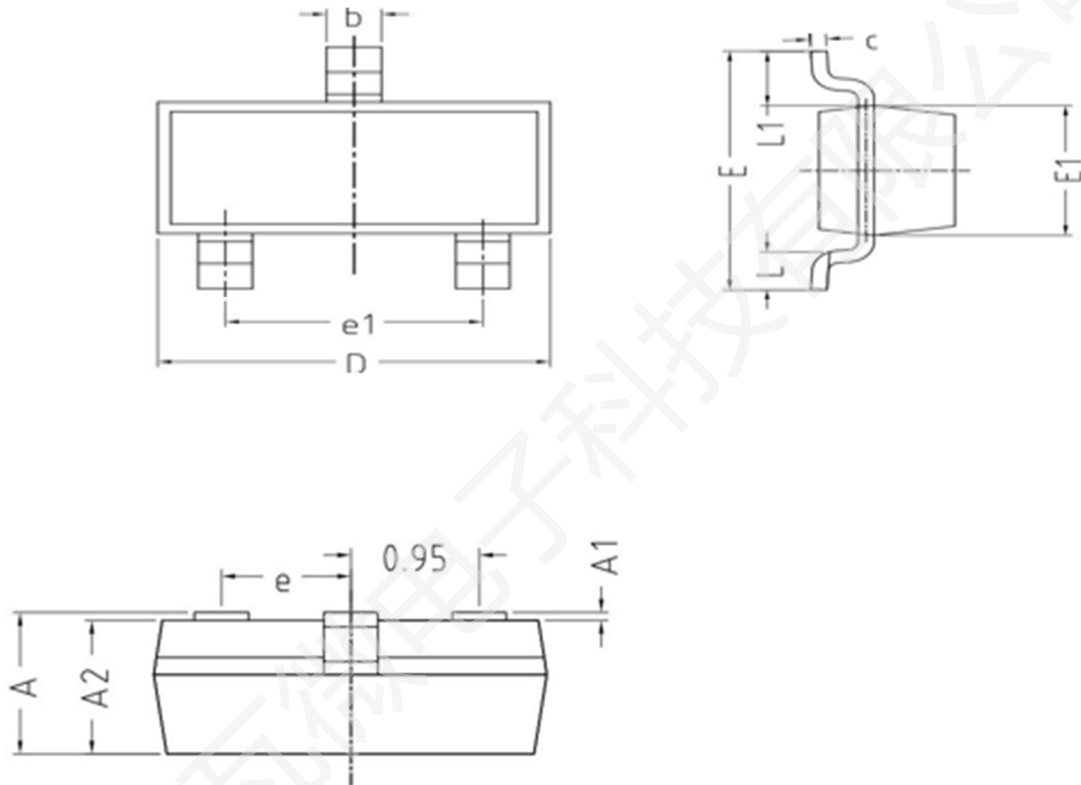
Part #	Output Voltage	Package	Shipping
LW5810N23C	1.0V	SOT23	3000 Pcs/ Tape & Reel
LW5812N23C	1.2V		
LW5815N23C	1.5V		
LW5818N23C	1.8V		
LW5825N23C	2.5V		
LW5828N23C	2.8V		
LW5830N23C	3.0V		
LW5833N23C	3.3V		
LW5836N23C	3.6V		
LW5842N23C	4.2V		
LW5850N23C	5.0V		
LW5810N23D	1.0V	SOT23-3L	3000 Pcs/ Tape & Reel
LW5812N23D	1.2V		
LW5815N23D	1.5V		
LW5818N23D	1.8V		
LW5825N23D	2.5V		
LW5828N23D	2.8V		
LW5830N23D	3.0V		
LW5833N23D	3.3V		
LW5836N23D	3.6V		
LW5842N23D	4.2V		
LW5850N23D	5.0V		

Part #	Output Voltage	Package	Shipping
LW5810A23E	1.0V	SOT23-5L	3000 Pcs/ Tape & Reel
LW5812A23E	1.2V		
LW5815A23E	1.5V		
LW5818A23E	1.8V		
LW5825A23E	2.5V		
LW5828A23E	2.8V		
LW5830A23E	3.0V		
LW5833A23E	3.3V		
LW5836A23E	3.6V		
LW5842A23E	4.2V		
LW5850A23E	5.0V		
LW5810N11E	1.0V		
LW5812N11E	1.2V		
LW5815N11E	1.5V		
LW5818N11E	1.8V		
LW5825N11E	2.5V		
LW5828N11E	2.8V		
LW5830N11E	3.0V		
LW5833N11E	3.3V		
LW5836N11E	3.6V		
LW5842N11E	4.2V		
LW5850N11E	5.0V		

If customers have special output voltage requirements, please contact us.

PACKAGE OUTLINE:

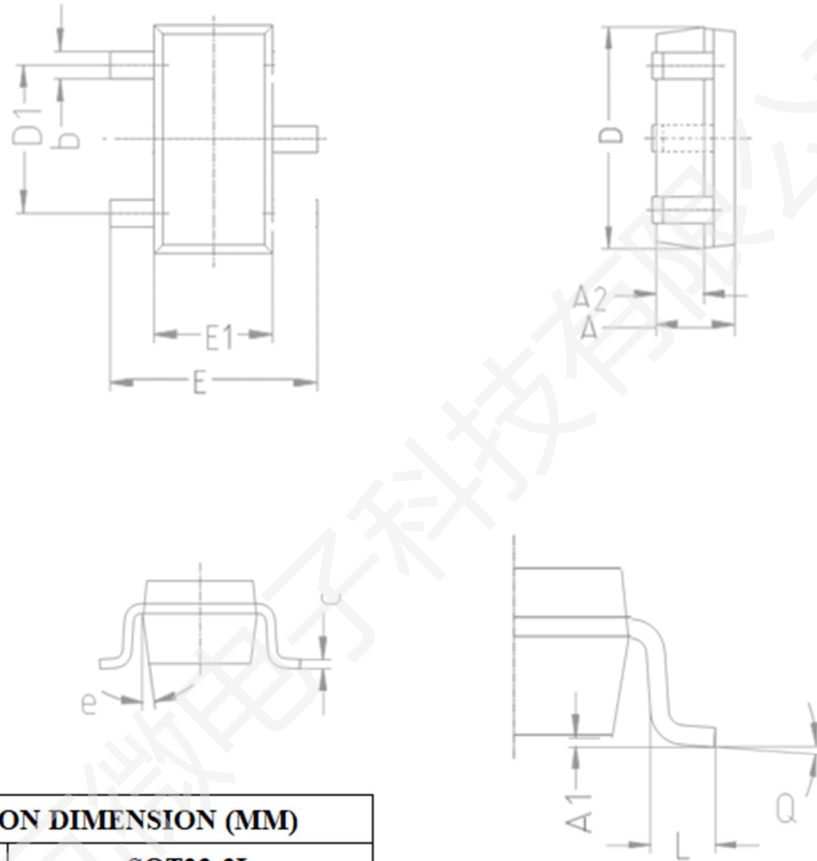
SOT23 Package



COMMON IN DIMENSION (MM)

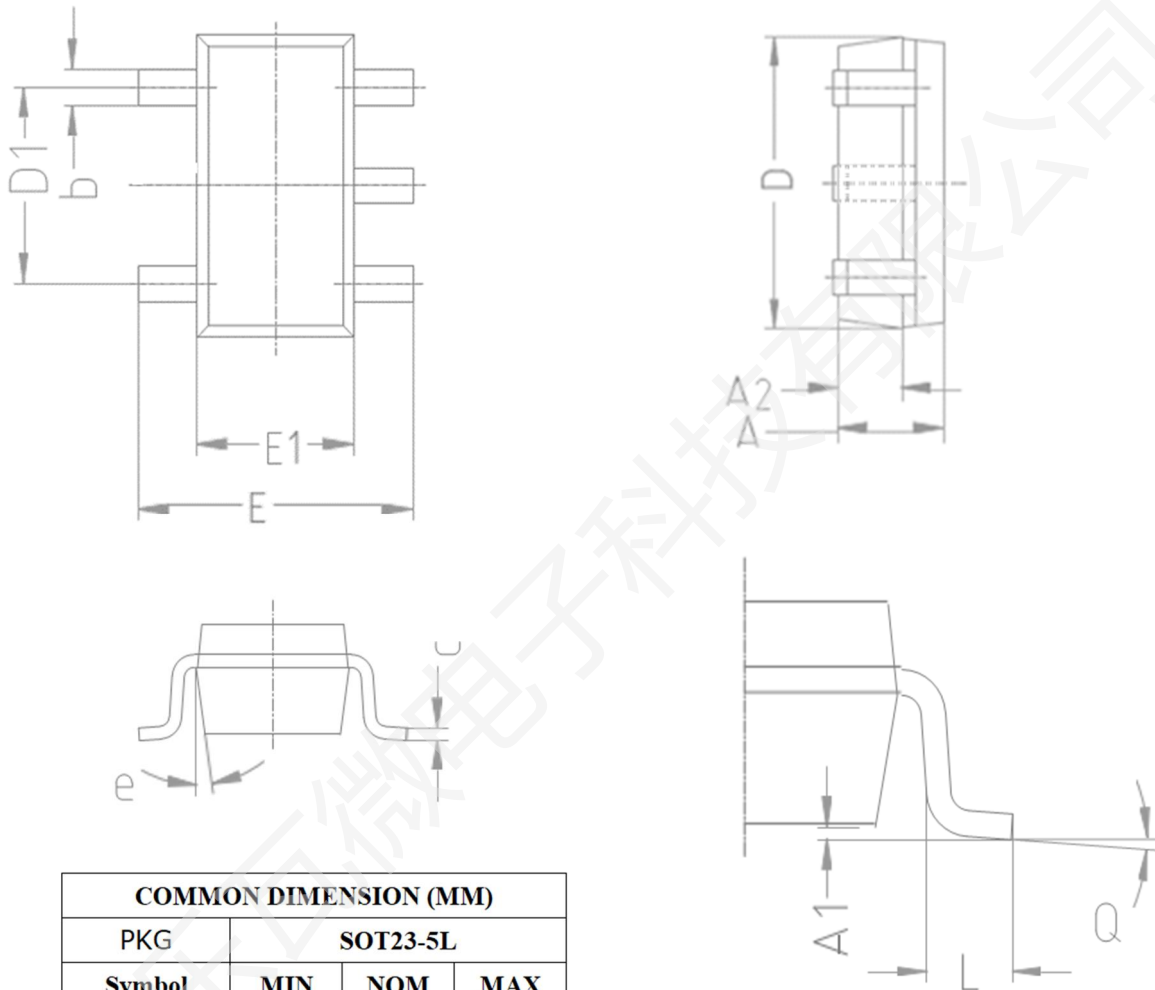
Symbol	Min.	Nom.	Max.
A	0.900	1.050	1.150
A1	0.000	0.050	0.100
A2	0.900	1.000	1.050
b	0.300	0.400	0.500
C	0.100	0.175	0.250
D	2.800	2.900	3.000
E	2.250	2.400	2.550
E1	1.200	1.300	1.400
e	0.950 TYP		
e1	1.800	1.900	2.000
L	0.290	0.395	0.500
L1	0.550REF		

SOT23-3L Package



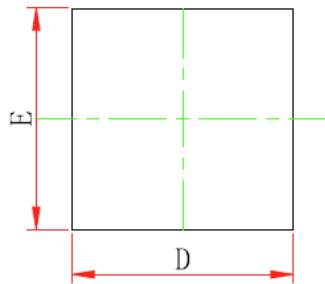
COMMON DIMENSION (MM)			
PKG	SOT23-3L		
Symbol	MIN	NOM	MAX
A	1.050	1.100	1.150
A1	0.010	0.060	0.150
A2	0.640	0.670	0.700
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.925	2.980
D1	1.800	1.900	2.000
E	2.650	2.825	3.000
E1	1.550	1.610	1.670
L	0.300	0.450	0.600
e	8°		
Q	0°	4°	8°

SOT23-5L Package

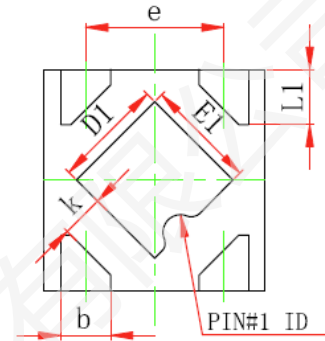


COMMON DIMENSION (MM)			
PKG	SOT23-5L		
Symbol	MIN	NOM	MAX
A	1.050	1.100	1.150
A1	0.010	0.060	0.150
A2	0.640	0.670	0.700
b	0.300	0.350	0.400
c	0.125	0.150	0.175
D	2.870	2.925	2.980
D1	1.800	1.900	2.000
E	2.650	2.800	2.950
E1	1.550	1.610	1.670
L	0.300	0.450	0.600
e	8°		
Q	0°	4°	8°

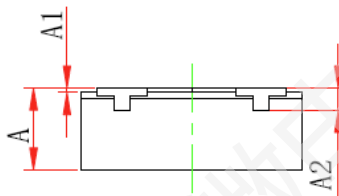
DFN1x1-4L Package



TOP VIEW
[顶视图]



BOTTOM VIEW
[背视图]



SIDE VIEW
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.335	0.405	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.100REF.		0.004REF.	
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.450	0.550	0.018	0.022
E1	0.450	0.550	0.018	0.022
k	0.195REF.		0.0077REF.	
b	0.175	0.275	0.007	0.011
e	0.575	0.675	0.023	0.027
L1	0.200	0.300	0.008	0.012

Revision History:

Revision	Date	Descriptions
Rev 0.1	Dec.2022	Initial Version
Rev 0.2	Feb.2023	Adjust characteristic
Rev 1.0	May.2023	Release Version
Rev 1.1	Jun.2023	Update Eletrical Characteristcs
Rev 1.2	Feb.2026	Update Eletrical Characteristcs
Rev 1.3	Feb.2026	Update Eletrical Characteristcs & Package Outline
Rev 1.4	Mar.2026	Add Package SOT23-3L

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Mailing Address: Unit 02&04&05, 10th Floor, Building 5, No.666 Shengxia Road, No.122 Yindong Road,
China (Shanghai) Pilot Free Trade Zone
Shanghai Lewa Micro-electronics Technology Co., Ltd