LKAD9653QF-100 type Quad-channel 16-bit 100MSPS ADC Product Manual

LKAD9653QF-100 Quad -Channel 16-Bit 100MSPS ADC

1 FEATURES

- 1.8 V supply operation
- Low power: 80 mW per channel at 100 MSPS
- SNR = 78.6 dBFS at 10 MHz (2.0 V p-p input span)
- SFDR = 90 dBc at 10 MHz (2.0 V p-p input span)
- DNL = ±0.7 LSB; INL = ±4.5 LSB (2.0 V p-p input span)
- Serial LVDS (700 mV p-p or 400 mV p-p swing optional)
- 650 MHz full power analog bandwidth
- V p-p input voltage range (supports up to 2.6 V p-p)
- SPI control for flexible configuration
- Multi-chip synchronization function
- Operating temperature: –40°C to +85°C
- Package: 48-lead QFN (7 mm × 7 mm × 0.75 mm)

2 APPLICATION

- Medical ultrasound and MRI
- High-Speed Imaging
- Orthogonal Radio Receiver
- Diversity Radio Receiver
- Test Equipment

3 OVERVIEW

The LKAD9653QF-100 is a four-channel, 16-bit, 1 00MSPS analog-to-digital converter (ADC) with built-in on-chip sample-and-hold circuitry. It operates from a single 1.8V supply and uses an LVPECL/CMOS/LVDS compatible sampling rate clock signal to fully utilize its performance.

For most applications, no external reference voltage source or driver is required. It features an automatic sampling rate multiplier clock to obtain the appropriate LVDS serial data rate; it provides a data clock output (DCO) for capturing data at the output, and a frame clock output (FCO) for sending new output bytes. Each channel can be individually shut down.

Device Information

Model	Packaging	Package Size
LKAD9653QF-100	QFN48	7.00mm × 7.00mm × 0.75mm

TABLE OF CONTENTS

4 PIN LAYOUT AND FUNCTION DESCRIPTION

4.1 PIN ARRANGEMENT

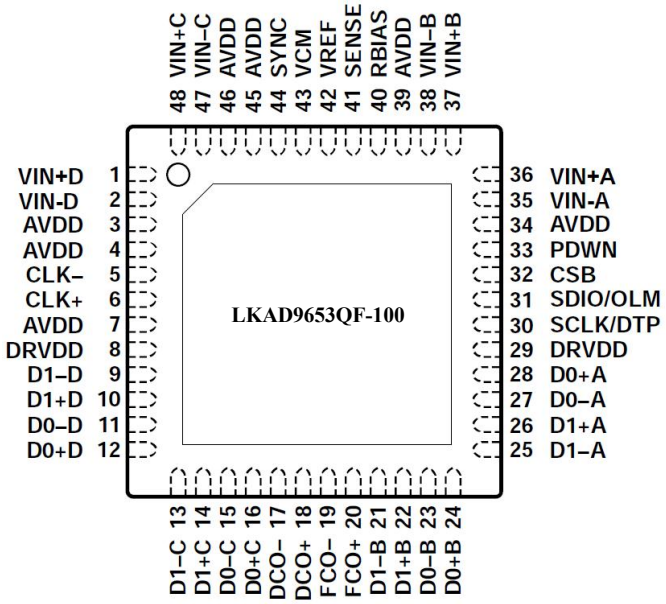


Figure 1 Pin arrangement diagram (top view)

Table 1 Pin Description

Pin No.	Mnemonic	Function
1, 2	VIN+D, VIN-D	ADC D Analog Input True and Complement.
48, 47	VIN+C, VIN-C	ADC C Analog Input True and Complement.
37, 38	VIN+B, VIN-B	ADC B Analog Input True and Complement.
36, 35	VIN+A, VIN-A	ADC A Analog Input True and Complement.
9, 10	D1−D, D1+D	Channel D Digital Outputs (D1).
11, 12	D0−D, D0+D	Channel D Digital Outputs (D0).
13, 14	D1−C, D1+C	Channel C Digital Outputs (D1).
15, 16	D0−C, D0+C	Channel C Digital Outputs (D0).
21, 22	D1−B, D1+B	Channel B Digital Outputs (D1).
23, 24	D0−B, D0+B	Channel B Digital Outputs (D0).
25, 26	D1−A, D1+A	Channel A Digital Outputs (D1).
27, 28	D0−A, D0+A	Channel A Digital Outputs (D0).
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output (Bidirectional SPI Data)/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up. For applications not using the SPI, connect this pin to AVDD.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device; PDWN low = run device, normal operation.
5, 6	CLK-, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
17, 18	DCO−, DCO+	Data Clock Outputs.

Pin No.	Mnemonic	Function
19, 20	FCO−, FCO+	Frame Clock Outputs.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	V_{REF}	Voltage Reference Input and Output.
43	VCM	Analog Output at Midsupply Voltage. Sets the common mode of the analog inputs.
44	SYNC	Digital Input. SYNC input to clock divider.
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply Pins.
8, 29	DRVDD	Digital Output Driver Supply.
49	AGND	Analog Ground. The device must be connected to ground for proper operation.

5 ELECTRICAL PROPERTIES

5.1 ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Minimum Value	Maximum Value	Unit
Power Supply Voltage	AVDD	-0.3	+2.0	V
	DRVDD	-0.3	+2.0	V
Input voltages (VIN±x, CLK±, SYNC, PDWN, RBIAS, VREF, SENSE)	V_{IN}	-0.3	AVDD+2.0	V
Input voltages (SCLK, SDIO, CSB)		-0.3	DRVDD+2.0	V
Digital output voltages (D0±x, D1±x, DCO±, FCO±)	V_{OUT}	-0.3	DRVDD+2.0	V
Lead wire soldering temperature resistance (5s)	T_h	240	250	℃
Junction temperature	T_j	150		℃
Storage temperature	T_{STG}	-65	+150	℃

5.2 RECOMMENDED WORKING CONDITIONS

parameter	symbol	Minimum value	Typical value	Maximum value	unit
Power Supply Voltage	AVDD	-	1.8	-	V
	DRVDD	-	1.8	-	V
Operating Temperature	T_A	- 40	-	8 5	℃

5.3 DC ELECTRICAL CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input at −1.0 dBFS, VREF = 1.0 V, DCS off, TA = −40°C to +85°C, unless otherwise noted.

parameter	Minimum value	Typical value	Maximum value	unit
Resolution	-	16	-	Bit
Integral Nonlinearity (INL)	-	±4.5	-	LSB
Differential Nonlinearity (DNL)	-	±0.7	-	LSB
Internal Reference Source Output Voltage (1.0V Mode)	-	1.0	-	V
Input reference (V_{REF} = 1.0V)	-	2.3	-	LSBrms
Differential Input Voltage (V_{REF} = 1.0V)	-	2.0	-	Vp-p

Common-Mode Input Voltage		-	0.9	-	V
Power Supply	I_{AVDD}	-	320	-	mA
	I_{DRVDD}(ANSI-644 Mode)	-	80	-	mA
	I_{DRVDD}(Reduced Range Mode)	-	65	-	mA
Total Power Consumption	DC Input	-	610	-	mW
	Sine Wave Input (Four Channels Including Output Drivers, ANSI-644 Mode)	-	720	-	mW
	Sine Wave Input (Four Channels Including Output Drivers, Reduced Range Mode)	-	693	-	mW

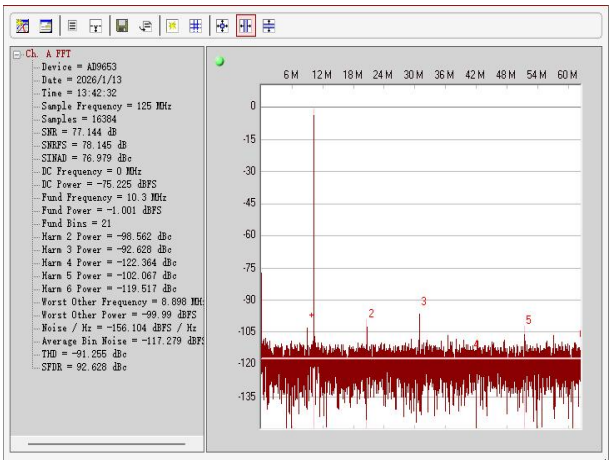
5.4 ALTERNATING CURRENT CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input at −1.0 dBFS; VREF = 1.0 V, DCS off, fSAMPLE = 100 MSPS, TA = −40°C to +85°C, unless otherwise noted.

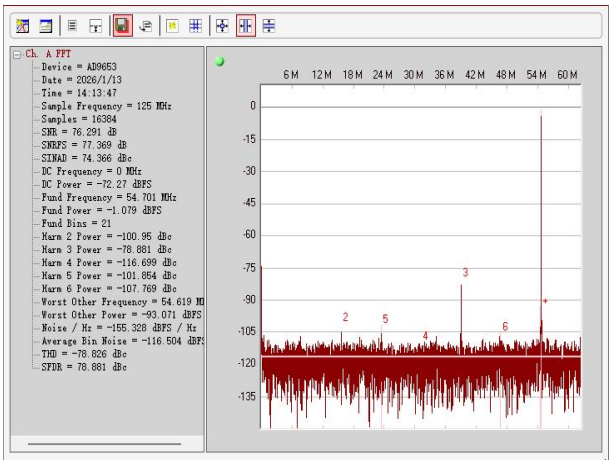
Parameter	Minimum Value	Typical Value	Maximum Value	Unit
SNR				
f_{IN} = 10MHz	-	77.4	-	dBFS
f_{IN} = 70MHz	-	76.47	-	dBFS
f_{IN} = 1 51 MHz	-	74.19	-	dBFS
f_{IN} = 245 MHz	-	71.72	-	dBFS
f_{IN} = 305 MHz	-	69.99	-	dBFS
SINAD				
f_{IN} = 10MHz	-	75.7	-	dBFS
f_{IN} = 70MHz	-	75.01	-	dBFS
f_{IN} = 1 51 MHz	-	73.19	-	dBFS
f_{IN} = 245 MHz	-	68.57	-	dBFS
f_{IN} = 305 MHz	-	66.25	-	dBFS
ENOB				
f_{IN} = 10MHz	-	12.28	-	Bits
f_{IN} = 70MHz	-	12.17	-	Bits
f_{IN} = 1 51 MHz	-	11.87	-	Bits
f_{IN} = 245 MHz	-	11.1	-	Bits
f_{IN} = 305 MHz	-	10.71	-	Bits
THD				
f_{IN} = 10MHz	-	-80.6	-	dBc
f_{IN} = 70MHz	-	-80.72	-	dBc
f_{IN} = 1 51 MHz	-	-80.07	-	dBc
f_{IN} = 245 MHz	-	-71.44	-	dBc
f_{IN} = 305 MHz	-	-68.63	-	dBc
SFDR				
f_{IN} = 10MHz	-	83.1	-	dBc

f_{IN} = 70MHz	-	81.8	-	dBc
f_{IN} = 151 MHz	-	80.85	-	dBc
f_{IN} = 245 MHz	-	72.73	-	dBc
f_{IN} = 305 MHz	-	70.07	-	dBc
Worst second harmonic				
f_{IN} = 10MHz	-	-84.6	-	dBc
f_{IN} = 70MHz	-	-87.41	-	dBc
f_{IN} = 151 MHz	-	-85.3	-	dBc
f_{IN} = 245 MHz	-	-72.73	-	dBc
f_{IN} = 305 MHz	-	-70.07	-	dBc

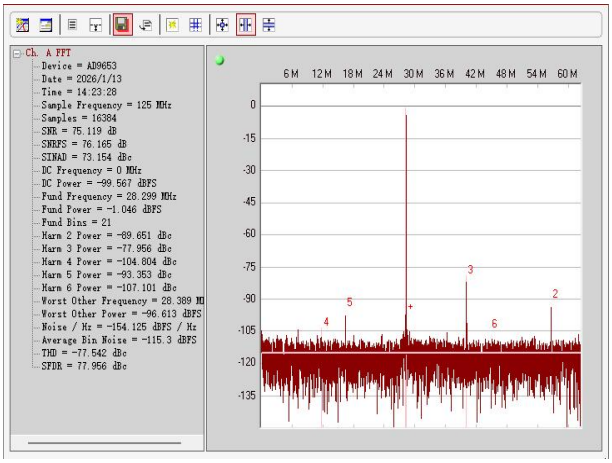
6 TYPICAL PERFORMANCE CHARACTERISTICS



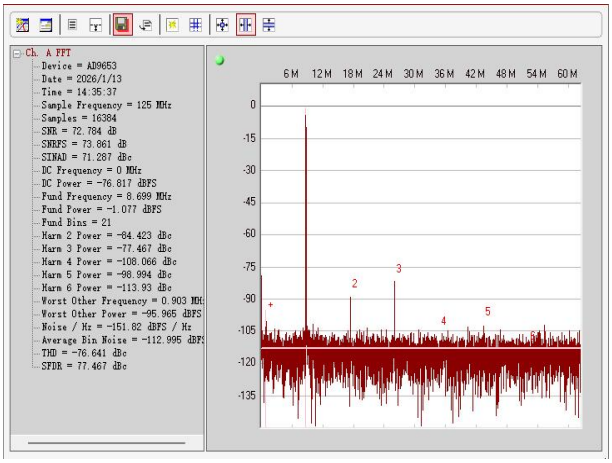
Single-Tone 16k FFT（fin=10.3M，fs=100MSPS，Vref=1V，socket）



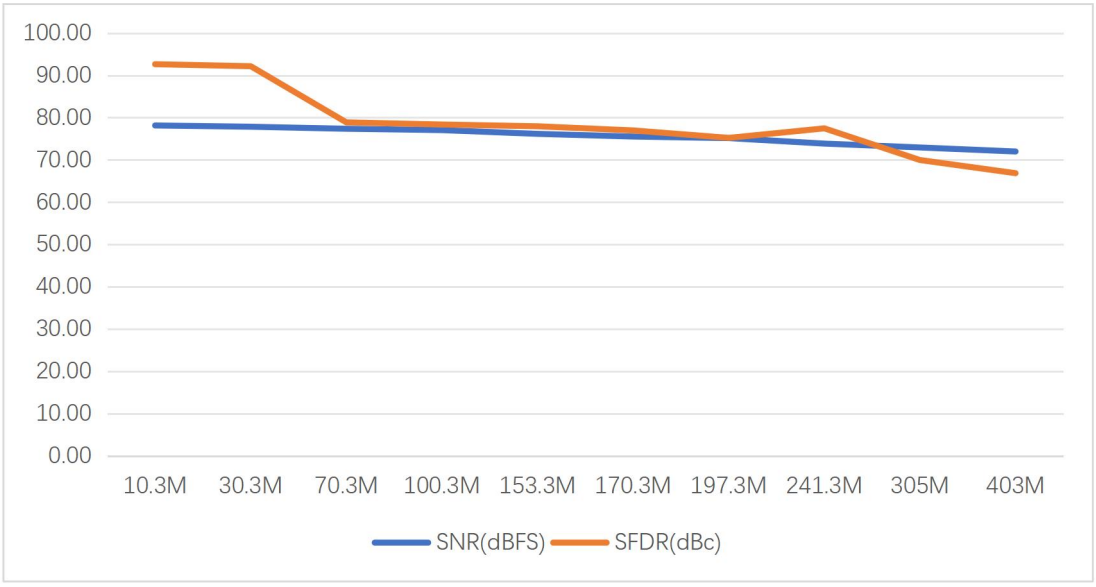
Single-Tone 16k FFT（fin=70.3M，fs=100MSPS，Vref=1V，socket）



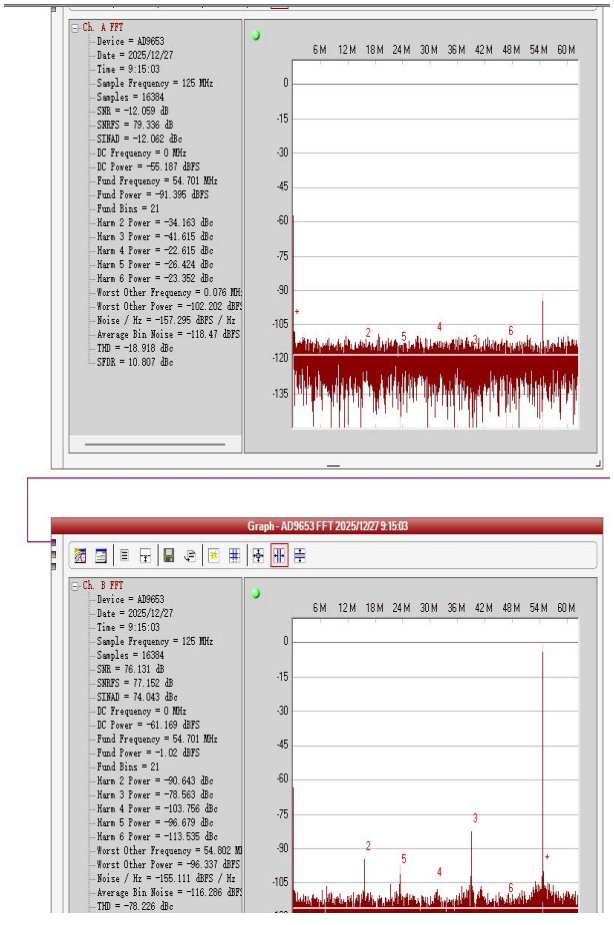
Single-Tone16k FFT（fin=153.3M，fs=100MSPS，Vref=1V，socket）



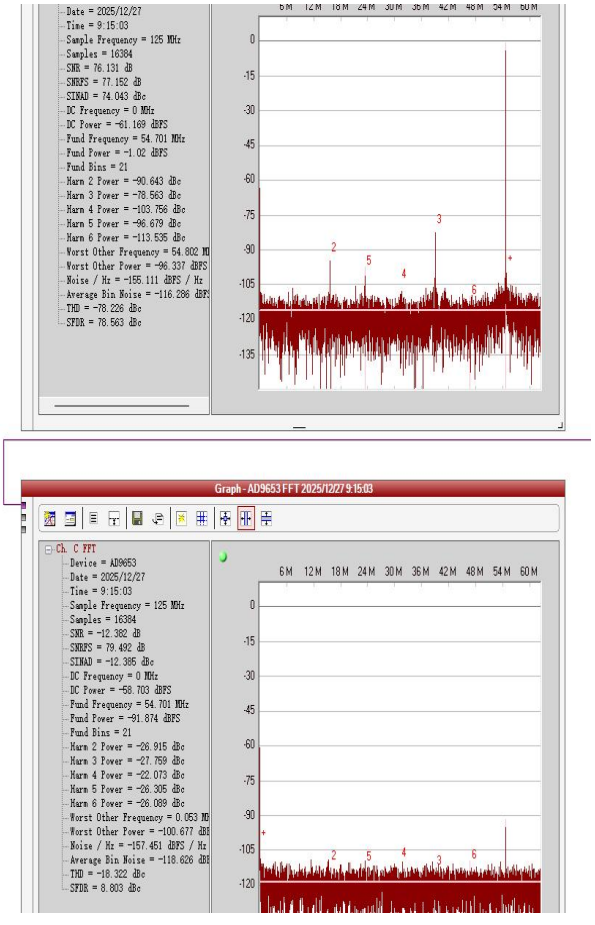
Single-Tone 16k FFT（fin=241M，fs=100MSPS，Vref=1V，socket）



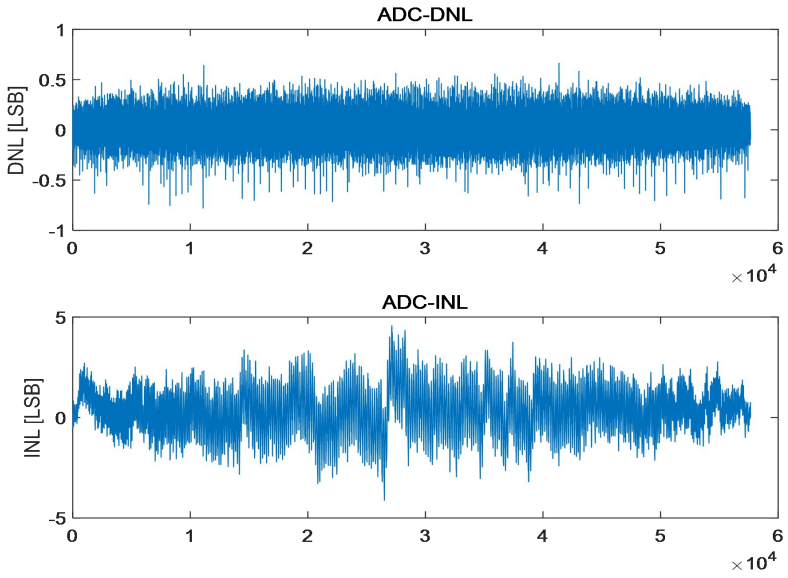
SNR/SFDR vs f_{IN}（Fs=100MSPS，V_{REF}=1V）



Isolation：f_{IN}=70.3MHz，B to A



Isolation：f_{IN}=70.3MHz，B to C



DNL & INL （f_{IN}=10.3Mhz，fs=100MSPS，V_{REF}=1V）

7 WORKING PRINCIPLE

7.1 FUNCTIONAL BLOCK DIAGRAM

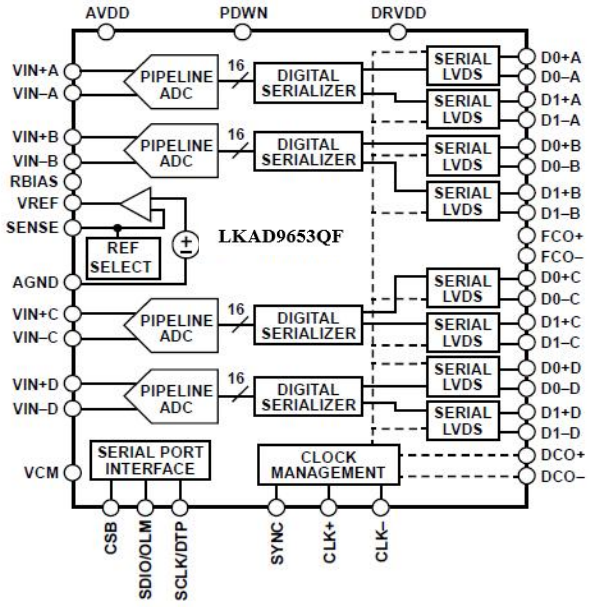


Figure 2. Functional block diagram of the chip

The LKAD9653QF-100 is a multistage, pipelined ADC where each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16- bit result in the digital correction logic. The serializer transmits this converted data in a 16- bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier. The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. The last stage simply consists of a 4-bit flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

7.2 POWER SUPPLY

When connecting power to the LKAD9653QF-100, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

7.3 REFERENCE VOLTAGE SOURCE

The device incorporates a stable and accurate voltage reference. The VREF pin can be configured to generate a user-selectable reference voltage using the internal 1.0 V reference, an externally applied 1.0 V to 1.3 V reference, or an external resistor applied to the internal reference. The VREF pin should be externally bypassed to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

Table 2 Reference Voltage Configuration Table

Model	SENSE voltage (V)	VREF (V)	Difference Range (VPP)
Internal Reference (Fixed)	AGND ~ 0.2	1.0, Internal	2.0
Internal Reference (Programmable)	Connect To External Voltage Divider Resistor	0.5×(1+R2/R1)	2 × V_{REF}
External Reference (Fixed)	AVDD	1.0 to 1.3, applied to the external V_{REF} pin.	2.0～2.6

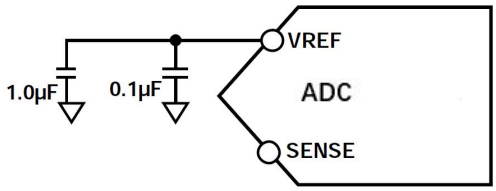
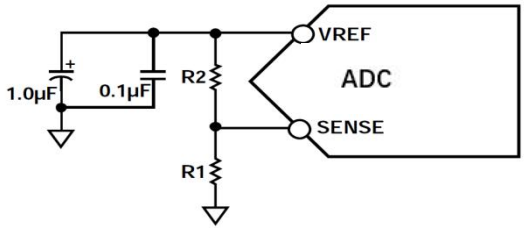


Figure 3 1.0v Internal Reference Voltage Configuration



Note: VREF = 0.5 × (1 + R2/R1) , where 7kΩ ≤ (R1 + R2) ≤ 10kΩ.

Figure 4 Programmable Internal Reference Voltage Configuration

7.4 CLOCK INPUT

For optimum performance, clock the LKAD9653QF-100 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no external bias.

7.4.1 CLOCK INPUT OPTION

The LKAD9653QF-100 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of primary concern.

For clock frequencies from 100 MHz to 1 GHz, an RF balun configuration is recommended, as shown in Figure 5. For clock frequencies from 20 MHz to 200 MHz, an RF transformer configuration is recommended, as shown in Figure 6. Using an RF balun or RF transformer, a single-ended signal from a low-jitter clock source can be converted into a differential signal.

Back-to-back Schottky diodes connected across the transformer/balun secondary winding limit clock excursions into the device to approximately 0.8 V p-p differential. This prevents large voltage swings from feeding through to other portions of the device while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, diode capacitance comes into play at frequencies above 500 MHz. Care must be taken in choosing the appropriate signal limiting diode.

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins, as shown in Figure 7.

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 8.

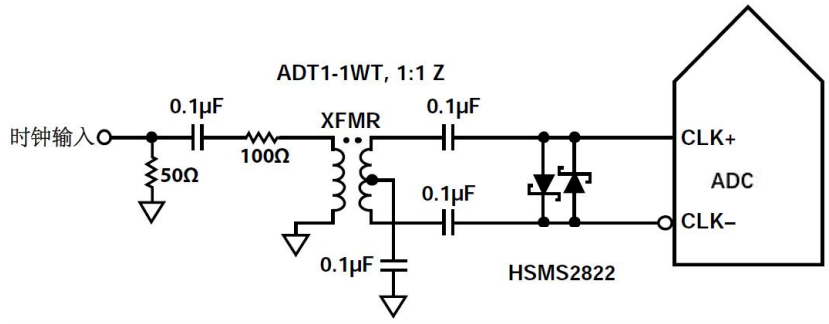


Figure 5 Transformer-Coupled Differential Clock

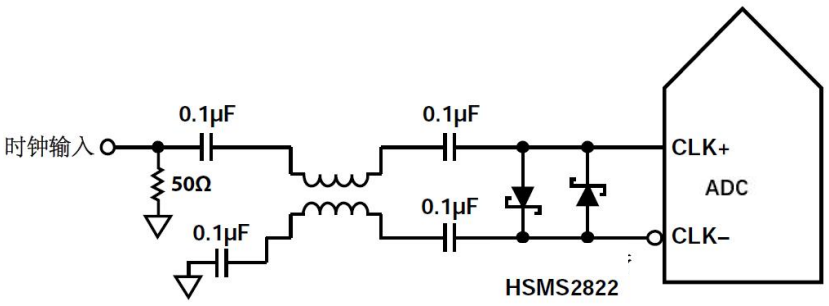


Figure 6. Balun-Coupled Differential Clock

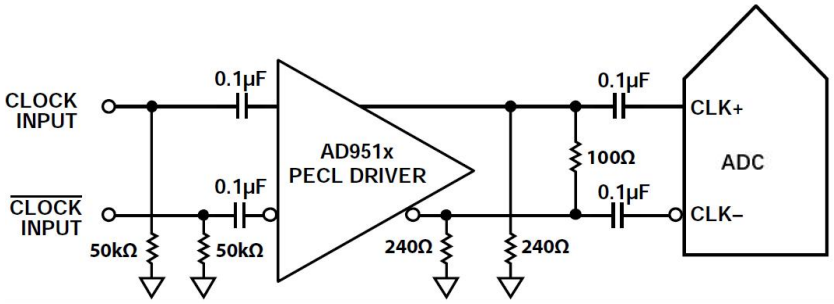


Figure 7 Differential PECL sampling clock

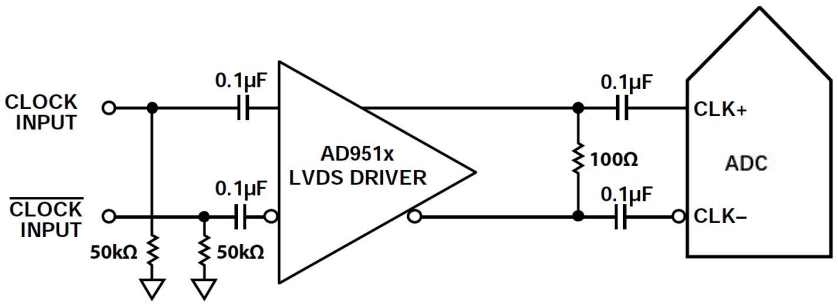


Figure 8. Differential LVDS Sampling Clock

7.4.2 INPUT CLOCK DIVIDER

The device contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. The clock divider can be synchronized using the external SYNC input. Bit 0 of Register 0x109 allows the clock divider to be resynchronized upon receiving a SYNC signal. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

7.4.3 CLOCK DUTY CYCLE

Typically, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The device contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This feature minimizes performance degradation in cases where the clock input duty cycle deviates from 50% by more than the specified ±5%. Noise and distortion performance are nearly flat for a wider range of duty cycles with the DCS on.

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency change before the DCS loop is relocked to the input signal.

7.4.4 JITTER CONSIDERATION

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (fA) due only to aperture jitter (tJ) can be calculated by

$$\text{SNR Degradation} = 20\log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the device. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

7.5 ANALOG INPUT

The analog inputs of the device are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. The device can function over a wider common-mode range with reasonable performance; for optimum performance, setting VCM = AVDD/2 is recommended. An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be bypassed to ground by a 0.1 µF capacitor.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. The input span of the device is dependent on the reference voltage (see Table 2).

Optimum performance can be achieved by driving the analog inputs differentially. For baseband applications, using a differential double balun configuration to drive the device provides excellent performance and a flexible interface for the ADC, as shown in Figure 9. In applications where SNR is a critical parameter, differential transformer coupling is recommended in the input configuration, as shown in Figure 10, because the noise performance of most amplifiers is insufficient to realize the true performance of the device. Regardless of the configuration used, the series resistor (R) and shunt capacitor (C) values depend on the input signal frequency. For high-to-mid frequency inputs, it may be necessary to reduce or even remove these components. Driving the device inputs in a single-ended manner is not recommended.

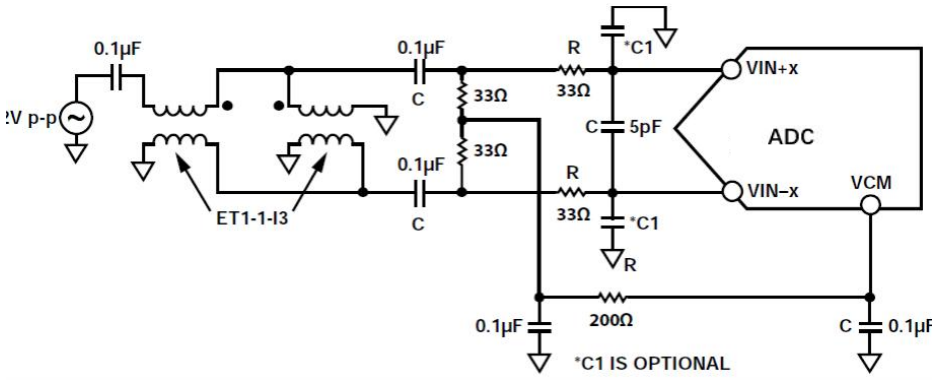


Figure 9. Differential dual balun input configuration (for baseband applications)

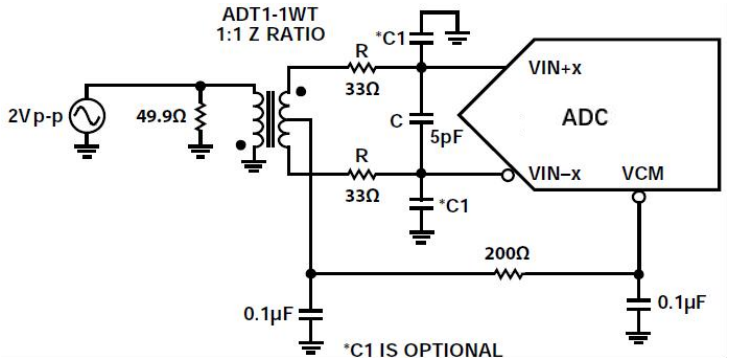


Figure 10. Differential transformer coupling configuration (for baseband applications)

7.6 DIGITAL OUTPUT

The device differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver. When operating in reduced range mode, the output current is reduced to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The device LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 24 inches and that the differential output traces be close together and at equal lengths.

It is the user's responsibility to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination of all four outputs to drive longer trace lengths. This can be achieved by programming Register 0x15. Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used.

The format of the output data is twos complement by default. An example of the output coding format can be found in Table 3. To change the output data format to offset binary, see Section 6.8.

In DDR mode, data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 16 bits times the sample clock rate, with a maximum of 500 Mbps per channel. The lowest typical conversion rate is 20 MSPS. For more information on using this feature, see Section 6.8.

Two output clocks are provided to assist in capturing data from the device. The DCO is used to clock the output data and is equal to four times the sample clock (CLK) rate for the default mode of operation. Data is clocked out of the device one byte at a time and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. The FCO is used to signal the start of a new output byte and is equal to the sample clock rate in 1× frame mode.

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO+ and DCO− timing, as shown in Figure 4, is 90° relative to the output data edge. In default mode, the MSB is first in the data output serial stream. This can be inverted so that the LSB is first in the data output serial stream by using the SPI.

Table 3 Output Encoding Format

Input (V)	Condition(V)	Offset Binary Output Mode	Binary Two's Complement Mode	Graymall
VIN+ -VIN-	<-VREF-0.5LSB	0000 0000 0000 0000	1000 0000 0000 0000	0000 0000 0000 0000
VIN+-VIN-	= -VREF	0000 0000 0000 0000	1000 0000 0000 0000	0000 0000 0000 0000
VIN+-VIN-	= 0	1000 0000 0000 0000	0000 0000 0000 0000	1100 0000 0000 0000
VIN+-VIN-	= VREF-1.0LSB	1111 1111 1111 1111	0111 1111 1111 1111	1000 0000 0000 0000
VIN+-VIN-	= VREF-0.5LSB	1111 1111 1111 1111	0111 1111 1111 1111	1000 0000 0000 0000

7.6.1 CSB PIN

For applications that do not require SPI operation mode, the CSB pin should be connected to AVDD. Connecting CSB high will ignore all SCLK and SDIO information. Note that when the CSB pin is connected to AVDD, the device's DCS is off by default and remains off until the device enters SPI mode and is controlled via SPI.

7.6.2 RBIAS PIN

To set the core bias current of the ADC, a 10kΩ±1% resistor should be connected from the RBIAS pin to ground.

7.6.3 SERIAL PORT INTERFACE (SPI)

The device serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port.

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin. The SCLK (serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual- purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing can be found in Figure 11. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16- bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits. In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on- chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change

direction from an input to an output at the appropriate point in the serial frame. All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB-first mode is the default on power-up and can be changed via the SPI port configuration register.

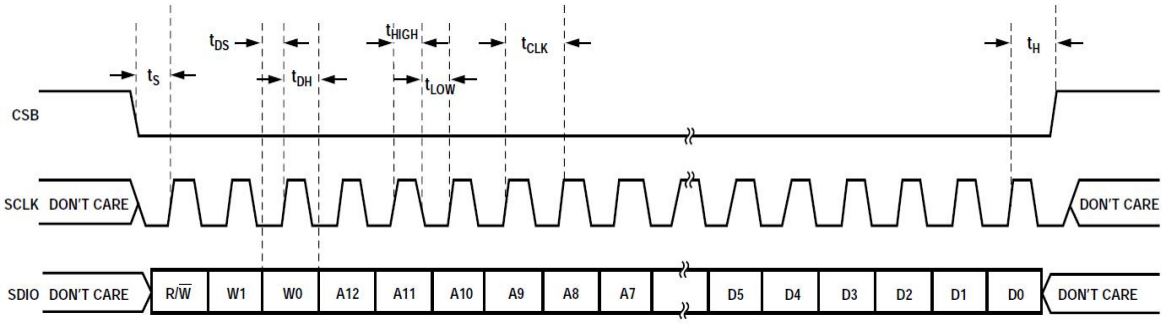


Figure 11. SPI serial interface control timing

7.6.4 HARDWARE INTERFACE

When using the SPI, the SCLK pin and the CSB pin function as inputs. The SDIO pin is bidirectional, operating as an input during write operations and as an output during readback.

When the SPI interface is not in use, certain pins serve dual functions. During device power-up, strapping these pins to DRVDD or ground configures specific features. Refer to Table X and Table Y for the strappable functions supported on the device.

7.6.5 CONFIGURATION WITHOUT THE SPI

In applications that do not use the SPI control register interface, the SDIO/OLM, SCLK/DTP, and PDWN pins are used as independent CMOS-compatible control pins. When the device is powered on, it is assumed that the user intends to use these pins as static control lines to control the output channel mode, digital test code, and power-down characteristics, respectively. In this mode, the CSB pin should be connected to AVDD to disable the serial port interface. When the device is in SPI mode, the PDWN pin (if enabled) remains active. To control power-down via SPI, the PDWN pin should be set to its default state.

7.7 DATA OUTPUT TIMING

Refer to the register list to perform different data timing controls on the chip.

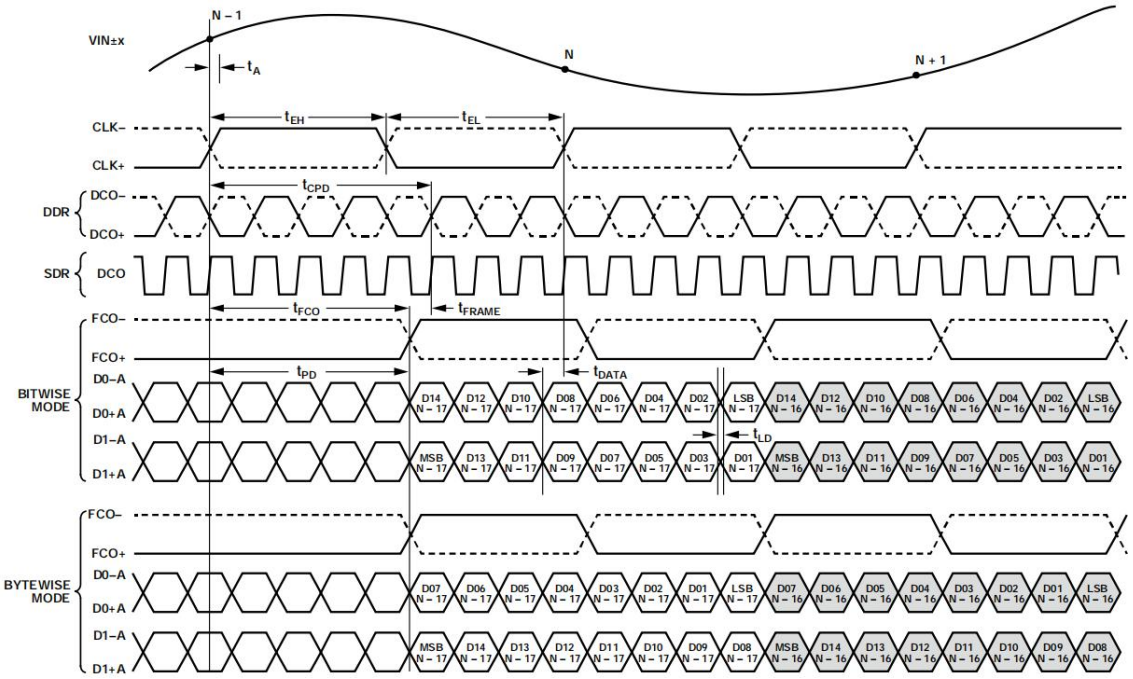


Figure 12 16-Bit DDR/SDR, Dual-Channel, 1×Frame Mode

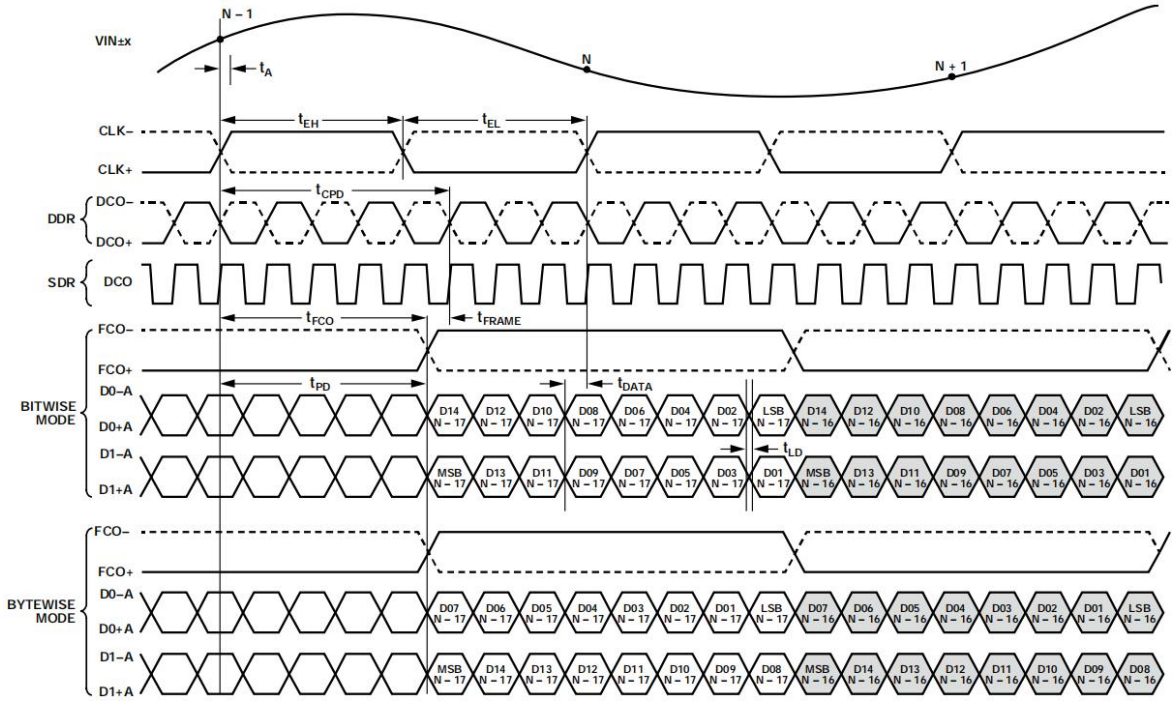


Figure 13. 16-Bit DDR/SDR, Dual Channel, 2 × Frame Mode

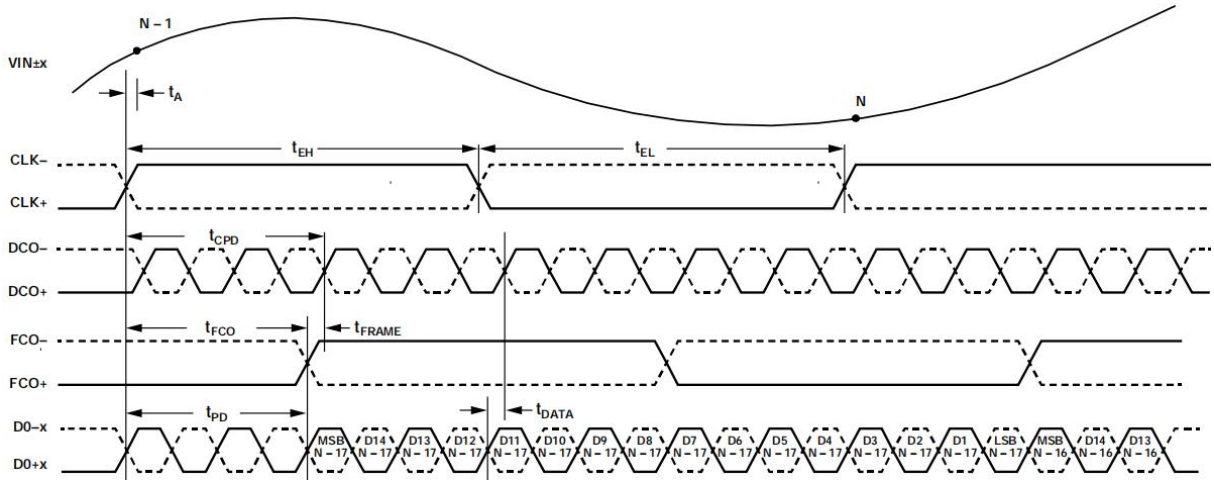


Figure 14. Word-By-Word DDR, Single Channel, 1×Frame, 16-Bit Mode

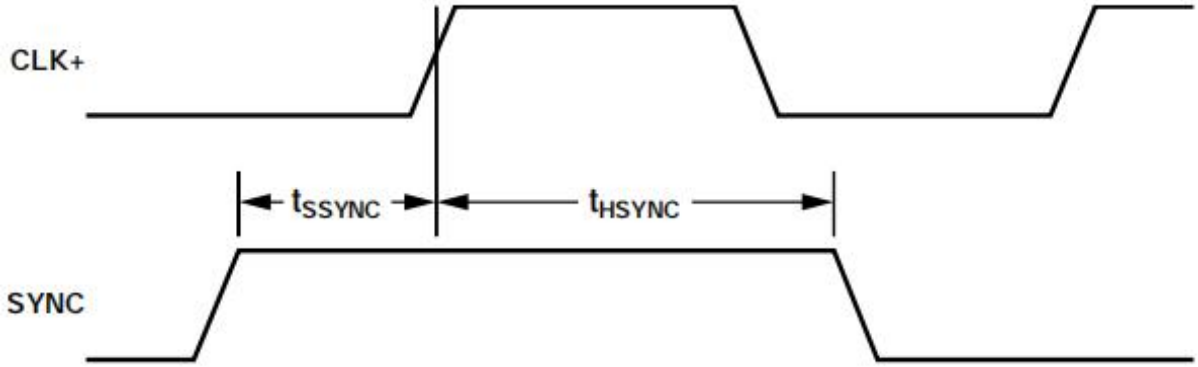


Figure 15. SYNC Input Timing Requirements

7.8 REGISTER LIST

Table 4 Memory-mapped register table

address	memory name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default value	Notes
Chip configuration register											
0x00	SPI port configuration (global)	0	LSB priority	Soft reset	1	1	Soft reset	LSB priority	0	0x18	The nibbles are mirror images of each other, ensuring that LSB-first or MSB-first registers can correctly record data regardless of the shift mode.
0x01	Chip ID	8-bit chip ID								0xB5	Read-only
0x02	Chip level	Disable	Speed rating (110 = 100MSPS)			Disable	Disable	Disable	Disable		Read-only
Channel Index and Transfer Register											
0x04	Channel Index	Disable	Disable			Data Channel D	Data Channel C	Data Channel B	Data Channel A	0x0F	By default, all four channels are selected.
0x05	Channel Index	Disable	Disable	Clock Channel DCO	Clock Channel FCO	Data Channel D	Data Channel C	Data Channel B	Data Channel A	0x3F	By default, all four channels are selected.
0xFF	Teleport	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Teleport	0x00	Data is synchronously transferred from the master shift register to the

address	memory name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default value	Notes
											slave shift register.
ADC function											
0x08	Power consumption mode (Partial)	Disable	Disable	External power-down pin function (partial) 0 = Power off, 1 = Standby	Disable	Disable	Disable	Internal power failure mode (partial) 00 = Normal operation, 01 = Complete power failure 10 = Standby, 11 = Reset		0x00	Determines the operating mode of the device
0x09	Global clock	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Duty cycle stabilizer 0 = On, 1 = Off	0x01	By default, the duty cycle stabilizer is off.
0x0B	Clock divider	Disable	Disable	Disable	Disable	Disable	Clock division ratio [2:0] 000 = 1 divider, 001 = 2 dividers, 010 = 3 dividers, 011 = 4 dividers. 100 = 5 crossovers, 101 = 6 crossovers, 110 = 7 crossovers, 111 = 8 crossovers			0x00	
0x0C	Enhanced control	Disable	Disable	Disable	Disable	Disable	Disable			0x00	Enable/disable chopper mode (This feature is not available)

address	memory name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default value	Notes
0x0D	Data output test mode (partial)	User input test mode 00 = Single 01 = Alternate 10 = Single time 11 = alternating once (This only affects the user input test mode, bits [3:0]=1000)		Generate a reset PN long sequence	Generate a short reset sequence	Output test mode 000=off, 001=midscale short, 010=positive FS, 011=negative FS, 100=alternting checkerboard, 101=PN 23sequence, 111=0/1 toggle				0x00	
0x10	Disorder adjustment	8-bit device misalignment adjustment, bits [7:0] (local) The misalignment adjustment is in LSB units, from +127 to -127 (two's complement format).								0x00	Device offset adjustment
0x14	Data output mode	Disable	LVDS amplitude 0 = 350mV 1=200mV (Global)	Disable	Disable	Disable	Disable	Output format (partial) 00 = offset binary, 01 binary two's complement		0x03	
0x15	Data output adjustment	Disable	Disable	Termination resistor of output driver 00 = None, 01 = 200Ω 10 = 100Ω, 11 = 100Ω		Disable	Disable	Output drive strength 0 = 1 × driver, 1 = 2 × driver		0x00	Determines the output properties of LVDS
0x16	DCO output	Disable	Disable	Disable	Disable	Disable	Disable			0x03	

address	memory name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default value	Notes
	delay (global)						DCO clock phase adjustment 000 = 0°, 001 = 60° 010 = 120°, 011 = 180° 100 = 240°, 101 = 300°				
0x18	VREF selection (Global)	Disable	Disable	Disable	Disable	Disable	Full-frame range selection 000=1.00VP-P, 001=1.14VP-P, 010=1.33VP-P, 011 = 1.60VP-P, 100 = 2.00VP-P (default)			0x04	Default 2.00VP-P full-frame input range
0x19	USER_PARTT 1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined test code 1LSB
0x1A	USER_PARTT 1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined test code 1MSB
0x1b	USER_PARTT 2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined test code 2LSB
0x1c	USER_PARTT 2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined test code 2MSB
0x21	Serial data output control (Global)	LSB/MSB priority 0 = MSB priority, 1 = LSB priority	SDR/DDR/lane/bit-byte wise 000 = SDR, double lane, bitwise. 001=SDR, dual lane, bytewise, 010 = DDR, dual lanes, bitwise. 011 = DDR, dual lanes, bytewise (default)			Disable	FCO frequency multiplier 0 = 1 × frame 1 = 2 ×	Serial output bit depth 00 = 16 bits		0x30	

address	memory name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default value	Notes
							frames				
0x100	Sampling rate coverage	Disable	Sampling rate coverage enable	0	0	Disable	Sampling rate 000 = 20 MSPS 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 100MSPS			0x00	Sampling rate coverage (requires transfer register, 0xFF)
0x101	User I/O Control 2	Disable	Disable	Disable	Disable	Disable	Disable	Disable	该bit我校	0x00	Disable SDIO pull-down resistors
0x102	User I/O Control 3	Disable	Disable	Disable	Disable	VCM power failure	该bit无效	Disable	Disable	0x00	VCM control
Digital control characteristics											
0x109	Synchronization control	Disable	Disable	Disable	Disable	Disable	Disable	该bit无效	Synchronous enable	0x00	

8 APPLICATION INFORMATION

8.1 POWER SUPPLY AND GROUNDING RECOMMENDATIONS

When connecting power to the device, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the device. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

8.2 EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the device. An exposed continuous copper plane on the PCB should mate to the device exposed pad, Pin 49. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 76 for a PCB layout example.

8.3 REFERENCE DECOUPLING

The VREF pin should be externally bypassed to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

8.4 SPI port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the device to keep these signals from transitioning at the converter inputs during critical sampling periods.

8.5 CROSSTALK PERFORMANCE

The device is available in a 48-lead QFN package with the input pairs on either corner of the chip. To maximize the crosstalk performance on the board, add grounded filled vias in between the adjacent channels as shown in Figure 16.

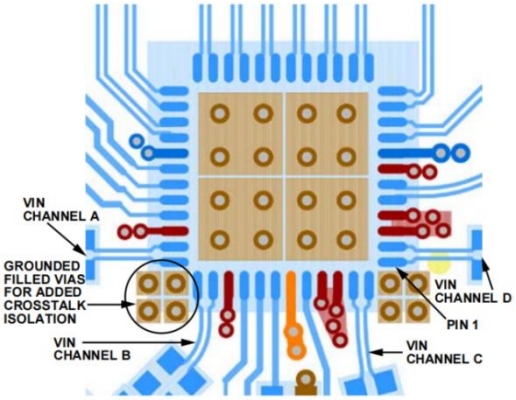
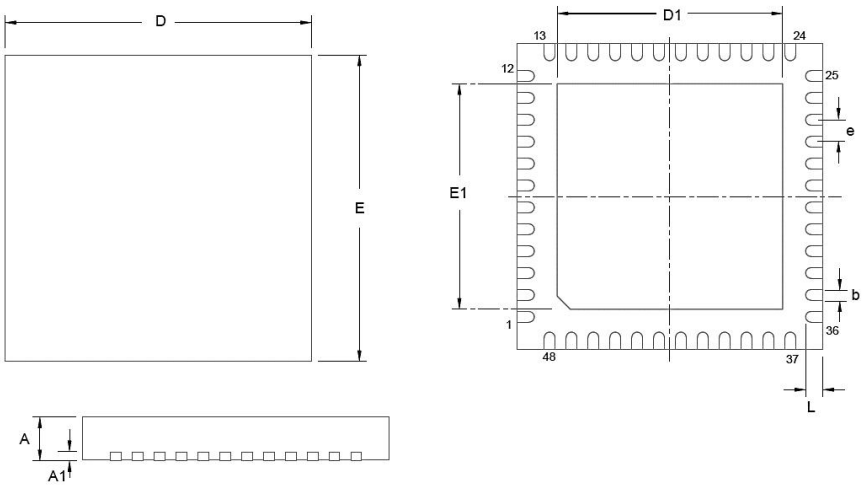


Figure 16 Layout Techniques To Maximize Crosstalk Performance

9 PACKAGE TYPE (QFN48)



Size symbol	Unit: mm		
	Minimum	Nominal	Maximum
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.24	0.30
D	6.80	7.00	7.20
D1	5.40	5.60	5.80
E	6.80	7.00	7.20
E1	5.40	5.60	5.80
e	0.50BSC		

Size symbol	Unit: mm		
	Minimum	Nominal	Maximum
L	0.35	0.40	0.45

10 ORDERING INFORMATION

LK ① **AD** ② **9653** ③ **QF** ④

① Product Series Code

② Category Identifier

③ Product Code

④ Encapsulation Type

Table 5 Ordering Information

model	Packaging	Quality grade	Operating temperature
LK AD9653QF	QFN , plastic package	Industrial grade	-40 ℃ ～+ 85 ℃

11 VERSION INFORMATION

Version number	date	Version Notes	Change Notes
REV 1.00	2025-06-25	Updated version	—
REV 1.01	2025-11-27	Updated version	Parameter updates