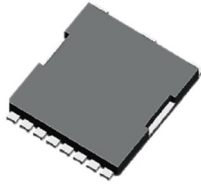


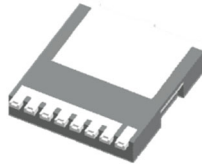
### Product Summary

$V_{DS}$	$R_{DS(ON\_MAX)}$	$I_{D\_MAX}$
100 V	1.3 m $\Omega$ @ $V_{GS} = 10V$	393 A

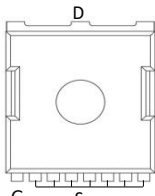
### TOLL



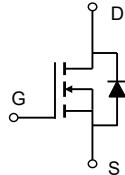
Top View



Bottom View



PIN Configuration  
(Top View)



Schematic Diagram

### Features

- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% UIS and  $R_g$  tested



### Applications

- DC/DC in Telecoms and Industrial
- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit

### Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

### Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
MX10T01AHTL	TOLL	MX10T01AHTL	13" Tape&Reel	2,000

### Maximum Ratings (@ $T_c = 25^\circ\text{C}$ , unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	$V_{DS}$	100	V
Gate - Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $V_{GS} = 10V$ ) <sup>(1)</sup>	$I_D$	$T_c = 25^\circ\text{C}$	393
		$T_c = 100^\circ\text{C}$	278
Pulsed Drain Current <sup>(2)</sup>	$I_{DM}$	1341	A
Single Pulse Avalanche Energy <sup>(3)</sup>	$E_{AS}$	2016	mJ
Single Pulse Avalanche Current ( $L = 0.3\text{mH}$ )	$I_{AS}$	74	A
Power Dissipation	$P_D$	$T_c = 25^\circ\text{C}$	429
		$T_c = 100^\circ\text{C}$	214
Junction & Storage Temperature Range	$T_J, T_{STG}$	-55 ~ +175	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient <sup>(4)</sup>	$R_{\theta JA}$	23	29	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case <sup>(5)</sup>	$R_{\theta JC}$	0.27	0.35	$^\circ\text{C/W}$

**Electrical Characteristics** (@  $T_J = 25^\circ\text{C}$ , unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b> <sup>(6)</sup>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$	-	-	1.0	$\mu A$
			-	-	100	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(6)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	1.1	1.3	$m\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 5.0V, I_D = 20A$	-	80	-	S
Diodes Forward Voltage	$V_{SD}$	$I_S = 2.0A, V_{GS} = 0V$	-	0.7	1.2	V
<b>Dynamic Characteristics</b> <sup>(7)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	-	9660	-	pF
Output Capacitance	$C_{oss}$		-	3476	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	48	-	pF
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$	-	2.1	-	$\Omega$
<b>Switching Characteristics</b> <sup>(7)</sup>						
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DS} = 50V$ $I_D = 20A, R_{GEN} = 3.0\Omega$	-	25	-	ns
Rise Time	$t_r$		-	42	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	87	-	ns
Fall Time	$t_f$		-	63	-	ns
<b>Gate Charge Characteristics</b> <sup>(7)</sup>						
Total Gate Charge ( $V_{GS} = 10V$ )	$Q_g$	$V_{DS} = 50V, I_D = 20A$ $V_{GS} = 10V$	-	140	-	nC
Total Gate Charge ( $V_{GS} = 6.0V$ )	$Q_g$		-	88	-	nC
Gate-Source Charge	$Q_{gs}$		-	38	-	nC
Gate-Drain Charge	$Q_{gd}$		-	27	-	nC
Gate Plateau Voltage	$V_{plateau}$		-	4.2	-	V
<b>Drain-Source Diode Characteristics</b> <sup>(7)</sup>						
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20A, di/dt = 100A/\mu s,$ $T_J = 25^\circ\text{C}$	-	105	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	394	-	nC
Diode Forward Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	393	A

**Notes:**

1. This current is chip limited, which is calculated based on  $R_{thjc}$ .
2. This current is calculated on single pulse with  $10\mu s$  Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test,  $E_{AS}$  condition:  $T_J = 25^\circ\text{C}, V_{DD} = 50V, V_{GS} = 10V, L = 1.0mH$ .
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

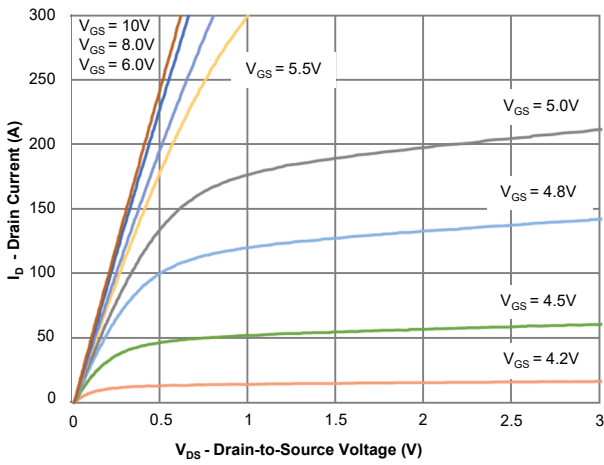


Figure 1: Output Characteristics

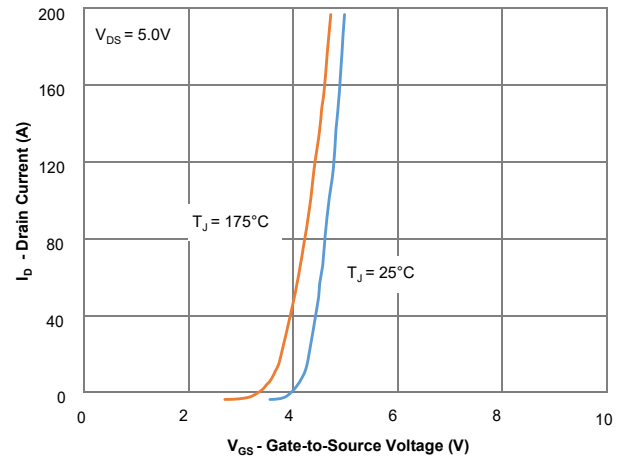


Figure 2: Transfer Characteristics

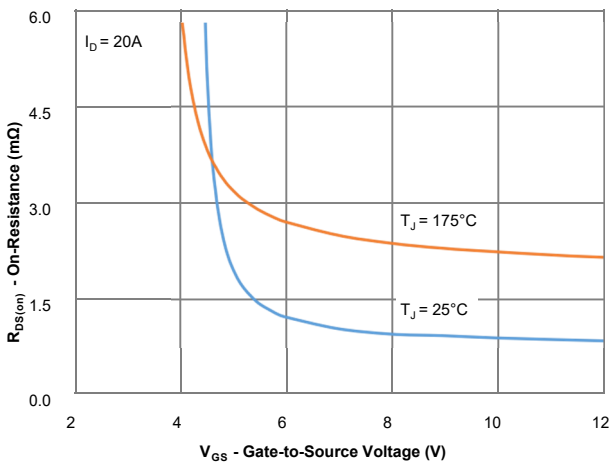


Figure 3: On-Resistance vs. Gate-Source Voltage

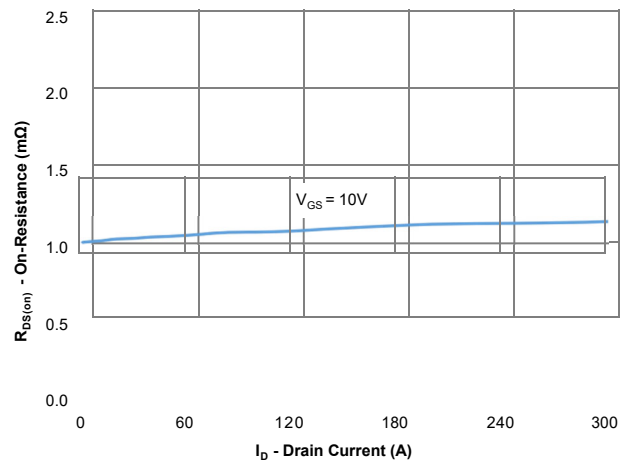


Figure 4: On-Resistance vs. Drain Current

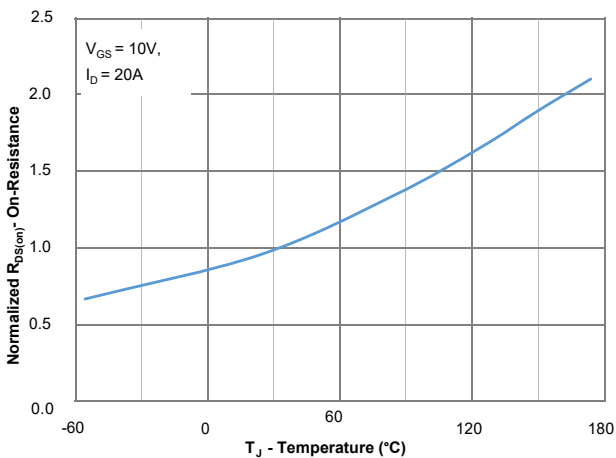


Figure 5: On-Resistance vs. Junction Temperature

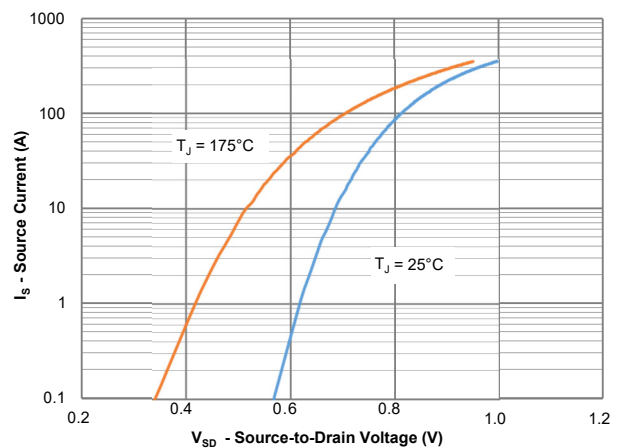
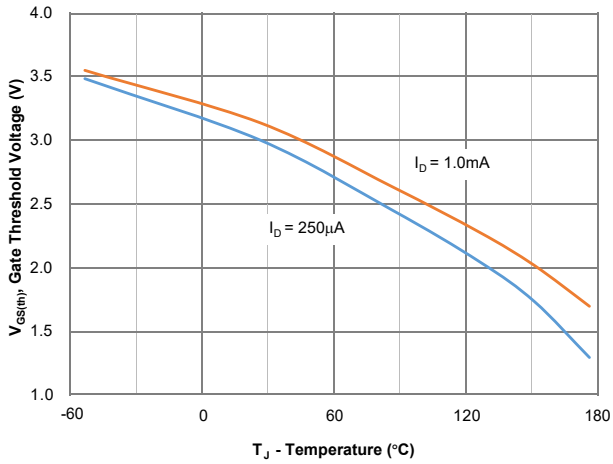
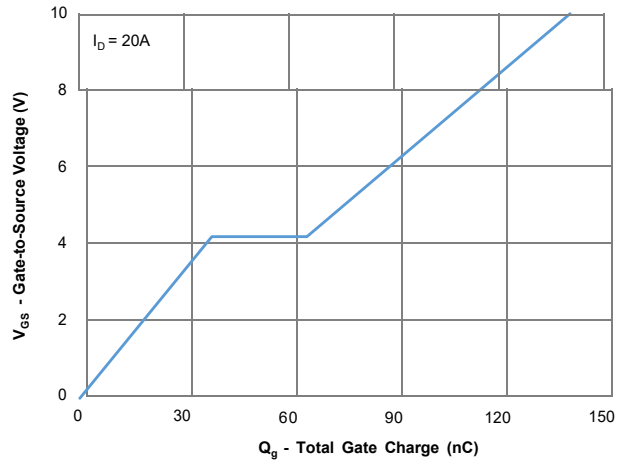


Figure 6: Source-Drain Diode Forward Voltage

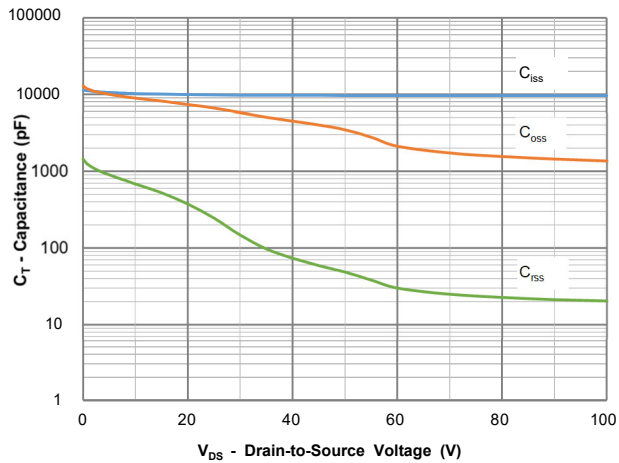
**Typical Electrical and Thermal Characteristics**



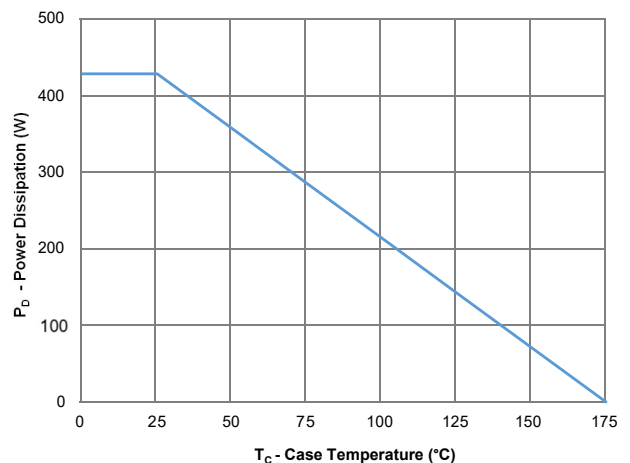
**Figure 7: Gate Threshold Variation vs. Junction Temperature**



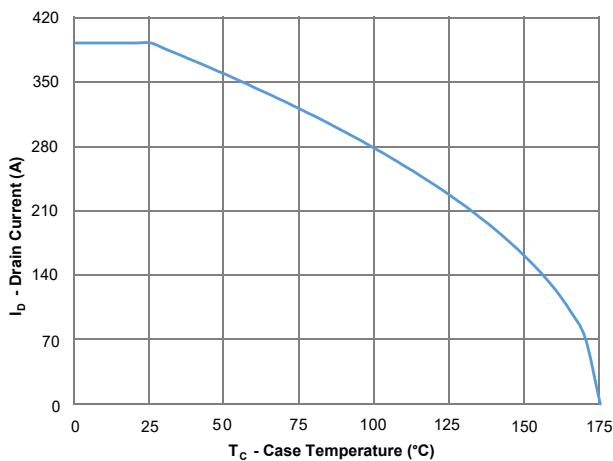
**Figure 8: Gate Charge Characteristics**



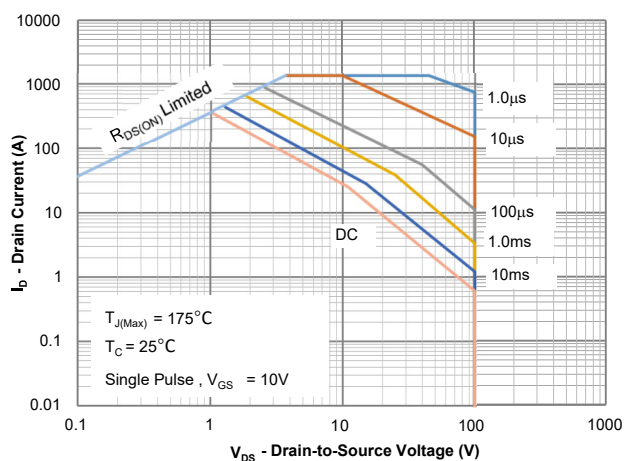
**Figure 9: Capacitance Characteristics**



**Figure 10: Power Derating**



**Figure 11: Current Derating**



**Figure 12: Safe Operating Area**

Typical Electrical and Thermal Characteristics

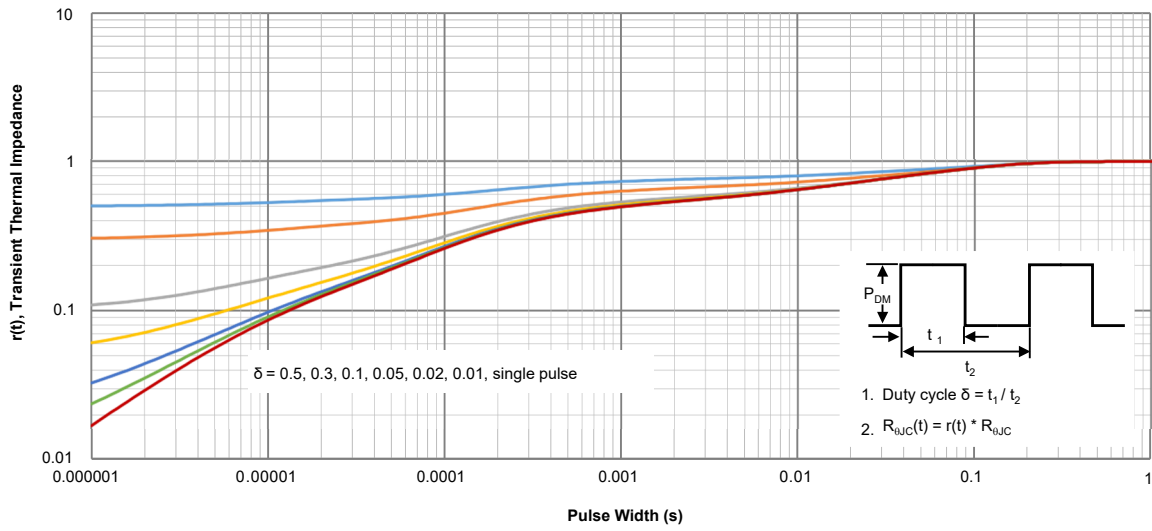
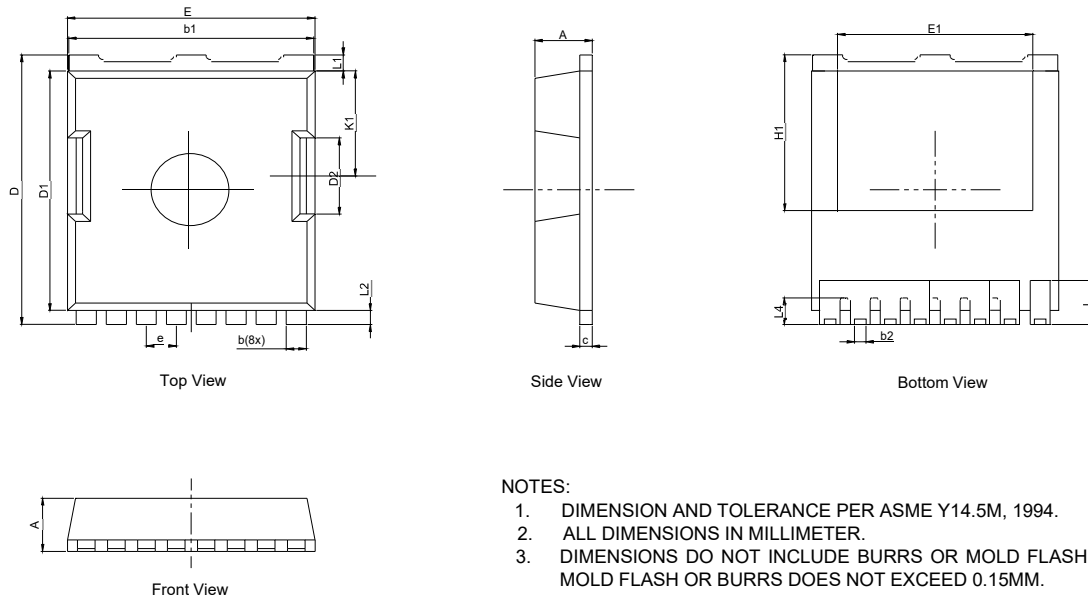


Figure 13: Normalized Maximum Transient Thermal Impedance

**TOLL Package Outline**

**Package Outlines**



**NOTES:**

1. DIMENSION AND TOLERANCE PER ASME Y14.5M, 1994.
2. ALL DIMENSIONS IN MILLIMETER.
3. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.15MM.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.65	9.80	9.95
c	0.40	0.50	0.60
D	11.48	11.68	11.95
D1	10.28	--	10.70
D2		3.30	
E	9.70	9.90	10.10
E1		8.10	
e		1.20 (BSC)	
H1	6.70	7.00	7.30
K1		4.55	
L	1.35	--	2.10
L1		0.70	
L2		0.60	
L4	0.95	1.20	1.35

**Recommended Soldering Footprint**

