

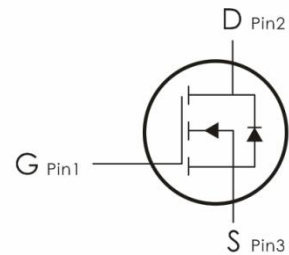
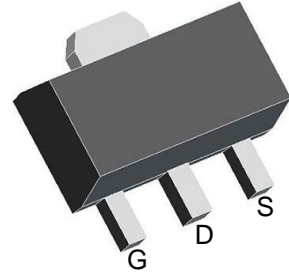
Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=40V, I_D=16A, R_{DS(ON)} < 16m\ \Omega @ V_{GS}=10V$ (Typ: $12m\ \Omega$)
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(ON)}$.
- 5) Excellent package for good heat dissipation.
- 6) MSL3



Package Marking and Ordering Information:

Part NO.	Marking	Package	Packing
WD016NG	D016N	SOT-89	1000 pcs/Reel

Absolute Maximum Ratings: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	16	A
I_{DM}	Pulsed Drain Current ¹	40	
E_{AS}	Single pulse avalanche energy ²	36	mJ
P_D	Power Dissipation	2.4	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55--+150	$^\circ\text{C}$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ³	52	$^\circ\text{C}/\text{W}$

Electrical Characteristics: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu\text{A}$	40	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS}=0V, V_{DS}=40V$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0A$	---	---	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\ \mu\text{A}$	1	1.3	1.8	V
$R_{DS(on)}$	Drain-Source On Resistance ³	$V_{GS}=10V, I_D=10A$	---	12	16	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=5A$	---	14	18	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20V, V_{GS}=0V, f=1\text{MHz}$	---	1113	---	pF
C_{oss}	Output Capacitance		---	109	--	
C_{rss}	Reverse Transfer Capacitance		---	88	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=20V, I_D=10A,$ $R_{ENG}=3\ \Omega, V_{GS}=10V$	---	7	---	ns
t_r	Rise Time		---	11.5	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	27	---	ns
t_f	Fall Time		---	5	---	ns
Q_g	Total Gate Charge		$V_{GS}=10V, V_{DS}=20V,$ $I_D=10A$	---	27	---
Q_{gs}	Gate-Source Charge	---		6.3	---	nC
Q_{gd}	Gate-Drain "Miller" Charge	---		5	---	nC
Drain-Source Diode Characteristics						
I_S	Continuous Drain Current	$V_D=V_G=0V$	---	---	16	A
I_{SM}	Pulsed Drain Current		---	---	40	A
T_{rr}	Reverse Recovery Time	$I_F=15A, T_J=25^\circ\text{C}$	---	10	---	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu\text{s}$	---	6	---	nC
V_{SD}	Diode Forward Voltage ³	$V_{GS}=0V, I_{SD}=10A$	---	---	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition : $T_J=25^{\circ}\text{C}$, $V_{DD}=20\text{V}$, $V_G=10\text{V}$, $L=0.5\text{mH}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Test Circuit

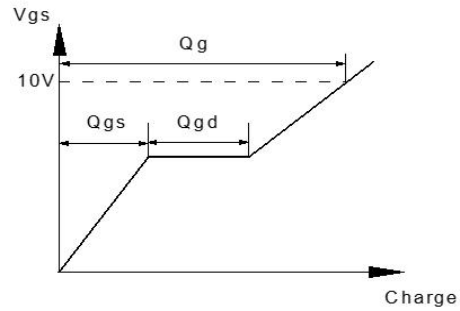
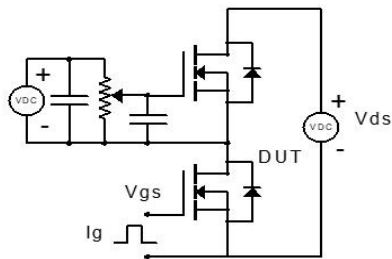


Figure 1: Gate Charge Test Circuit & Waveform

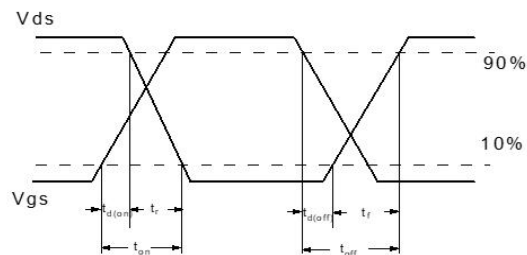
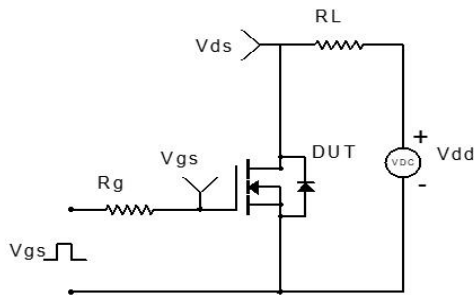


Figure 2: Resistive Switching Test Circuit & Waveform

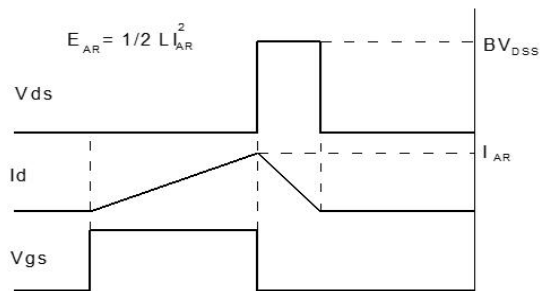
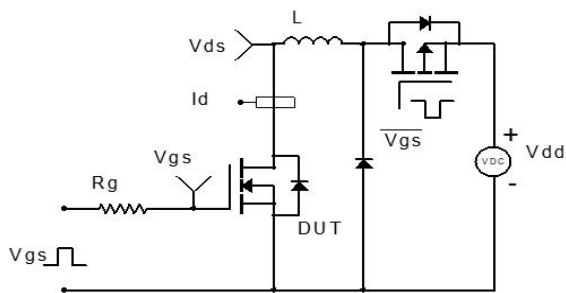


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

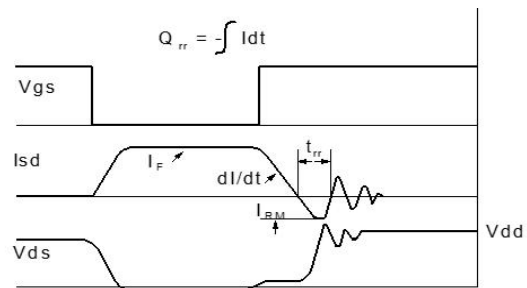
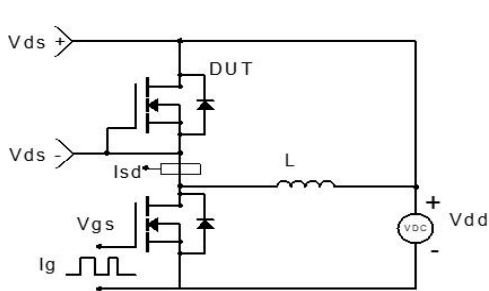
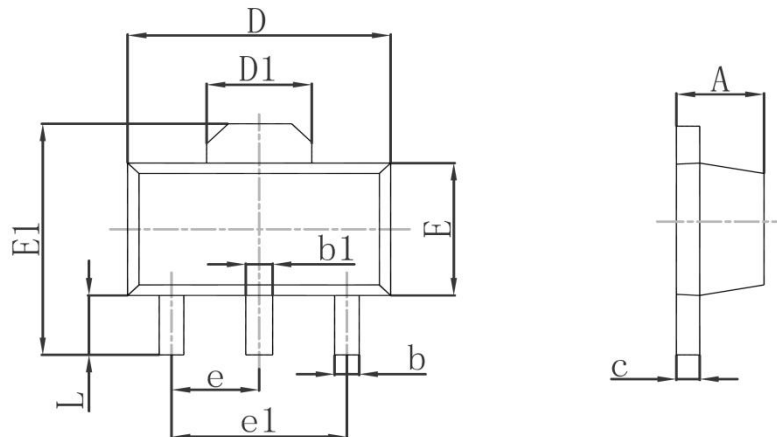


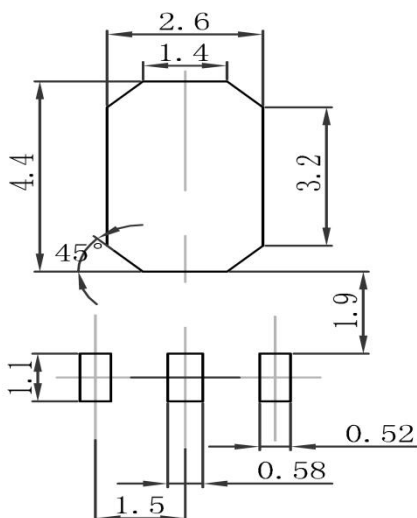
Figure 4: Diode Recovery Test Circuit & Waveform

SOT-89 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550REF		0.061REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	3.000TYP		0.118TYP	
L	0.900	1.200	0.035	0.047

SOT-89 Suggested Pad Layout



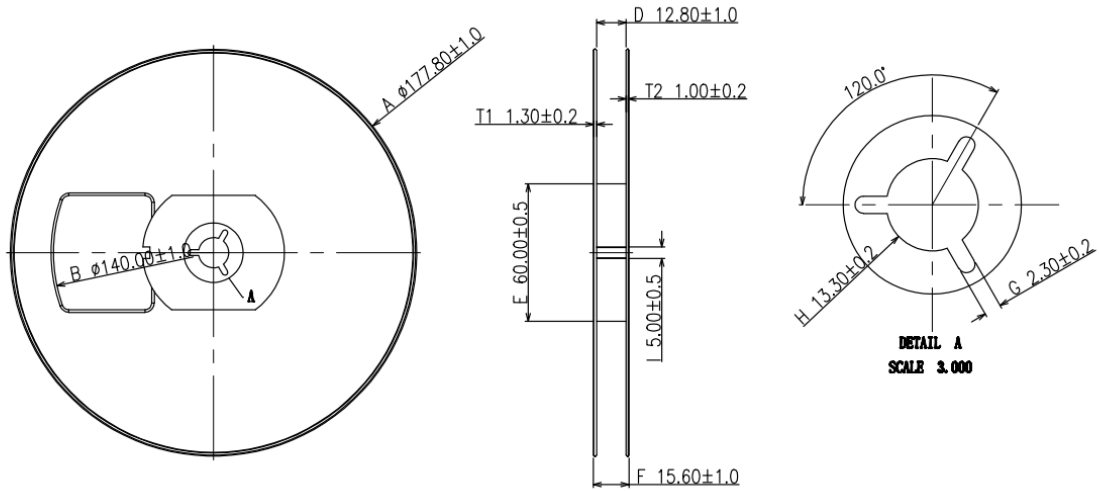
Note:

1. Controlling dimension: in millimeters
2. General tolerance: $\pm 0.05\text{mm}$
3. The pad layout is for reference purposes only

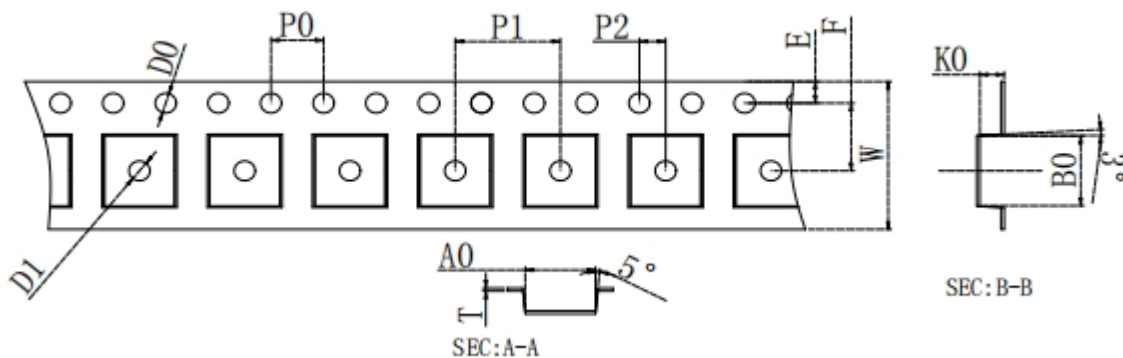
UNIT: mm

Tape & Reel Information

Dimensions in mm



W	12.00±0.10	T	0.22±0.02	D1	1.60±0.10	MM
E	1.75±0.10	F	5.50±0.10	DO	1.60±0.10	PC+PS
PO	4.00±0.10	P1	8.00±0.10	P2	2.00±0.10	SOT89
A0	4.90±0.10	BO	4.50±0.10	KO	1.75±0.10	



Pulling direction →

Marking Information:

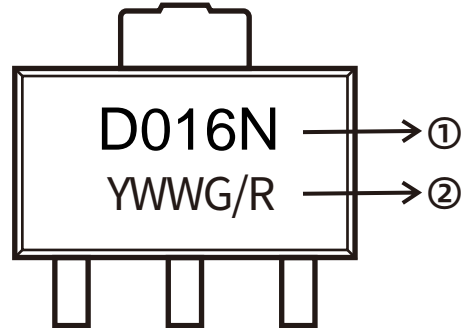
①. Part NO.

②. Date Code(YWWG / R)

Y : Year Code , last digit of the year

WW : Week Code(01-53)

G/R : G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2024-10-20	Release of final version

Attention :

- Information furnished in this document is believed to be accurate and reliable. However, Shenzhen Doingter Semiconductor Co.,Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.
- Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Shenzhen Doingter complies with the agreement. Products and information provided in this document have no infringement of patents.
- Shenzhen Doingter assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.



Is a registered trademark of Shenzhen Doingter Semiconductor Co., Ltd. Copyright © 2013 Shenzhen Doingter Semiconductor Co.,Ltd. Printed All rights reserved.