SA23002A

High-Efficiency, 5.5V, 2A, Single Synchronous Buck Converter

General Description

The SA23002A high-efficiency synchronous Buck converter can deliver 2A output current over an input voltage range from 2.8V to 5.5V. It uses built-in power MOSFETs to supply a resistor-configurable output voltage between 0.6V and V_{IN}. The fixed 2.35MHz switching frequency allows for small external inductor and capacitor values.

The SA23002A is available in a DFN2mm×2mm-8 package.

Features

- 2.8V to 5.5V Input Voltage Range
- Up to 2A Output Current
- External Adjustable Voltage with ±1.5% Reference Accuracy
- 1μA Shutdown Current (Typical)
- Fixed 2.35MHz Switching Frequency Minimizes Required External Components
- Selectable PWM and PFM Operating Modes
- 100% Duty-Cycle Capable
- Cycle-by-Cycle Current-Limit Protection
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown
- Package: DFN2mm×2mm-8
- AEC-Q100 Qualified for Automotive Applications

Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Display

Typical Application

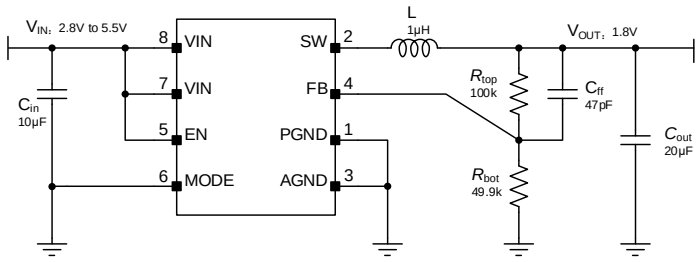


Figure 1. Schematic Diagram

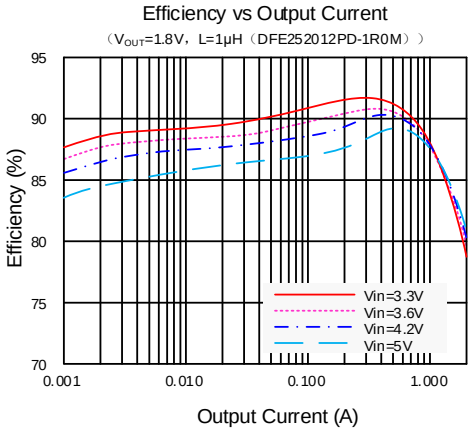


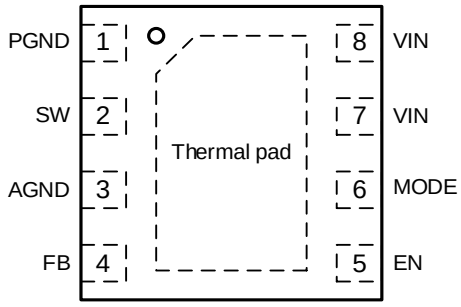
Figure 2. Efficiency vs Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SA23002ADFD	DFN2×2-8 RoHS Compliant and Halogen Free	**FFW***xyz*

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	PGND	Power ground.
2	SW	Switching node.
3	AGND	Analog ground.
4	FB	Output voltage feedback pin. The output voltage reference is 0.6V.
5	EN	Device enable pin, logic-high enable. There is no pulldown resistor inside. Do not leave floating. The external resistor should be less than 500kΩ.
6	MODE	PFM/FCCM Mode selection. When the MODE pin is high, the device is forced to operate in FCCM. When the pin is low, the device enters PFM mode automatically during light load conditions. There is no pulldown resistor inside. Do not leave floating.
7, 8	V_{IN}	V_{IN} power supply.

Block Diagram

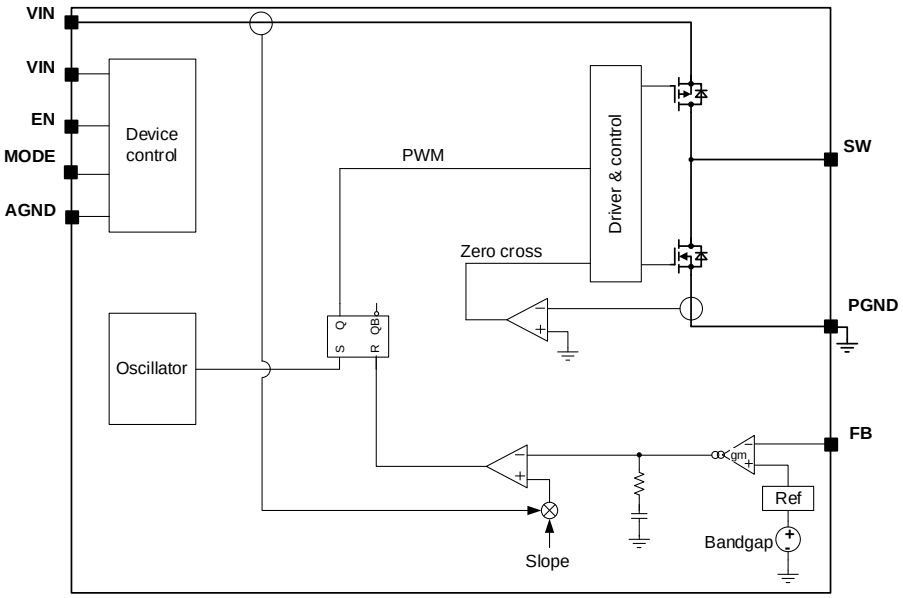


Figure 3. Functional Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
V_{IN}	-0.3	6.5	V
FB, EN, MODE	-0.3	V_{IN} + 0.3	
Dynamic SW to GND Voltage in 20ns Duration	-3	V_{IN} + 1.5	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)		±2000	V
CDM (Charge Device Model) All Pins		±500	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	56.5	°C/W
θ_{JC_BOT} Junction-to-Case Thermal Resistance	14.5	
Ψ_{JT}	3.5	
P_D Power Dissipation T_A = 25°C	2.2	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
V_{IN}	2.8	5.5	V
Ambient Temperature	-40	125	°C

Electrical Characteristics

(2.8V ≤ V_{IN} ≤ 5.5V, -40°C ≤ T_J ≤ 125°C. typical values at V_{IN} = 5V and T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN}	UVLO Rising Threshold	V_{UVLO_R}		2.6	2.7	2.8	V
	UVLO Falling Threshold	V_{UVLO_F}		2.45	2.55	2.65	V
	Shut Down Current A	I_{SDA}	V_{EN} = 0V, T_J = 25°C		1	2	μA
	Shut Down Current B	I_{SDB}	V_{EN} = 0V, T_J = 125°C		6	12	μA
	Quiescent Current	I_Q	V_{MODE}=logic low, V_{EN}=logic high, no load		22	35	μA
EN	EN Logic 1 Threshold	V_{EN_H}		1.2			V
	EN Logic 0 Threshold	V_{EN_L}				0.4	V
Power Stage	Switching Frequency	f_{sw}		2	2.35	2.7	MHz
	HS FET $R_{DS(ON)}$	$R_{DS(ON)\_HS}$	V_{IN} = 5V		120		mΩ
	LS FET $R_{DS(ON)}$	$R_{DS(ON)\_LS}$	V_{IN} = 5V		85		mΩ
	Discharge Resistor	$R_{DISCHARGE}$			200		Ω
Feedback and Soft-Start	Output Feedback Reference	V_{REF}		591	600	609	mV
	Soft-Start Time	T_{SS}	T_J = 25°C	0.1	0.2	0.5	ms
Mode	Input Bias Current	I_{IN}			0.01	1	μA
	Logic 1 Threshold	V_{MODE_H}		1.2			V
	Logic 0 Threshold	V_{MODE_L}				0.4	V
Thermal Shutdown	Thermal Shutdown Threshold	T_{SD}		150	165	180	°C
	Thermal Shutdown Hysteresis	T_{SDHYS}		10	15	20	°C
Current Limit	Peak Current Limit	I_{LIMIT_P}		2.8	3.5	4.2	A
	Valley Foldback Current Limit	I_{LIMIT_V}		2	2.8	3.5	A
	Negative Valley Current Limit	I_{LIMIT_N}		0.7	1.2	1.7	A
Short-Circuit Protection	Short-Circuit Threshold	V_{SCP}	V_{FB} as percent of V_{REF}	20	30	40	%V_{REF}
	Short-Circuit Response Time	t_{SCP}	From V_{FB} < V_{SCP} to stop switching. No delay on the other side, V_{IN} = 5V.	5	10	20	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A=25°C on an 6cm × 6cm two-layer Silergy Evaluation Board with 1oz copper.

Note 3: The device is not guaranteed to electrical parameter outside its recommended operating conditions.

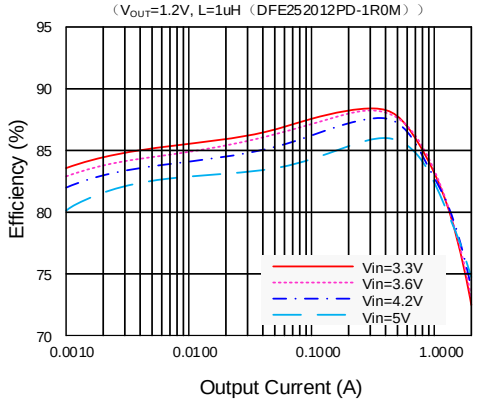
Note 4: Guaranteed by design. Not tested in production.

Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, V_{OUT} =1.8 V, L = 1μH, C_{OUT} = 20μF, unless otherwise noted)

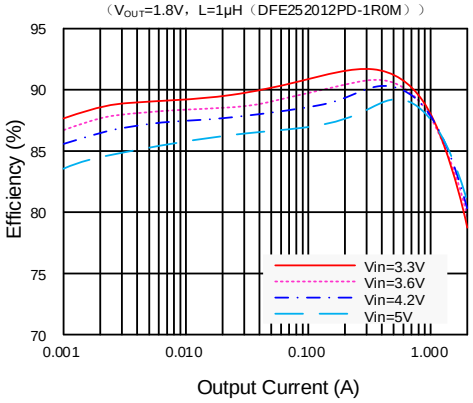
Efficiency vs Output Current

(V_{OUT}=1.2V, L=1uH（DFE252012PD-1R0M））



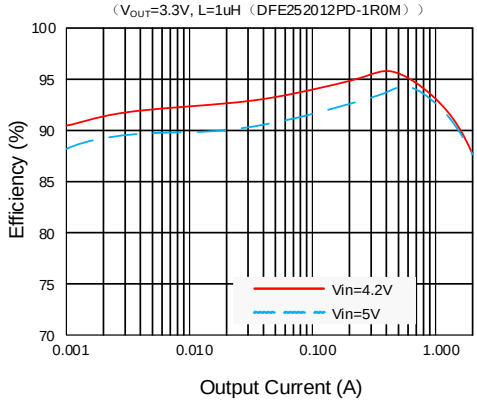
Efficiency vs Output Current

(V_{OUT}=1.8V，L=1μH（DFE252012PD-1R0M））



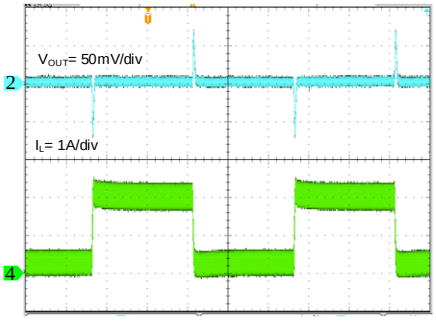
Efficiency vs Output Current

(V_{OUT}=3.3V, L=1uH（DFE252012PD-1R0M））



Load Transient Response

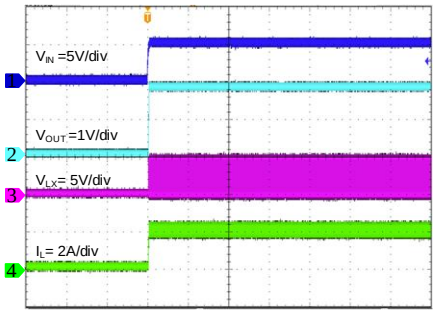
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.2~2A)



Time (400μs/div)

Startup from VIN

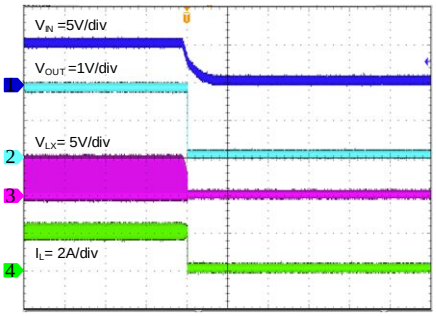
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (20ms/div)

Shutdown from VIN

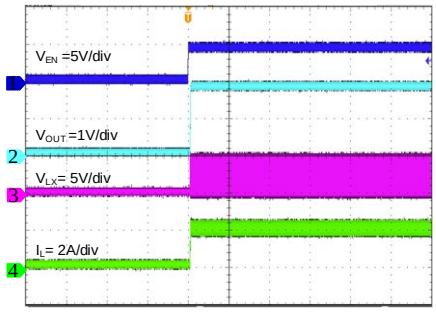
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (20ms/div)

Startup from VEN

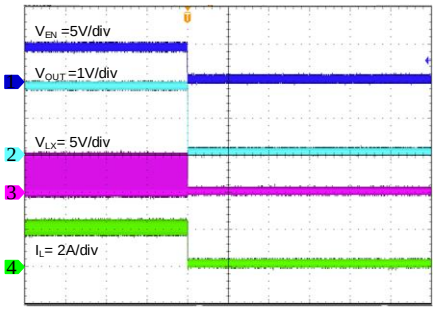
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (10ms/div)

Shutdown from VEN

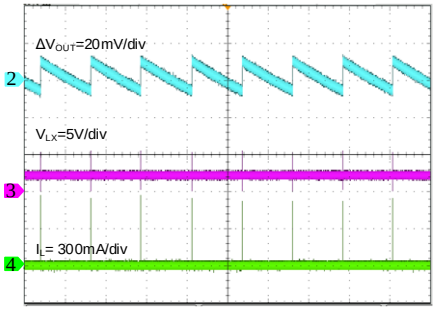
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (10ms/div)

Output Ripple

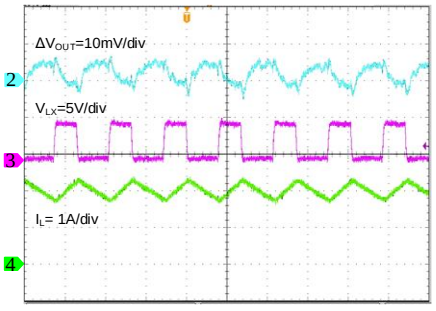
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (40ms/div)

Output Ripple

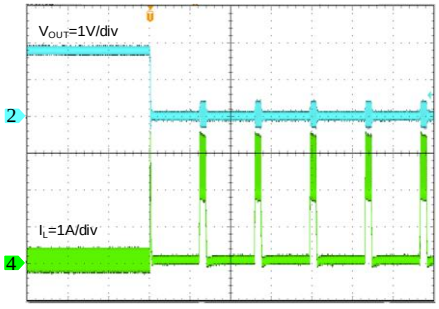
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (400ns/div)

Output Short Circuit

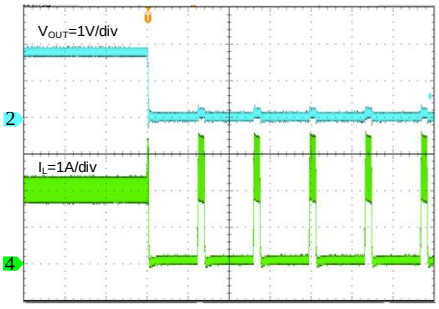
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



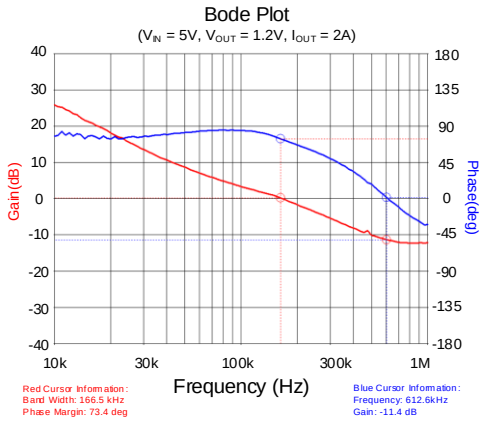
Time (2ms/div)

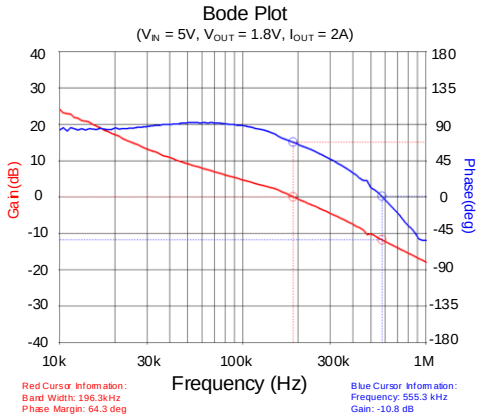
Output Short Circuit

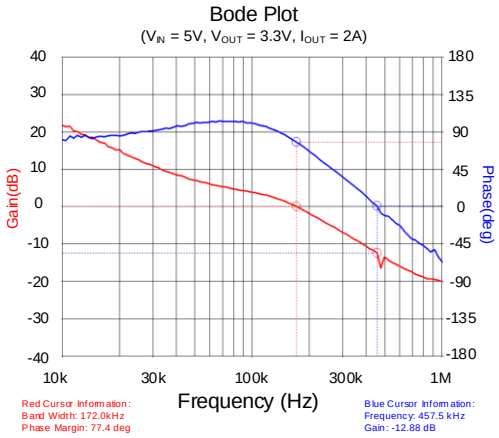
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=2A)



Time (2ms/div)







Applications Information

The SA23002A high-efficiency synchronous Buck converter can deliver 2A output current over an input voltage range from 2.8V to 5.5V. It uses built-in power MOSFETs to supply a resistor-configurable output voltage between 0.6V and V_{IN}. The fixed 2.35MHz switching frequency allows for small external inductor and capacitor values.

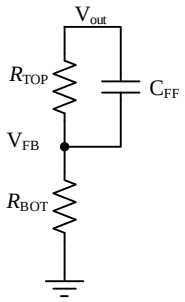
The selection process for the feedback resistors (R_{TOP} and R_{BOT}), output inductor L, input capacitor C_{IN}, and output capacitor C_{OUT} is described in the following sections.

Feedback Resistor-Divider R_{TOP} and R_{BOT}

Choose R_{TOP} and R_{BOT} to program the proper output voltage. Choose large resistance values between 10kΩ and 105kΩ for both R_{TOP} and R_{BOT} to minimize power consumption under light loads (refer to the Typical Application section for recommended feedback Resistor values).

The output voltage can be configured using the following equation:

$$V_{OUT} = (1 + \frac{R_{TOP}}{R_{BOT}}) \times V_{FB}$$



where V_{FB} has a value of 0.6V (typ).

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_s \times I_{OUT,MAX} \times 0.4}$$

where f_S is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SA23002A has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN\_MAX})}{2 f_S \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. Choose an inductor with smaller DCR to achieve a good overall efficiency.

Input Capacitor C_{IN}

The ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT\_MAX} \times \sqrt{D \times (1 - D)}$$

The capacitance of the input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times F_s \times \eta \times V_{IN}^2}$$

where ΔV_{IN} is maximum allowed input voltage ripple.

For reliable operation, place a typical X7R or better grade ceramic capacitor close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and the V_{IN}/GND pins. A 10μF low-ESR ceramic capacitor is recommended for most applications. There is no need to place a 100nF ceramic capacitor in parallel between SA23002A and the 10μF capacitor.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. It is recommended to use an X7R or better grade ceramic capacitor (refer to the Typical Application section for recommended capacitance values).

Peak Current Mode Control

The Buck regulator provides a supply voltage lower than input voltage. The PWM controller measures the output voltage via a resistor divider connected between Pin FB and ground, and determines the appropriate pulse width duty cycle (on time).

The SA23002A incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

ON-OFF Sequence

When the device is enabled and the input voltage is above the UVLO threshold, the internal reference is activated and the analog circuits are settled. Afterwards, the soft-start is activated and the output voltage is ramped up.

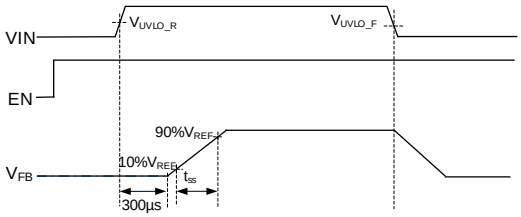


Figure 4. VIN ON/OFF Sequence

The device is enabled by setting the EN pin high. When the input voltage is above the UVLO threshold and the device is enabled, the output voltage ramps up from 10% to 90% of nominal value with t_{SS} of 200μs (typical).

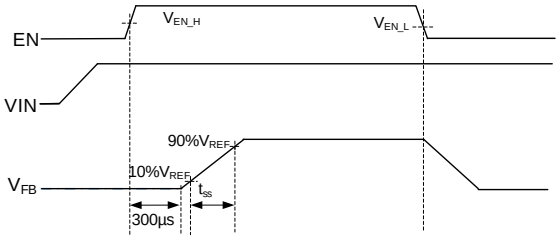


Figure 5. EN ON/OFF Sequence

Adaptive Frequency Foldback at Minimum T_{OFF} Operation (Dropout)

The SA23002A provides adaptive frequency reduction during large-duty-cycle operation when minimum T_{OFF} is reached. Unlike conventional peak-current control, this approach ensures the stability of the circuit during dropout operation. When V_{IN} drops below the configured V_{OUT} voltage, the SA23002A will enter dropout mode, wherein its high-side FET will always be ON. Normal operation resumes when V_{IN} exceeds the target V_{OUT} level.

Light-Load Operation

The SA23002A supports automatic PWM/PFM operation when the external MODE pin is set low. The converter operates in fixed-frequency PWM mode at medium to heavy loads, and in PFM mode during light loads, maintaining high efficiency over the entire load-current range.

Protection Features

The SA23002A provides integrated output short-circuit protection, output overcurrent protection, and thermal shutdown protection.

Table 1. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 165°C Falling: 150°C	–	Shutdown when temperature >165°C. Restart when temperature <150°C.
Cycle-by-Cycle Current Limit	3.5A	–	Peak limit = valley limit. Valley foldback to 80% after 3 cycles.
Output SCP	V_{FB} <30% V_{REF}	10μs	Hiccup time = 2.5ms.

Current Limit

The SA23002A features cycle-by-cycle current-limit protections. When the current-sense amplifier detects a voltage that exceeds the peak current limit, the HS FET is turned off for the remainder of the cycle. See Figure 6.

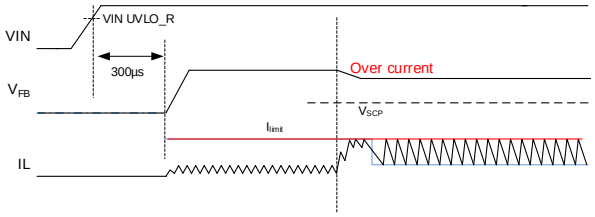


Figure 6. Cycle-by-Cycle Current Limit

Short-Circuit Protection

The SA23002A will attempt to protect the power MOSFET from damage in the event of a short circuit at the output. After the initial short-circuit blanking time T_{SCP}, when the output voltage falls below the short-circuit threshold, the device will be turned off for the hiccup time and then go through the soft-start time T_{SS}. See Figure 7.

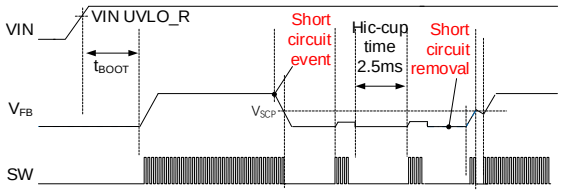


Figure 7. Short-Circuit Protection

Overtemperature Protection

The SA23002A enters thermal shutdown when the junction temperature exceeds 165°C (typical). In this mode, the high-side switch and low-side switch are turned off. When the junction temperature falls below 150°C (typical), the Buck will automatically be re-enabled. See Figure 8.

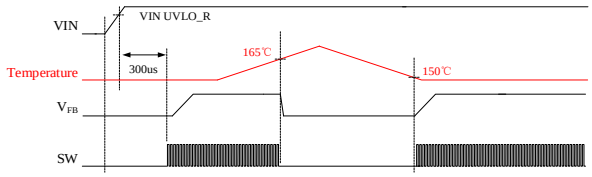
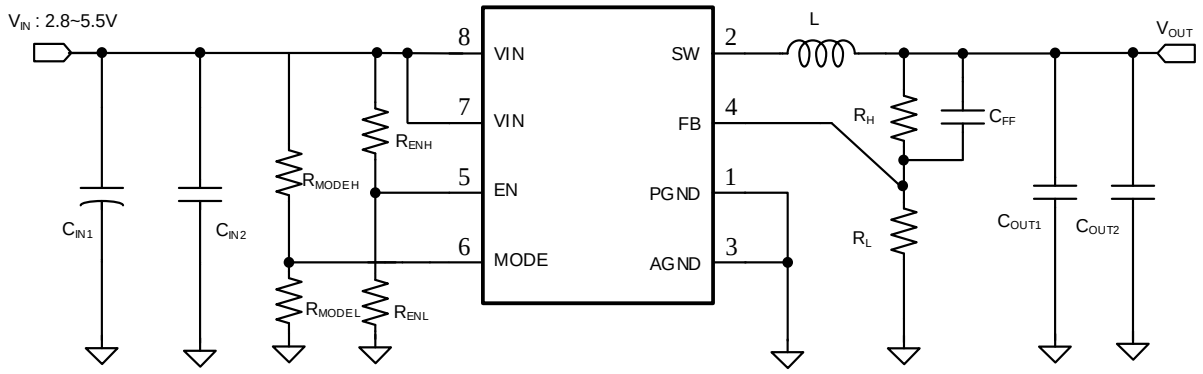


Figure 8. Overtemperature Protection

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V Electrolytic Capacitor		
C_{IN2}, C_{OUT1}, C_{OUT2}	10μF/6.3V/X7T, 0603	GCM188D70J106ME36D	muRata
L	1μH/inductor,3.2A	DFE252012PD-1R0M	muRata
C_{FF}	47pF/50V/C0G, 0603		
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{MODEH}	10kΩ, 1%, 0603		
R_{MODEL}	1MΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

Table 2. Setting the Output Voltage (C_{OUT} ≥ 20μF, V_{OUT} ≥ 0.6V)

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
0.6	0	NC	NC	1.0μH/DFE252012PD-1R0M	10μF*3/6.3V, 0603, X7T
0.8	10	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
0.9	15	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.0	20	30	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.1	20	24	68	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.2	51	51	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.5	30	20	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
1.8	100	49.9	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
2.5	105	33	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T
3.3	100	22.1	47	1.0μH/DFE252012PD-1R0M	10μF*2/6.3V, 0603, X7T

Table 3. Setting the Output Voltage (C_{OUT} = 10μF, V_{OUT} ≥ 1.2V)

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	10	10	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
1.5	30	20	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
1.8	30	15	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
2.5	47.5	15	22	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T
3.3	100	22.1	10	1.0μH/DFE252012PD-1R0M	10μF/6.3V, 0603, X7T

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. Using a separate layer as a ground plane is highly recommended.
- To avoid EMI, minimize the PCB copper area associated with the SW pin.
- To avoid potential noise, ensure that the feedback components R_H and R_L, and the trace connecting to the FB pin, are **not** adjacent to the SW net on the PCB layout.

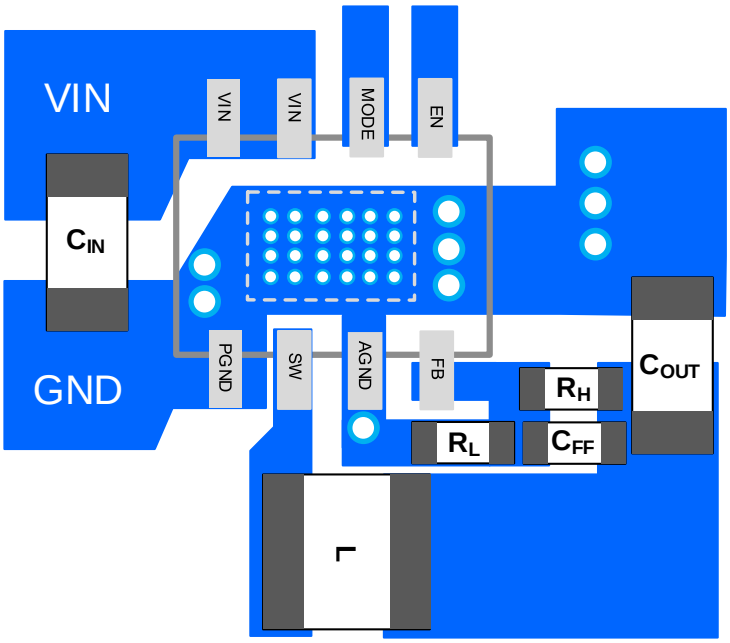
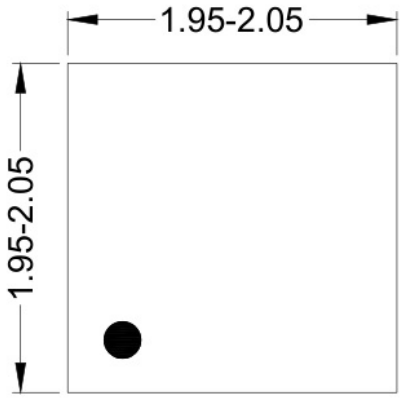
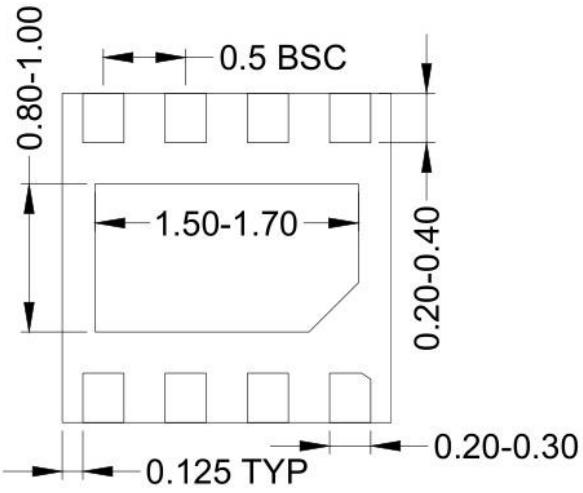


Figure 9. PCB Layout Suggestion

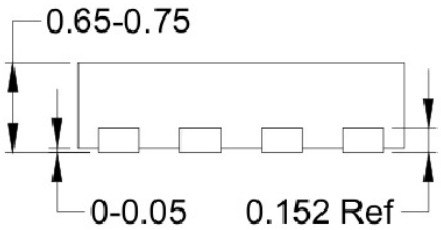
DFN2×2-8 Package Outline Drawing



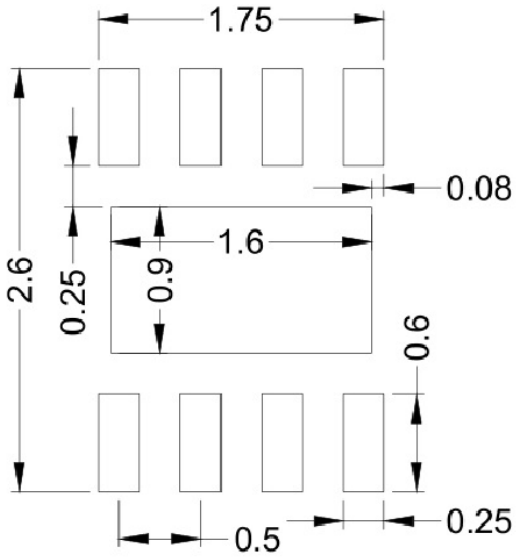
Top View



Bottom View



Side View

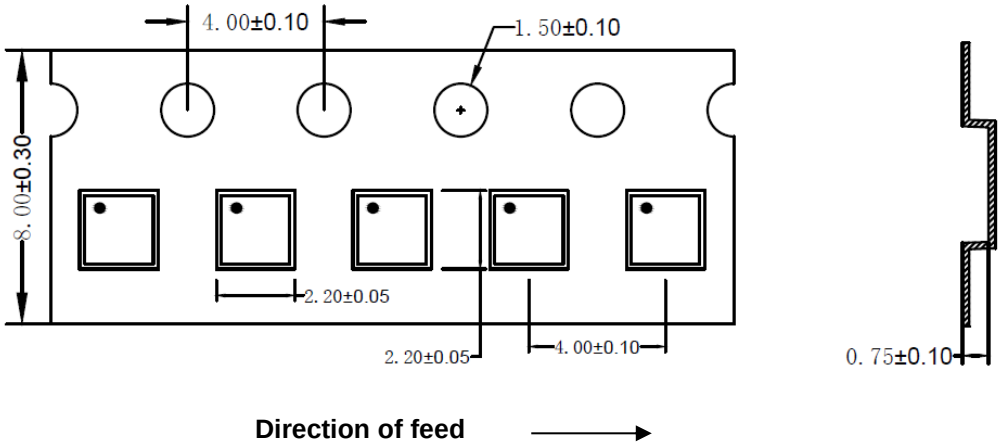


Recommended PCB layout (Reference only)

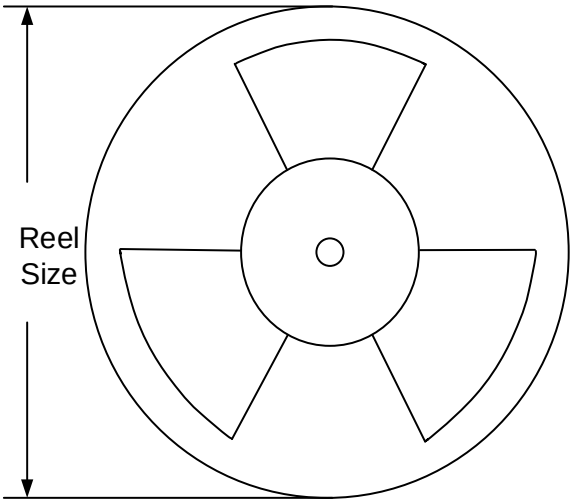
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7"	400	400	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jul.11, 2023	Revision 0.9	Initial Release
Oct. 09, 2023	Revision 0.9A	1. Add the application circuit diagram and recommended parameters. 2. Add Bode Plots. 3. Modify the descriptions of Absolute Maximum Ratings and Recommended 4. Modify the recommended input voltage range and ISD current description. 5. Modify the recommended voltage divider range. 6. Modify the short circuit waveform description. 7. Add description of ON-OFF sequence. 8. Add description of peak current mode. 9. Modify operation mode from PSM to PFM of Key Features in page 1. 10. Modify the description of thermal resistance test condition. 11. Modify the description of Current limit and Short Circuit Protection.
Feb.28, 2025	Revision 1.0	Initial production release.
Oct.09, 2025	Revision 1.0A	Language Improving.

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