

General Description

The 65R450 is power MOSFET using Cmos's advanced super junction technology that can realize very low on resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss.

Features

- Multi-layer Epitaxial Chip Technology
- Low On-Resistance
- 100% Avalanche Tested
- RoHS Compliant

Product Summary

BV _{DSS}	R _{DS(on)} max.	I _D
650V	0.45Ω	11A

Applications

- Charger
- Adaptor
- Power Supply

TO-252/TO-251 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25°C	Continuous Drain Current	11	A
I _D @T _C =100°C	Continuous Drain Current	7	A
I _{DM}	Pulsed Drain Current	44	A
EAS	Single Pulse Avalanche Energy (Note 1)	422	mJ
P _D @T _C =25°C	Total Power Dissipation	80	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Rating	Unit
R _{θJA}	Thermal Resistance Junction-ambient	68	°C/W
R _{θJC}	Thermal Resistance Junction-case	1.56	°C/W

Electrical Characteristics ($T_j=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=5.5A$	---	0.41	0.45	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	3	4	5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=650V, V_{GS}=0V, T_j=150^\circ\text{C}$	---	10	---	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=20V, I_D=5.5A$	---	7	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	3	---	Ω
Q_g	Total Gate Charge	$I_D=5.5A$	---	22	---	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	---	5.3	---	
Q_{gd}	Gate-Drain Charge	$V_{GS}=10V$	---	8.8	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=400V$ $V_{GS}=10V$ $I_D=5.5A$ $R_G=25\Omega$	---	20	---	ns
T_r	Rise Time		---	15	---	
$T_{d(off)}$	Turn-Off Delay Time		---	74	---	
T_f	Fall Time		---	43	---	
C_{iss}	Input Capacitance	$V_{DS}=100V, V_{GS}=0V, f=1\text{MHz}$	---	870	---	pF
C_{oss}	Output Capacitance		---	40	---	
C_{rss}	Reverse Transfer Capacitance		---	5	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	$V_{GS}=V_{DS}=0V$, Force Current	---	---	11	A
I_{SM}	Pulsed Source Current		---	---	44	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V, I_F=11A, T_j=25^\circ\text{C}$	---	0.86	1.5	V
t_{rr}	Reverse Recovery Time	$V_{DS}=100V, T_j=25^\circ\text{C}$ $I_{sd}=5.5A, di/dt=100A/\mu s$	---	212	---	ns
Q_{rr}	Reverse Recovery Charge		---	2.28	---	μC

Note :

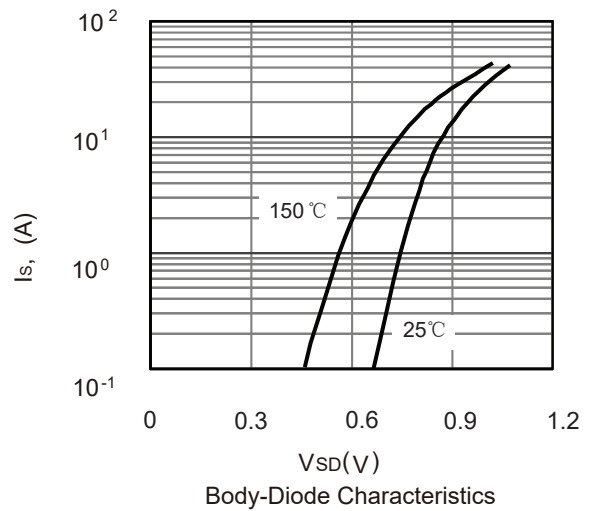
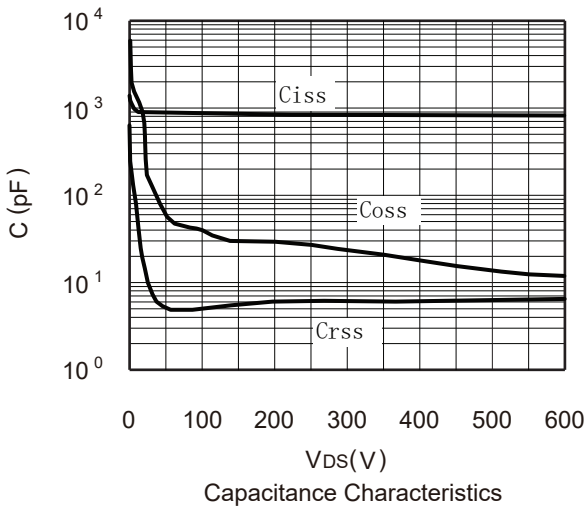
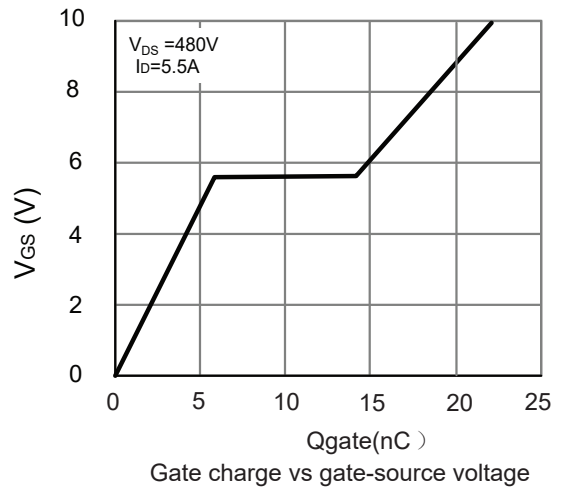
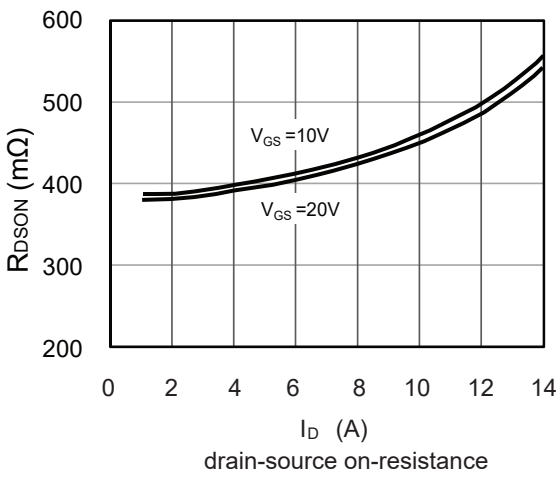
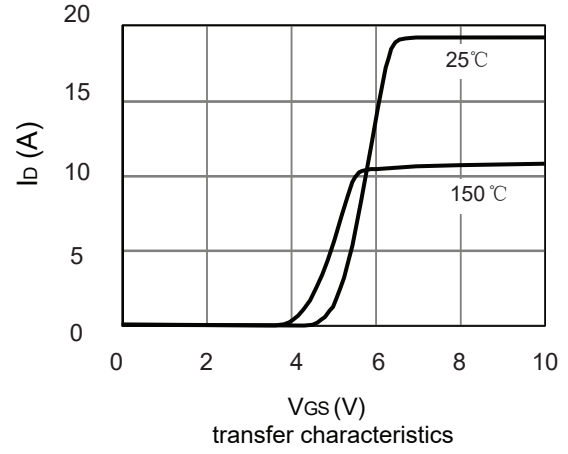
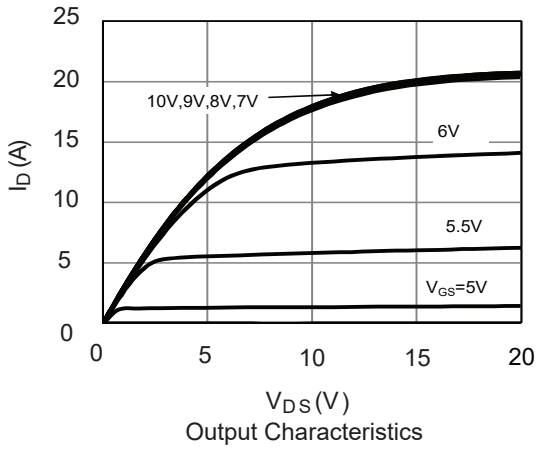
1. The EAS data shows Max. rating . The test condition is $V_{DD}=80V, V_{GS}=10V, L=20\text{mH}, I_{AS}=6.5A$.

This product has been designed and qualified for the consumer market.

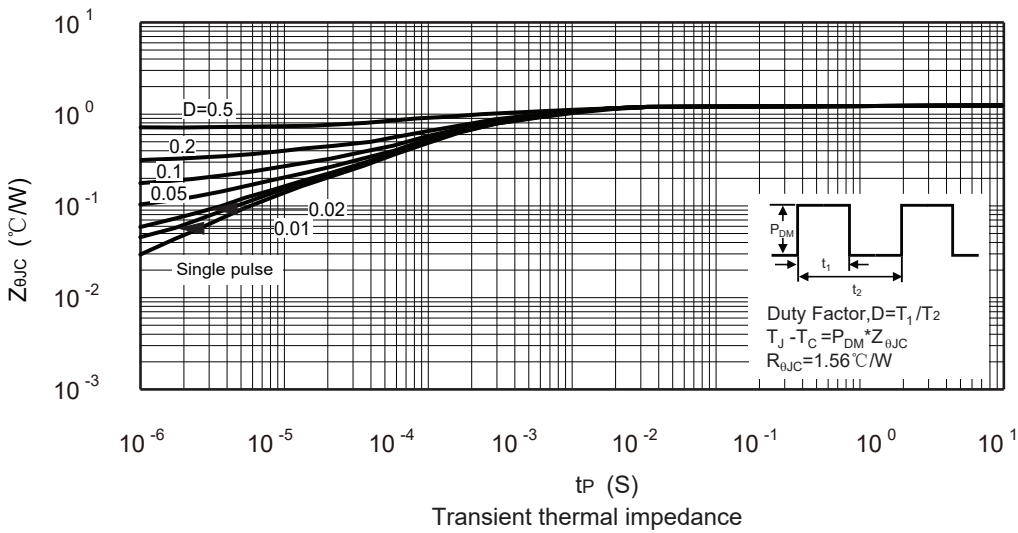
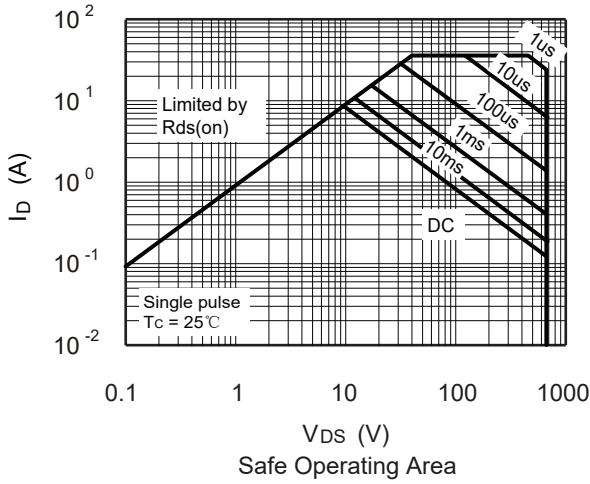
Cmos assumes no liability for customers' product design or applications.

Cmos reserves the right to improve product design ,functions and reliability without notice. Please refer to the latest version of specification.

Typical Characteristics

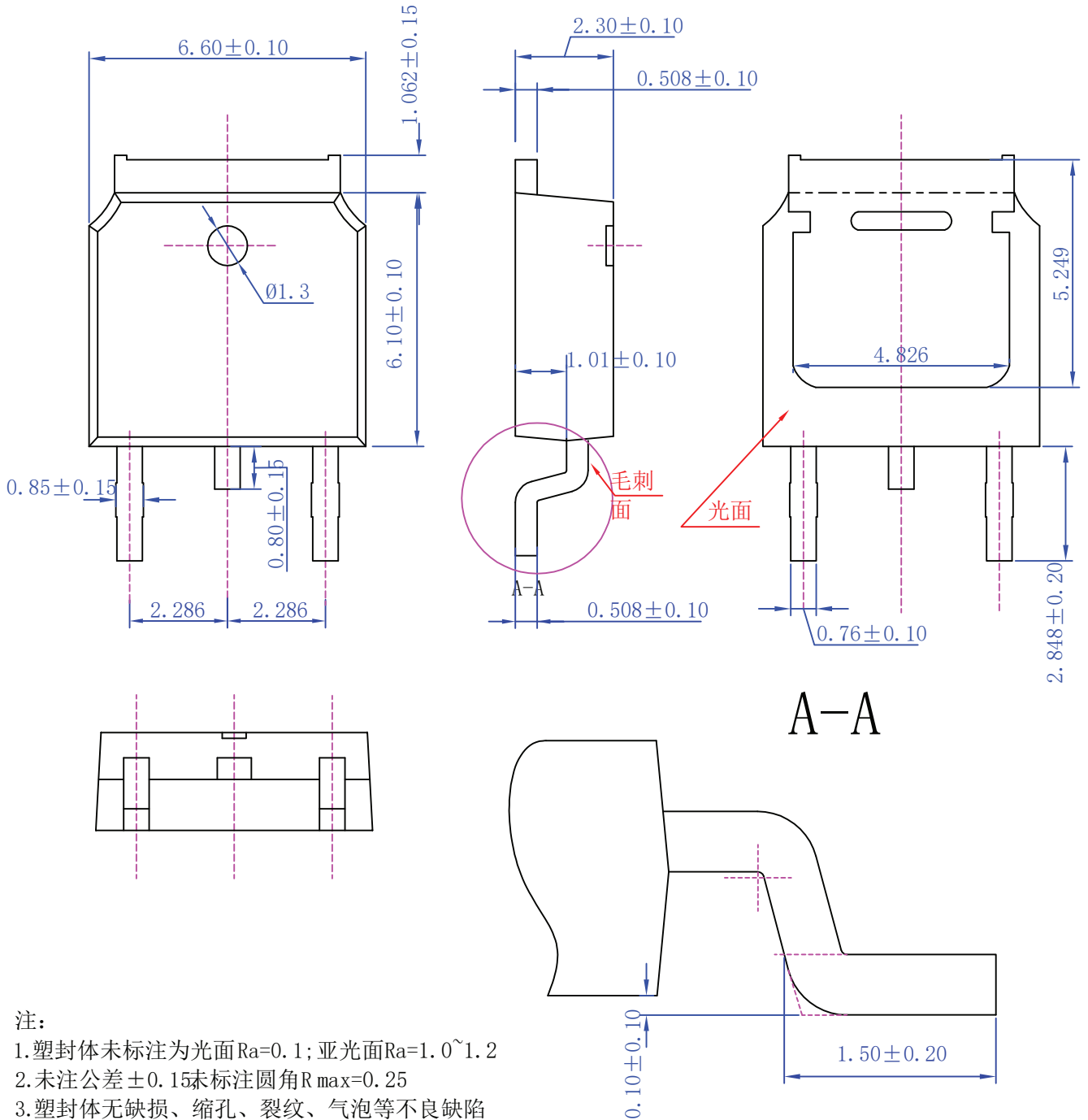


Typical Characteristics



Package Dimension

TO-252 Unit :mm



- 注:
1. 塑封体未标注为光面Ra=0.1; 亚光面Ra=1.0~1.2
 2. 未注公差±0.15未标注圆角R max=0.25
 3. 塑封体无缺损、缩孔、裂纹、气泡等不良缺陷
 4. 标注单位mm
 5. 顶针孔不允许凸出塑封体表面

Package Dimension

TO-251A

Unit :mm

