

General Description

The 65R290 is power MOSFET using Cmos's advanced super junction technology that can realize very low on resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of low EMI to designers as well as low switching loss.

Features

- Multi-layer Epitaxial Chip Technology
- Low On-Resistance
- 100% avalanche tested
- RoHS Compliant

Product Summary

BV _{DSS}	R _{DS(on)} max.	I _D
650V	0.3Ω	13A

Applications

- Charger
- Adaptor
- Power Supply

TO-252/TO-251 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25°C	Continuous Drain Current (Note 1)	13	A
I _D @T _C =100°C	Continuous Drain Current	8	A
I _{DM}	Pulsed Drain Current (Note 2)	52	A
EAS	Single Pulse Avalanche Energy (Note 3)	453	mJ
P _D @T _C =25°C	Total Power Dissipation	132	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Rating	Unit
R _{θJA}	Thermal Resistance Junction-ambient	127	°C/W
R _{θJC}	Thermal Resistance Junction-case	0.95	°C/W

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=6A$	---	0.27	0.3	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2	---	4	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=650V, V_{GS}=0V, T_J=150^{\circ}\text{C}$	---	5	---	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=6A$	---	7	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	9	---	Ω
Q_g	Total Gate Charge	$I_D=7.5A$	---	24	---	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	---	5	---	
Q_{gd}	Gate-Drain Charge	$V_{GS}=10V$	---	10	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=400V$ $V_{GS}=10V$ $I_D=7.5A$ $R_G=25\Omega$	---	14	---	ns
T_r	Rise Time		---	24	---	
$T_{d(off)}$	Turn-Off Delay Time		---	97	---	
T_f	Fall Time		---	22	---	
C_{iss}	Input Capacitance	$V_{DS}=100V, V_{GS}=0V, f=1\text{MHz}$	---	660	---	pF
C_{oss}	Output Capacitance		---	40	---	
C_{rss}	Reverse Transfer Capacitance		---	2.3	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current	---	---	13	A
I_{SM}	Pulsed Source Current		---	---	52	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V, I_S=12A, T_J=25^{\circ}\text{C}$	---	0.88	1.2	V
t_{rr}	Reverse Recovery Time	$di/dt = 100A/\mu s$	---	250	---	ns
Q_{rr}	Reverse Recovery Charge	$V_{DS}=100V, I_{SD}=7.5A$	---	2.94	---	μC

Notes:

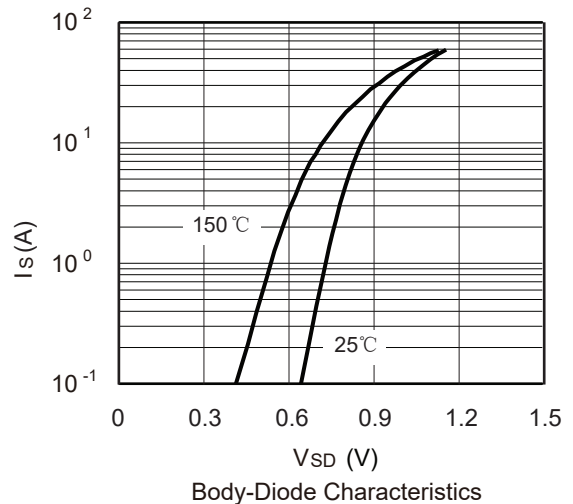
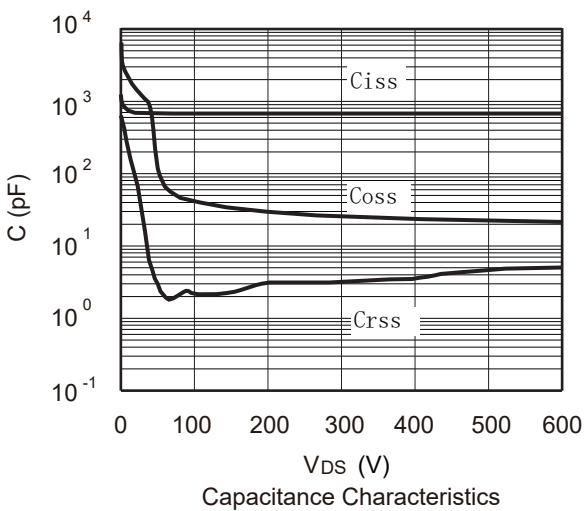
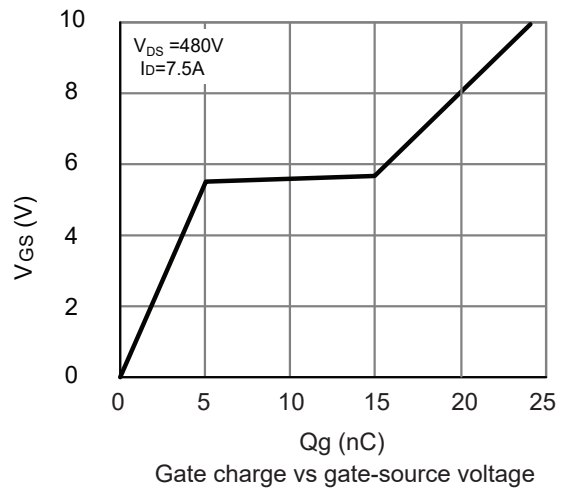
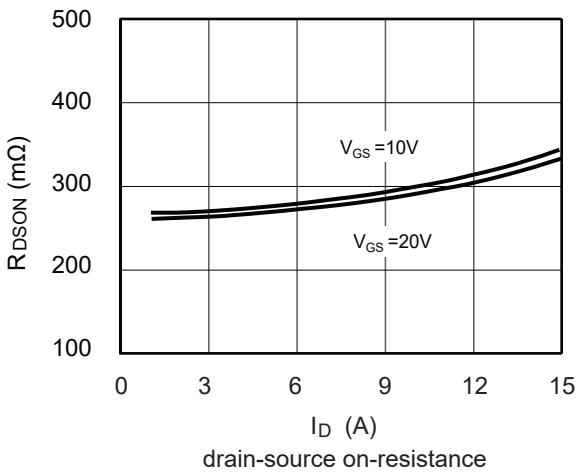
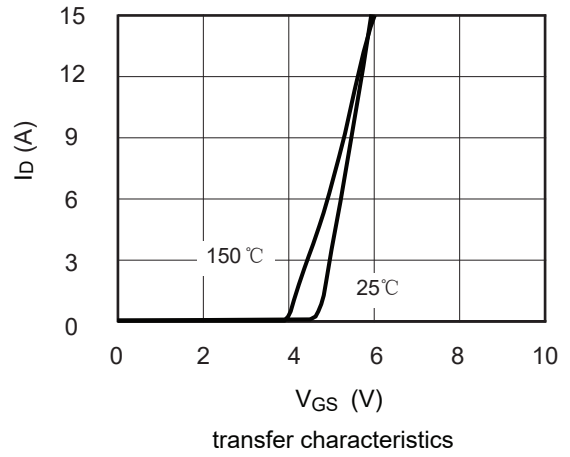
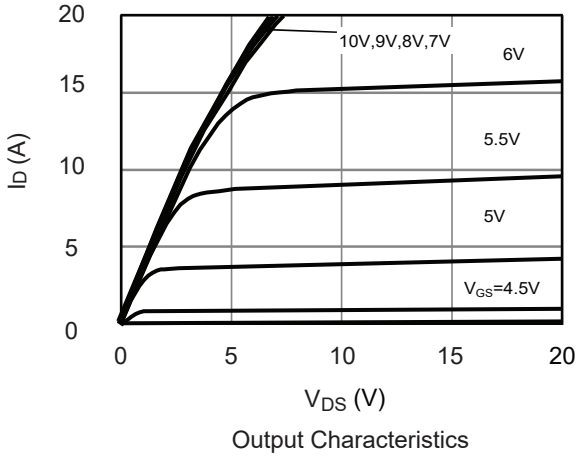
- Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$
- Pulse width t_p limited by $T_{j,max}$.
- The EAS data shows Max. rating. The test condition is $V_{DS}=80V, V_{GS}=10V, L=30mH, I_{AS}=5.5A$.

This product has been designed and qualified for the consumer market.

Cmos assumes no liability for customers' product design or applications.

Cmos reserves the right to improve product design, functions and reliability without notice. Please refer to the latest version of specification.

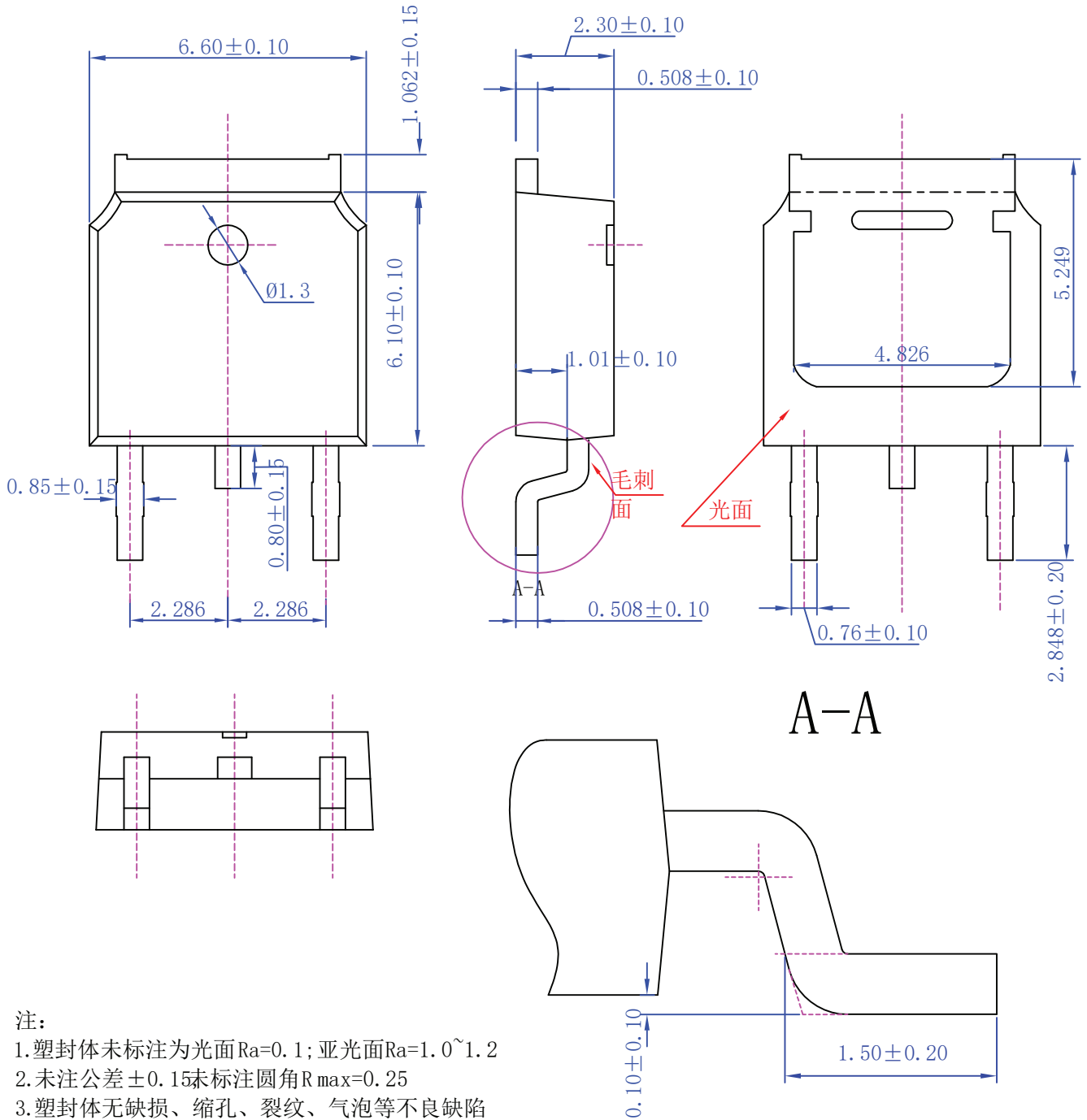
Typical Characteristics



Package Dimension

TO-252

Unit :mm



- 注:
1. 塑封体未标注为光面Ra=0.1; 亚光面Ra=1.0~1.2
 2. 未注公差±0.15未标注圆角R max=0.25
 3. 塑封体无缺损、缩孔、裂纹、气泡等不良缺陷
 4. 标注单位mm
 5. 顶针孔不允许凸出塑封体表面

