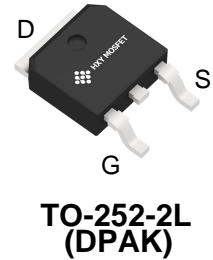




### Description

The STD90N4F3 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V.

This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = 40V$   $I_D = 80A$

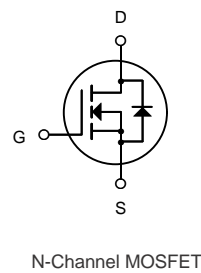
$R_{DS(ON)} < 5.4m\Omega @ V_{GS}=10V$

### Application

Battery protection

Load switch

Uninterruptible power supply



### Ordering Information

Product ID	Pack	Brand	Qty(PCS)
STD90N4F3	TO-252-2L(DPAK)	HXY MOSFET	2500

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	60	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	38	A
$I_{DM}$	Pulsed Drain Current	240	A
EAS	Single Pulse Avalanche Energy	100	mJ
$I_{AS}$	Avalanche Current	28	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation	114	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	37	$^\circ C/W$



### Electrical Characteristics ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$			1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.3	1.9	2.5	V
$R_{DS(on)}$	Static Drain-Source ON-Resistance <sup>(4)</sup>	$V_{GS} = 10\text{V}, I_D = 30\text{A}$		5.4	7.0	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$		8.1	10.5	m $\Omega$
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 20\text{V},$ $f = 1\text{MHz}$		2443		pF
$C_{oss}$	Output Capacitance			167		pF
$C_{rss}$	Reverse Transfer Capacitance			138		pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}, V_{DS} = 20\text{V}, I_D = 20\text{A}$		48		nC
$Q_{gs}$	Gate Source Charge			10		nC
$Q_{gd}$	Gate Drain("Miller") Charge			10		nC
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DD} = 20\text{V}$ $I_D = 20\text{A}, R_{GEN} = 3\Omega$		10		ns
$t_r$	Turn-On Rise Time			28		ns
$t_{d(off)}$	Turn-Off Delay Time			40		ns
$t_f$	Turn-Off Fall Time			7		ns
$I_S$	Maximum Continuous Drain to Source Diode Forward Current				60	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current				240	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$			1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A}/\mu\text{s}$		11		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge				5	

- Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.  
2.  $E_{AS}$  condition: Starting  $T_J=25^\circ\text{C}$ ,  $V_{DD}=20\text{V}$ ,  $V_G=10\text{V}$ ,  $R_G=25\text{ohm}$ ,  $L=0.5\text{mH}$ ,  $I_{AS}=20\text{A}$   
3.  $R_{\theta JA}$  is measured with the device mounted on a  $1\text{inch}^2$  pad of 2oz copper FR4 PCB  
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 0.5\%$ .



### Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

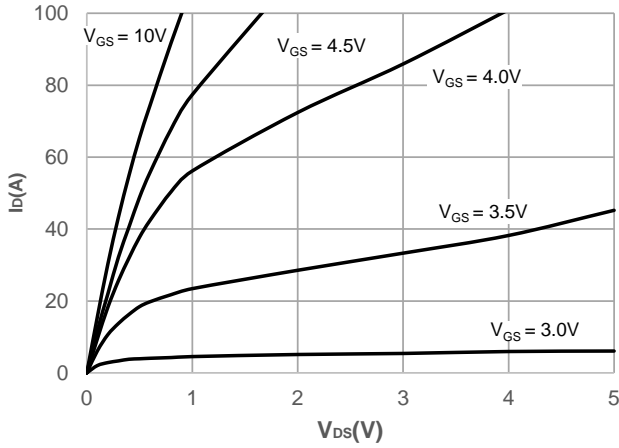


Figure 3: On-resistance vs. Drain Current

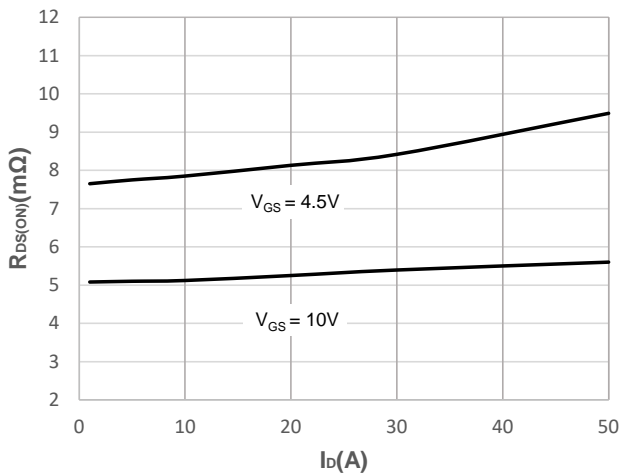


Figure 5: Gate Charge Characteristics

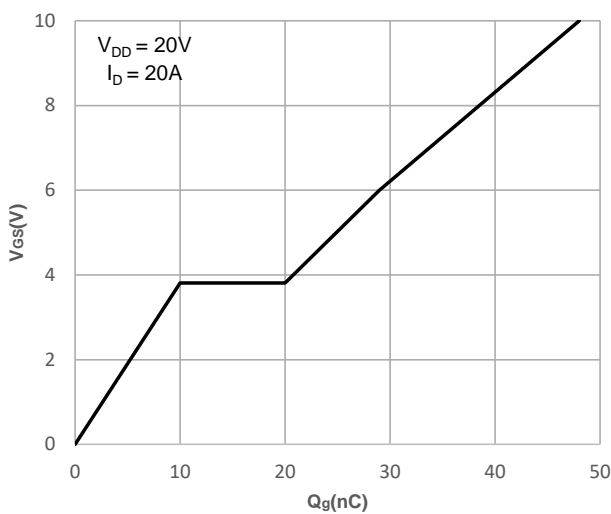


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

Figure 2: Typical Transfer Characteristics

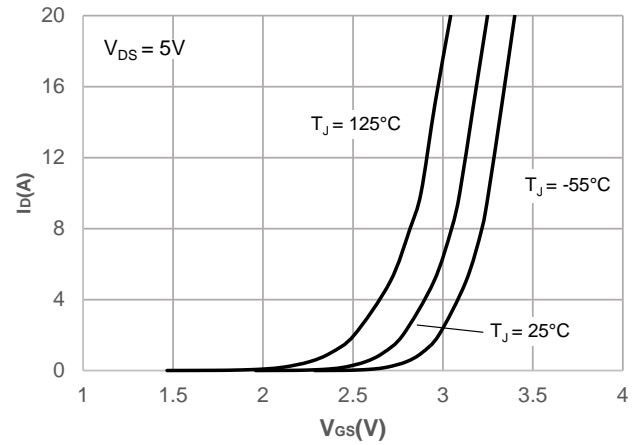


Figure 4: Body Diode Characteristics

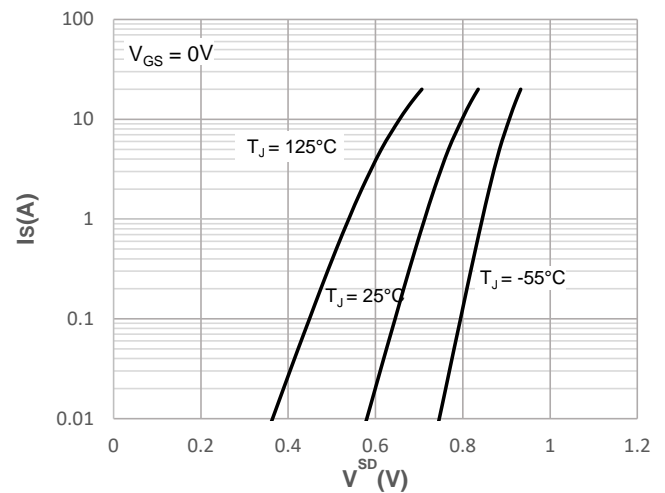


Figure 6: Capacitance Characteristics

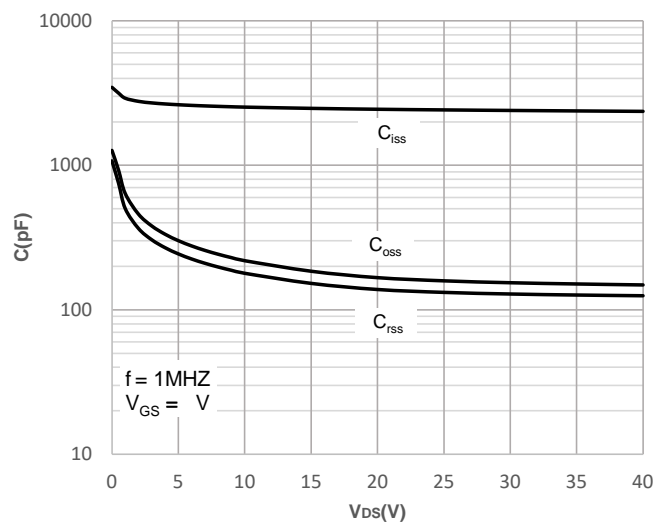


Figure 8: Normalized on Resistance vs. Junction Temperature

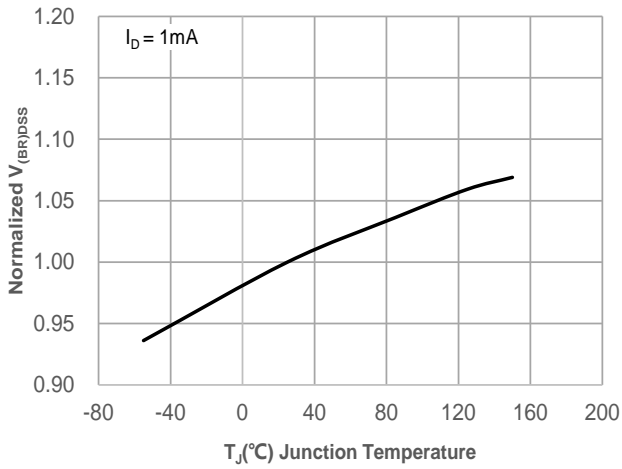


Figure 9: Maximum Safe Operating Area

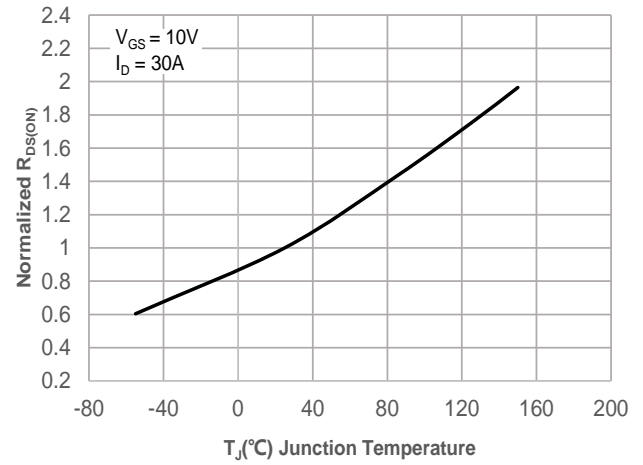


Figure 10: Maximum Continuous Drianc Current vs. Case Temperature

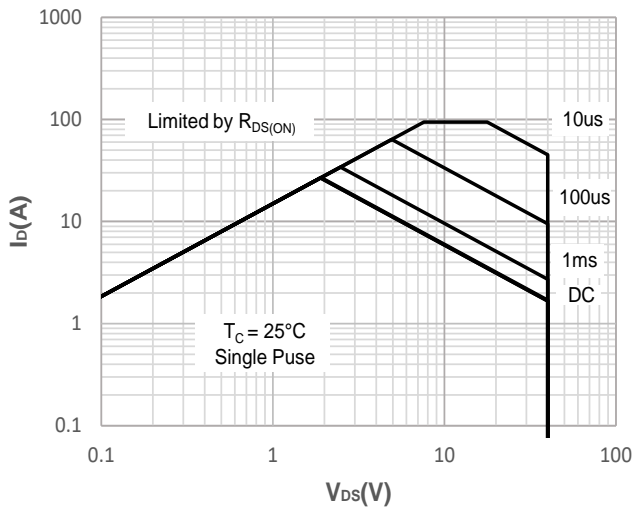


Figure 11: Normalized Maximum Transient Thermal Impedance

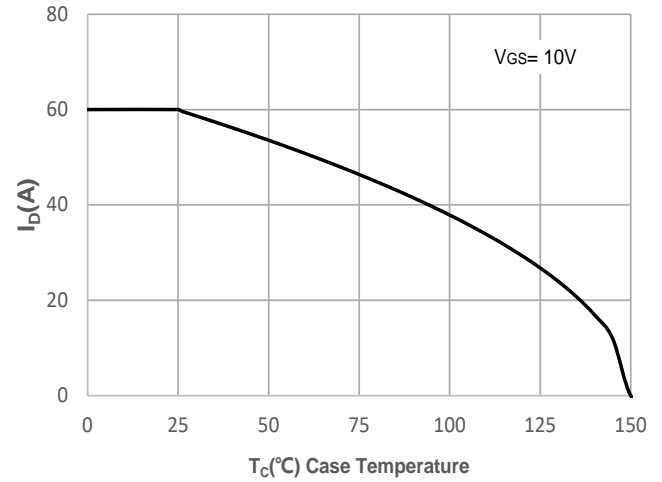
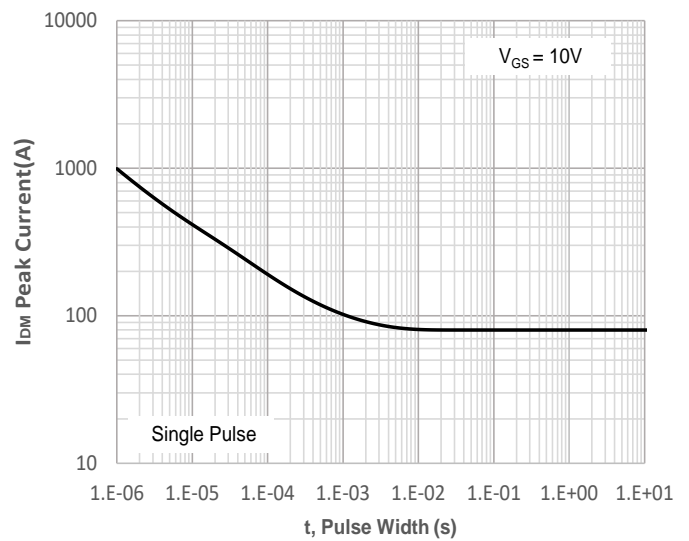
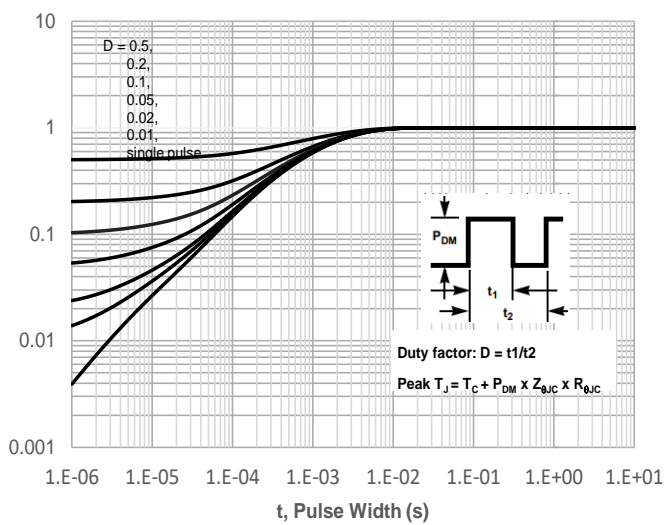


Figure 12: Peak Current Capacity





### Test Circuit

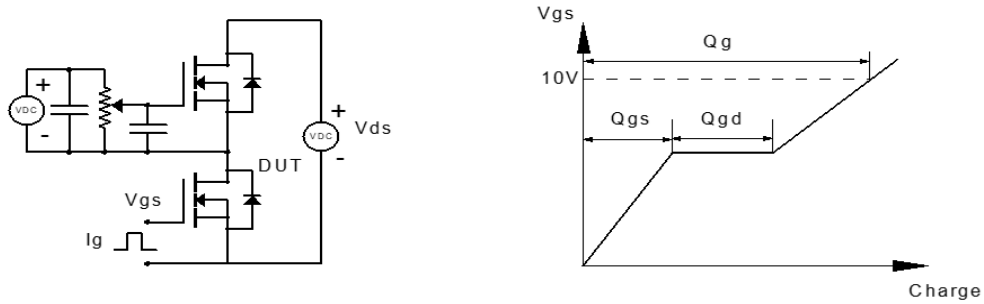


Figure 1: Gate Charge Test Circuit & Waveform

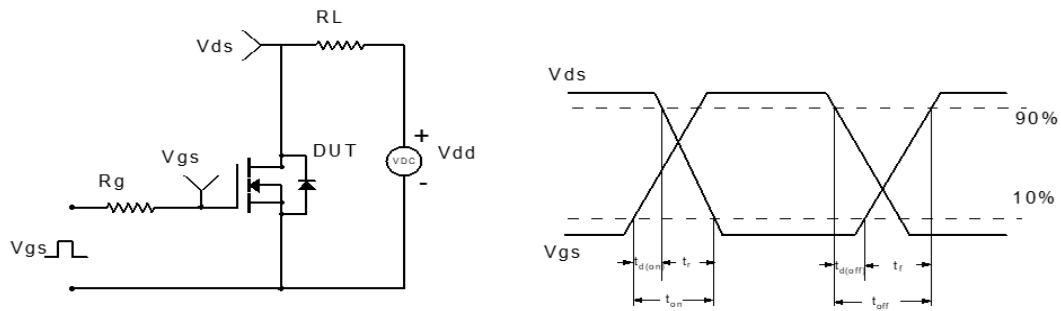


Figure 2: Resistive Switching Test Circuit & Waveform

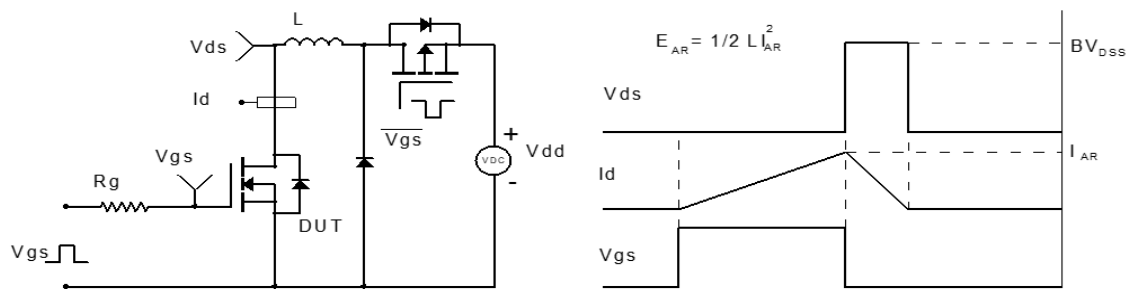


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

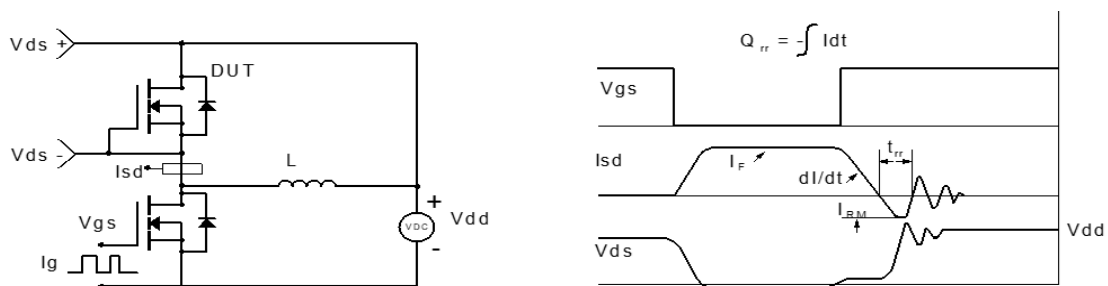
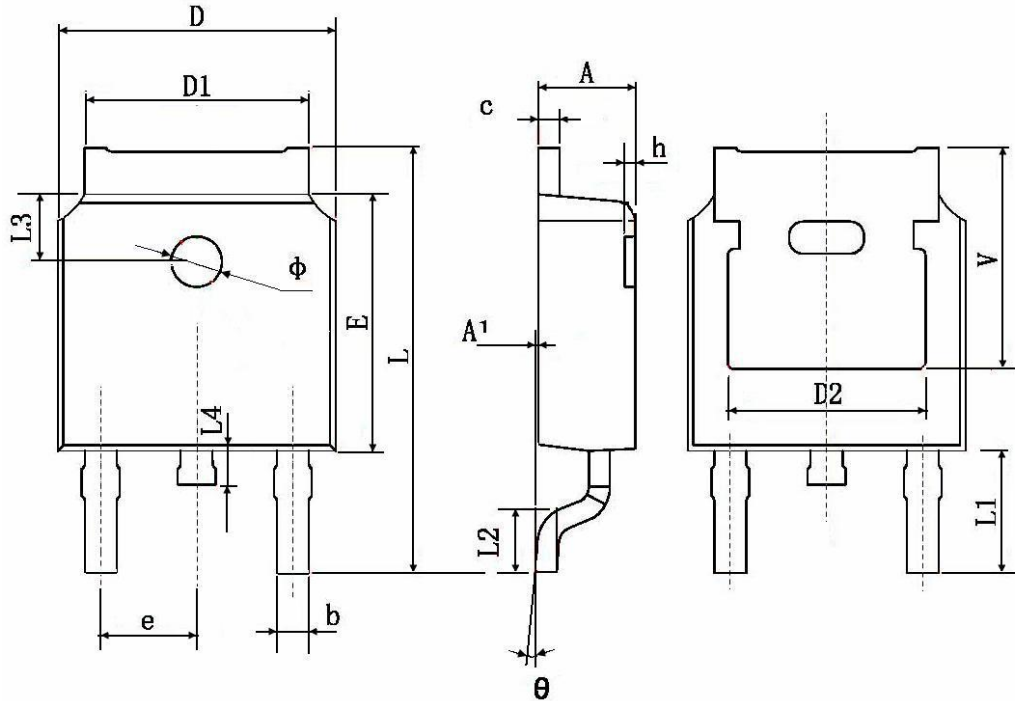


Figure 4: Diode Recovery Test Circuit & Waveform



### TO-252-2L(DPAK) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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