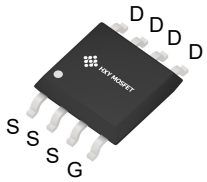
SQ4182EY-T1_GE3

N-Channel Enhancement Mode MOSFET

Description

The SQ4182EY-T1□GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

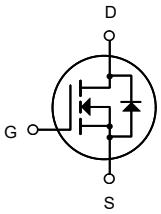


SOP-8
(SO-8)

General Features

V_{DS} = 30V I_D = 30A

$R_{DS(ON)}$ < 4.5mΩ @ V_{GS}=10V



N-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SQ4182EY-T1□GE3	SOP-8(SO-8)	HXY MOSFET	3000

Absolute Maximum Ratings (T_C =25°C unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current-Continuous	30	A
I_D (100℃)	Drain Current-Continuous(T_C=100℃)	21	A
I_{DM}	Pulsed Drain Current	120	A
P_D	Maximum Power Dissipation	1.4	W
E_{AS}	Single pulse avalanche energy	156	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	℃
$R_{\theta JA}$	Thermal Resistance,Junction-to-Case	90	℃/W

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=30V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1.2	1.5	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[4]	V_{GS}=10V,I_D=10A	---	3.3	4.5	mΩ
		V_{GS}=4.5V,I_D=5A	---	4.6	5.5	mΩ
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	---	3100	---	pF
C_{oss}	Output Capacitance		---	370	--	
C_{rss}	Reverse Transfer Capacitance		---	286	---	
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, I_D=30A, R_{ENG}=3Ω,V_{GS}=10V	---	11	---	ns
t_r	Rise Time		---	30	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	49	---	ns
t_f	Fall Time		---	18	---	ns
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=30A	---	24	---	nC
Q_{gs}	Gate-Source Charge		---	12	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	13	---	nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_{SD}=30A	---	---	1.2	V
I_S	Continuous Drain Curren	V_D=V_G=0V	---	---	30	A
I_{SM}	Pulsed Drain Current		---	---	120	A
Trr	Reverse Recovery Time	I_F=30A,T_J=25℃dI/dt=100A/us	---	16	---	ns
Qrr	Reverse Recovery Charge		---	7	---	nC

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : T_J=25℃,V_{DD}=15V,V_G=10V,L=0.5mH
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics

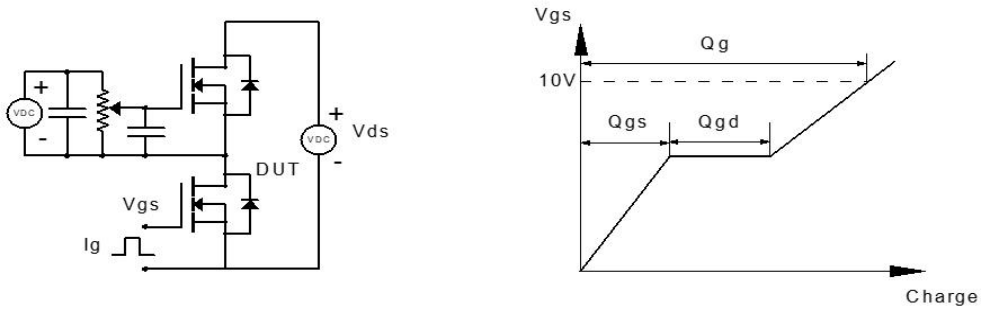


Figure 1: Gate Charge Test Circuit & Waveform

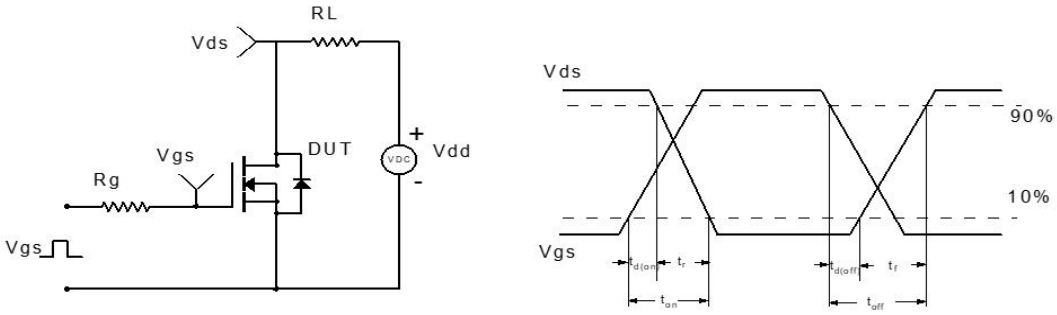


Figure 2: Resistive Switching Test Circuit & Waveform

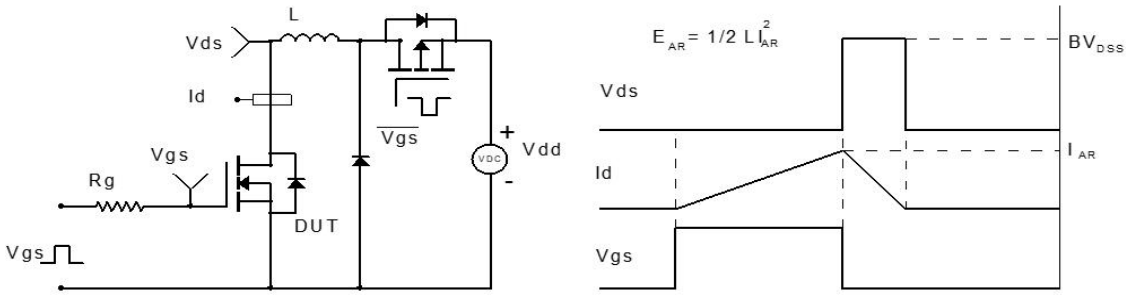


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

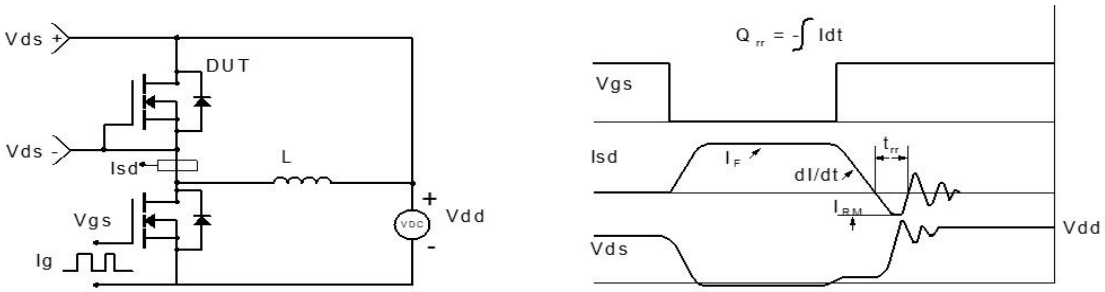
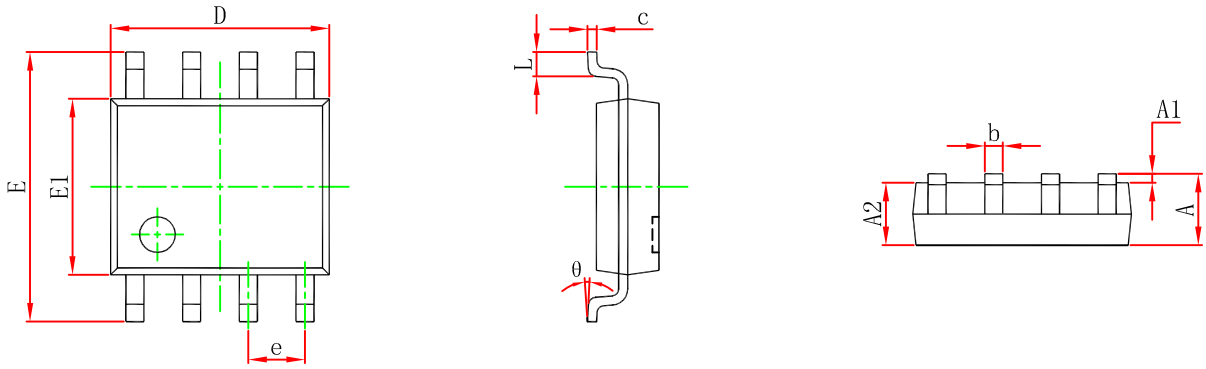
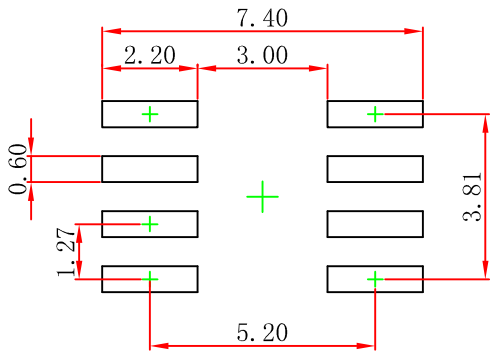


Figure 4: Diode Recovery Test Circuit & Waveform

SOP-8(SO-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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