



## Description

The DMT64M8LCG-7 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

## General Features

$V_{DS} = 60V$   $I_D = 100A$

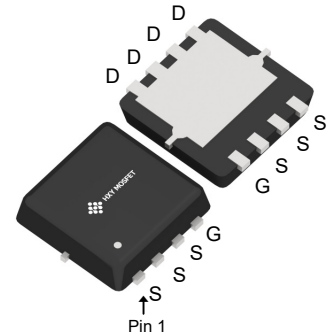
$R_{DS(ON)} < 4 m\Omega @ V_{GS}=20V$

## Application

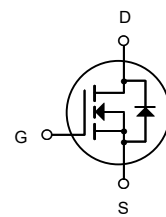
Battery protection

Load switch

Uninterruptible power supply



DFN3X3-8L



N-Channel MOSFET

## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMT64M8LCG-7	DFN3X3-8L	HXY MOSFET	5000

## Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	100	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	64	A
$I_{DM}$	Pulsed Drain Current	385	A
EAS	Single Pulse Avalanche Energy	80	mJ
$I_{AS}$	Avalanche Current	22	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	73.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	51	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case	1.7	°C/W



**Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60	-	-	V	
Gate-body Leakage Current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60V, V_{GS} = 0V$	$T_J=25^{\circ}\text{C}$	-	-	1	$\mu A$
			$T_J=100^{\circ}\text{C}$	-	-		
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.7	2.5	V	
Drain-Source On-Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 21A$	-	4.0	4.8	m $\Omega$	
		$V_{GS} = 4.5V, I_D = 10A$	-	5.2	6.6		
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{DS} = 10V, I_D = 21A$	-	89	-	S	
Input Capacitance	$C_{iss}$	$V_{DS} = 30V, V_{GS} = 0V, f = 1MHz$	-	2180	-	pF	
Output Capacitance	$C_{oss}$		-	735	-		
Reverse Transfer Capacitance	$C_{rss}$		-	42	-		
Gate Resistance	$R_g$	$f = 1MHz$	-	1.8	-	$\Omega$	
Total Gate Charge	$Q_g$	$V_{GS} = 10V, V_{DS} = 30V, I_D = 21A$	-	35	-	nC	
Gate-Source Charge	$Q_{gs}$		-	6.6	-		
Gate-Drain Charge	$Q_{gd}$		-	8.4	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 30V, R_G = 3\Omega, I_D = 21A$	-	9.4	-	ns	
Rise Time	$t_r$		-	8.4	-		
Turn-Off Delay Time	$t_{d(off)}$		-	32.5	-		
Fall Time	$t_f$		-	12.5	-		
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20A, dI/dt = 100A / \mu s$	-	50	-	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	20	-	nC	
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$I_S = 21A, V_{GS} = 0V$	-	-	1.2	V	
Continuous Source Current	$I_S$	$T_C = 25^{\circ}\text{C}$	-	-	100	A	

**Notes:**

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^{\circ}\text{C}$
2. The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=40A$ .
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.



## Typical Characteristics

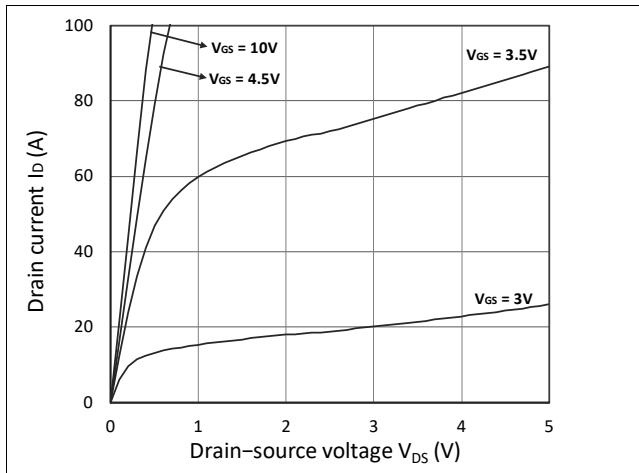


Figure 1. Output Characteristics

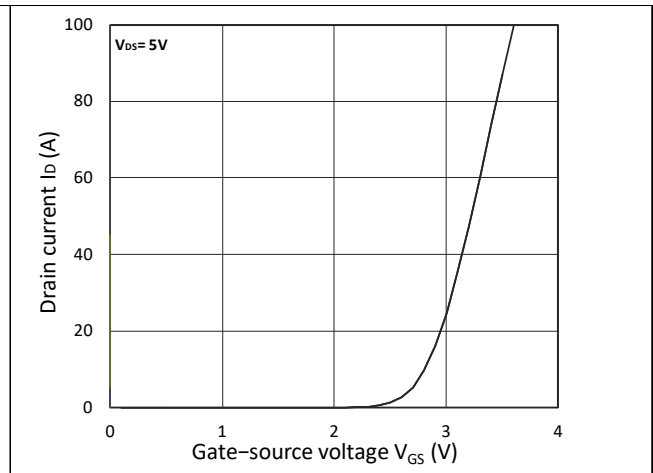


Figure 2. Transfer Characteristics

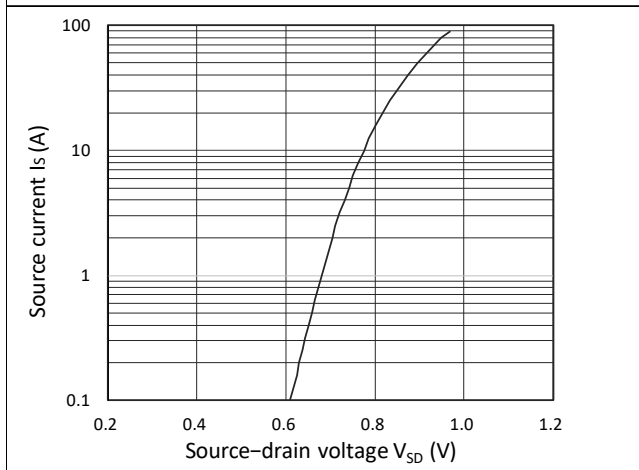


Figure 3. Forward Characteristics of Reverse

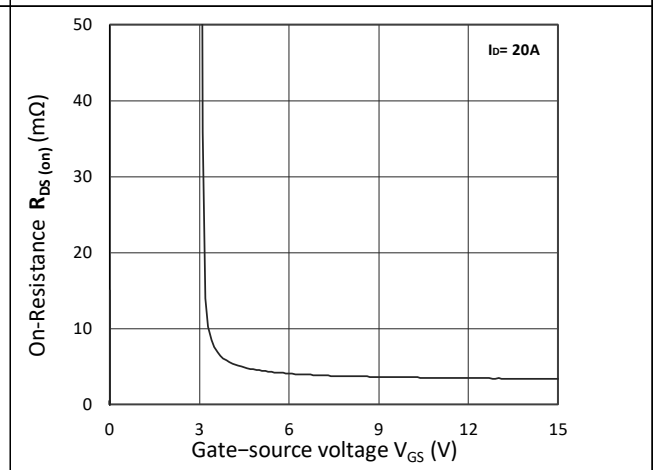


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$

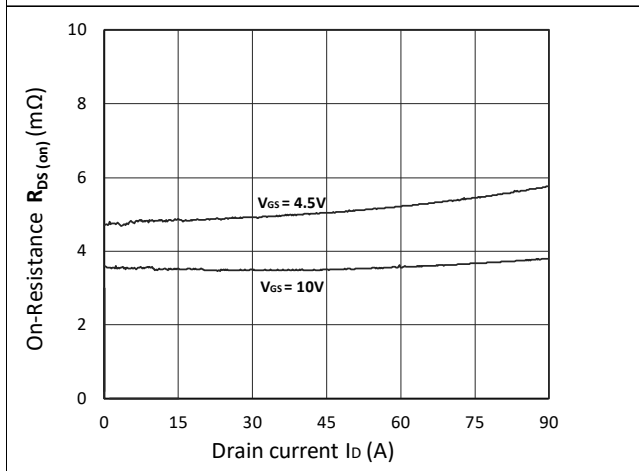


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$

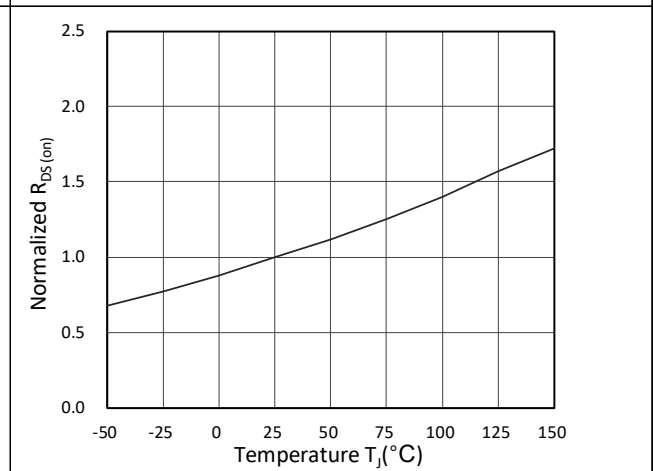


Figure 6. Normalized  $R_{DS(ON)}$  vs. Temperature

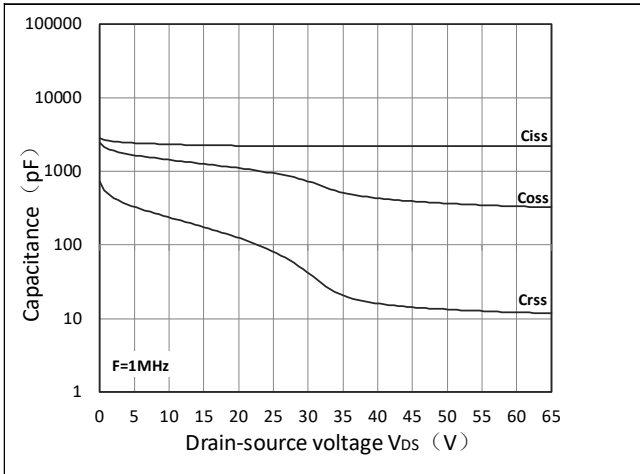


Figure 7. Capacitance Characteristics

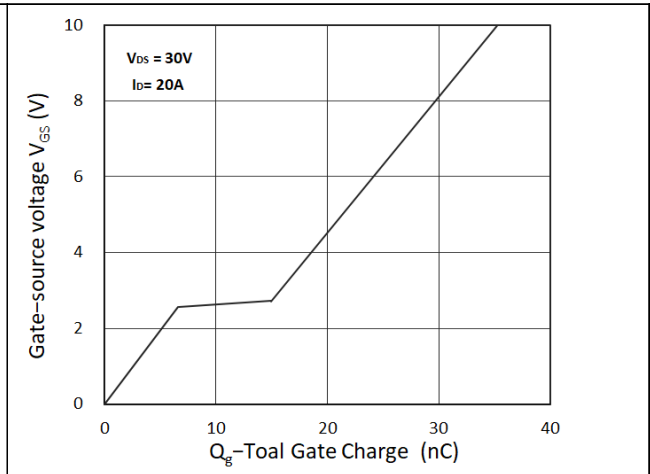


Figure 8. Gate Charge Characteristics

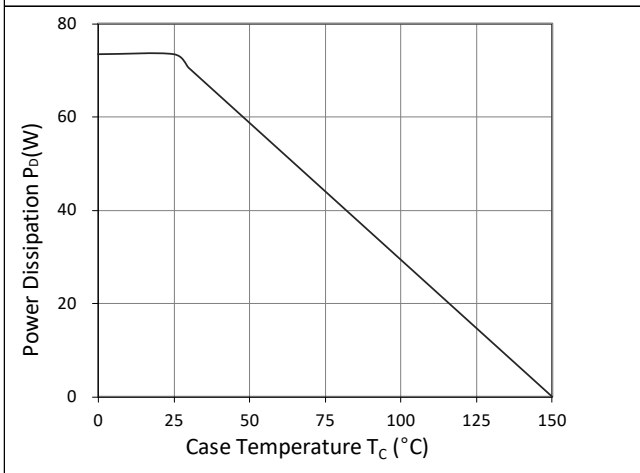


Figure 9. Power Dissipation

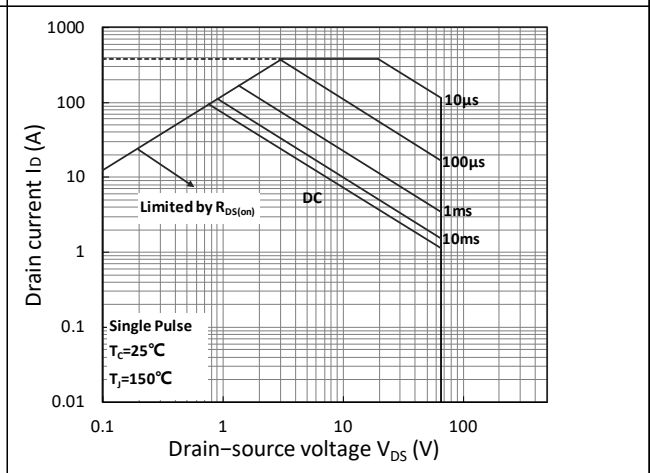


Figure 10. Safe Operating Area

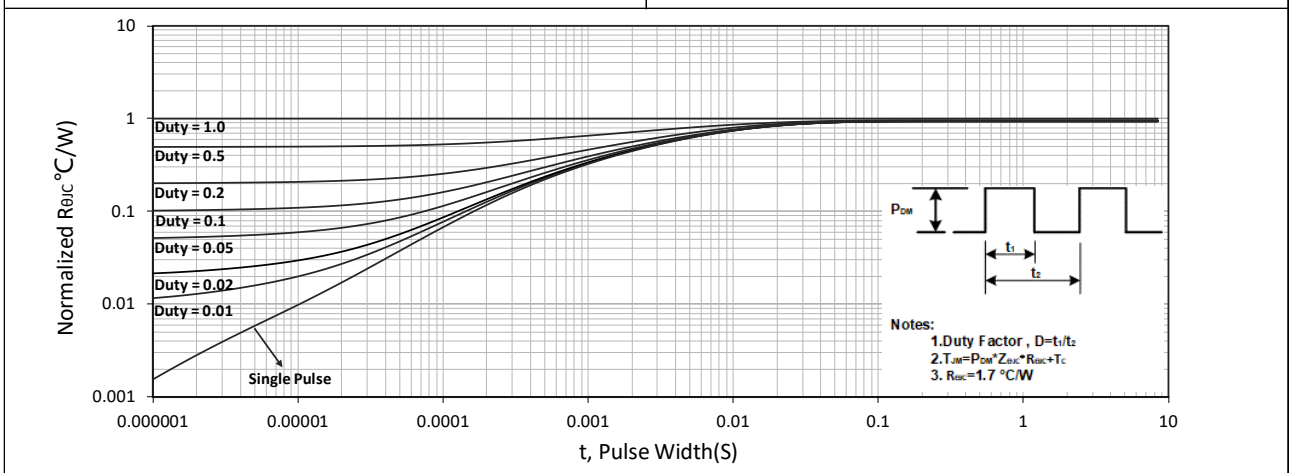


Figure 11. Normalized Maximum Transient Thermal Impedance



### Test Circuit

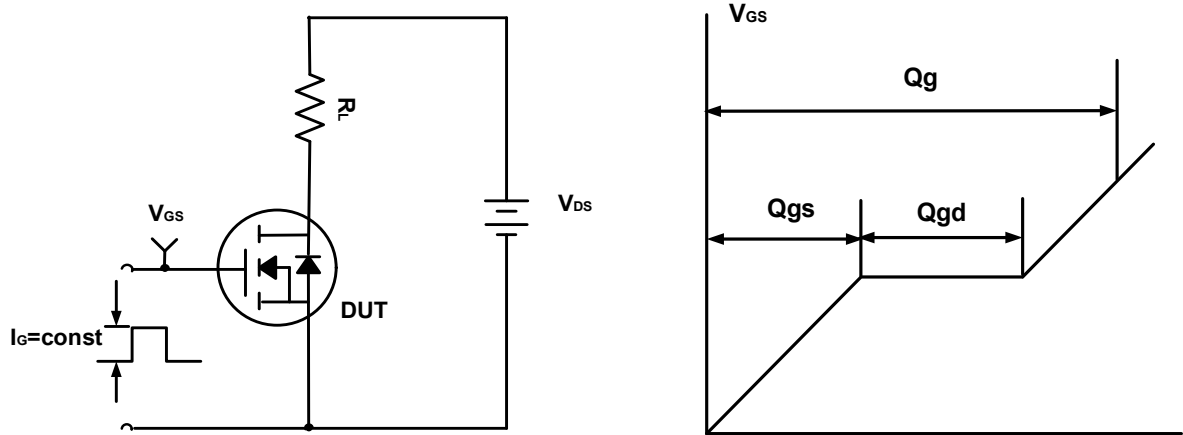


Figure A. Gate Charge Test Circuit & Waveforms

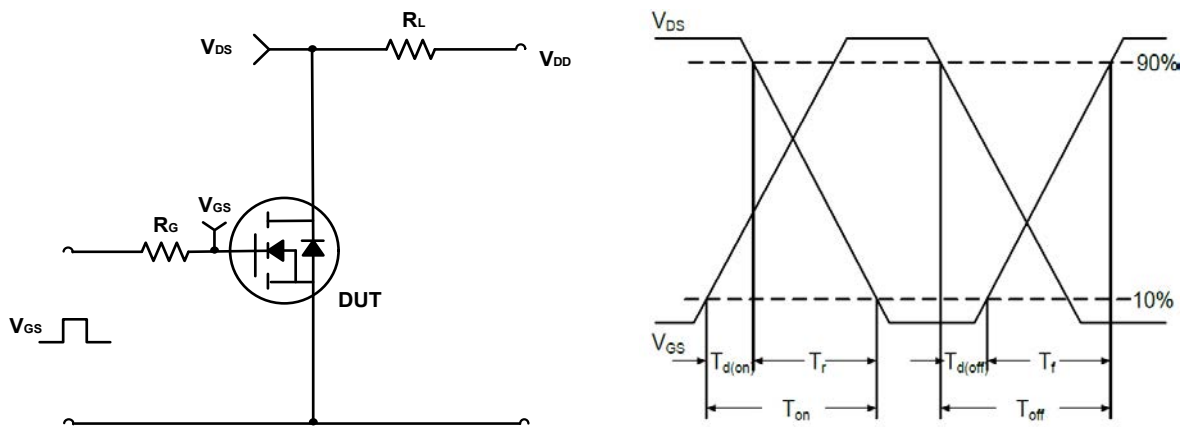


Figure B. Switching Test Circuit & Waveforms

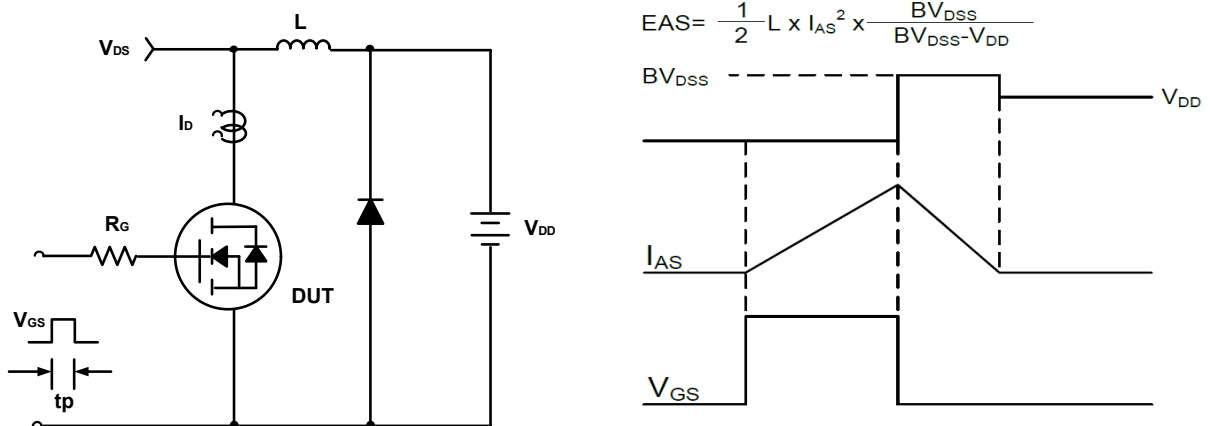
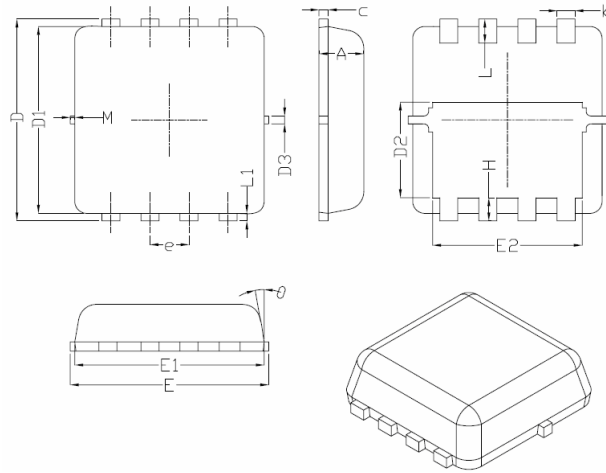


Figure C. Unclamped Inductive Switching Circuit & Waveforms



### DFN3X3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
$\theta$		10°	12°



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