



Description

The STFU13N65M2 can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220/TO-220F, which accords with the RoHS standard.

General Features

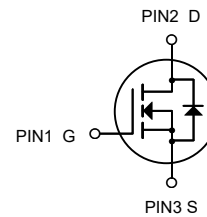
$V_{DS} = 650V, I_D = 20A$
 $R_{DS(ON)} < 0.3\Omega @ V_{GS}=10V$

Application

- Power switch circuit of adaptor and charger.



TO-220F



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Units Tube
STFU13N65M2	TO-220F	HXY MOSFET	50

Absolute Maximum Ratings@T=25°C(unless otherwise specified)

Symbol	Parameter	Limit	Unit
V_{DSS}	Drain-to-Source Voltage ^[1]	650	V
V_{GSS}	Gate-to-Source Voltage	± 30	
I_D	Continuous Drain Current	20	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current @ $T_c=100^\circ C$	13	
I_{DM}	Pulsed Drain Current at $V_{GS}=10V^{[2]}$	80	
E_{AS}	Single Pulse Avalanche Energy	980	mJ
P_D	Power Dissipation	32	W
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	°C
T_J & T_{STG}	Operating and Storage Temperature Range	-55 to 150	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	55	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.



Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 30\text{V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	-	0.4	0.47	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1\text{MHz}$	-	3234	-	pF
C_{oss}	Output Capacitance		-	266	-	pF
C_{rss}	Reverse Transfer Capacitance		-	34	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 520\text{V}, I_D = 20\text{A}$	-	73	-	nC
Q_{gs}	Gate Source Charge		-	17	-	nC
Q_{gd}	Gate Drain ("Miller") Charge		-	29	-	nC
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 330\text{V}$ $I_D = 20\text{A}, R_{GEN} = 24\Omega$	-	45	-	ns
t_r	Turn-On Rise Time		-	64	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	218	-	ns
t_f	Turn-Off Fall Time		-	84	-	ns
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	80	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 20\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A}/\mu\text{s}$	-	494	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	7.9	-	μC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $V_G = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 10\text{mH}$, $I_{AS} = 14\text{A}$
 3. $R_{\theta JA}$ is measured with the device mounted on a minimum recommended pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Characteristics

Figure 1: Output Characteristics

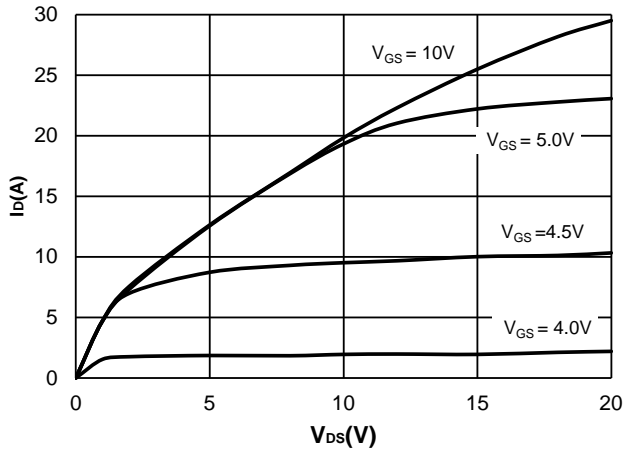


Figure 2: Typical Transfer Characteristics

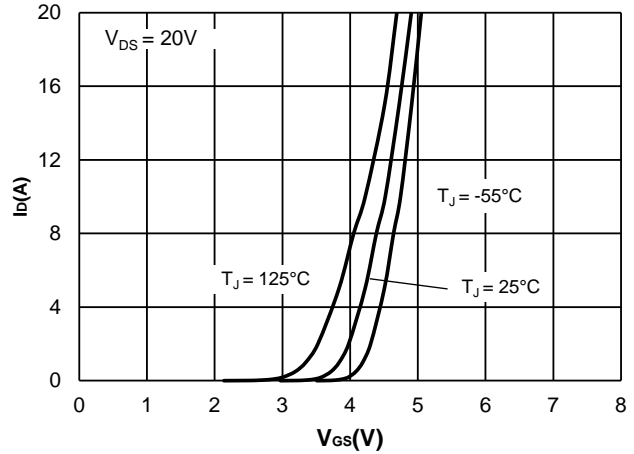


Figure 3: On-resistance vs. Drain Current

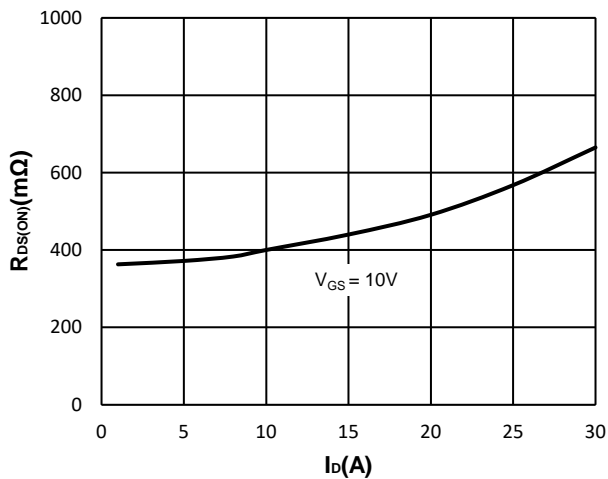


Figure 4: Body Diode Characteristics

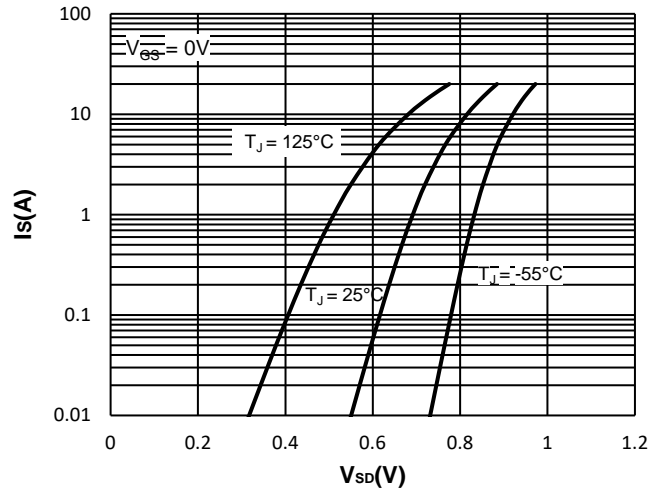


Figure 5: Gate Charge Characteristics

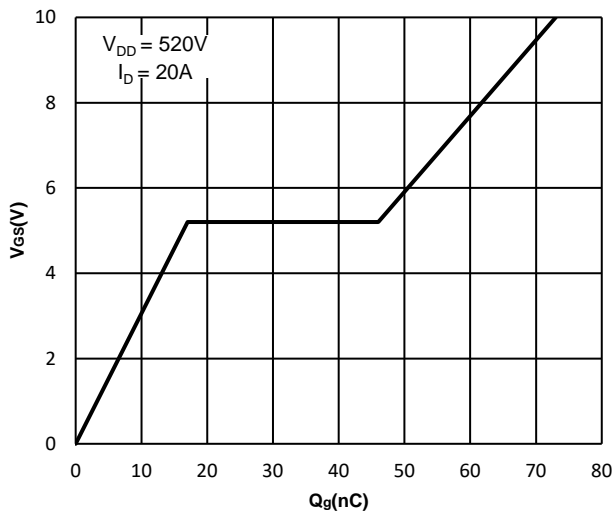


Figure 6: Capacitance Characteristics

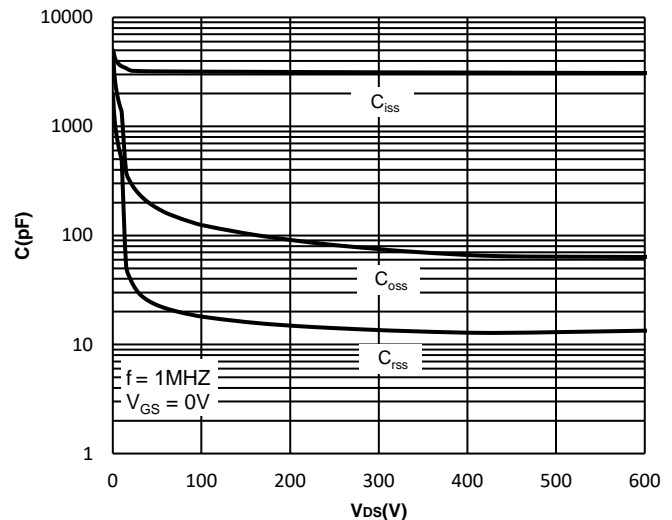




Figure 7: Normalized Breakdown voltage vs. Junction Temperature

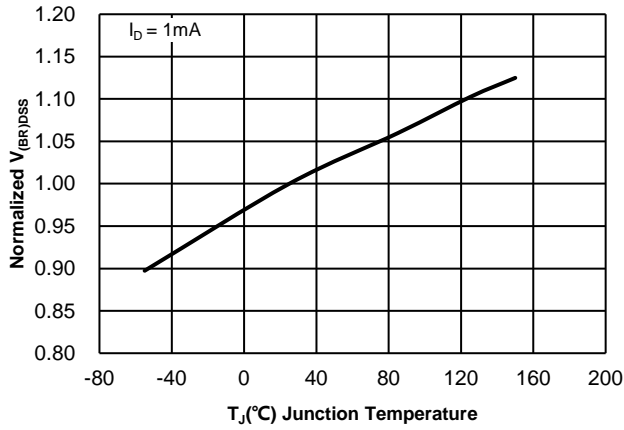


Figure 8: Normalized on Resistance vs. Junction Temperature

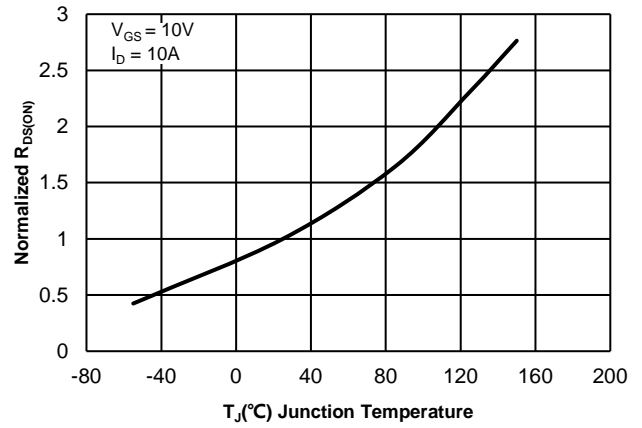


Figure 9: Maximum Safe Operating Area

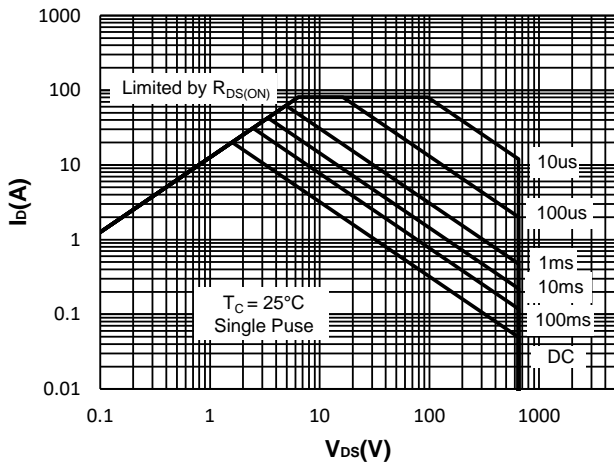


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

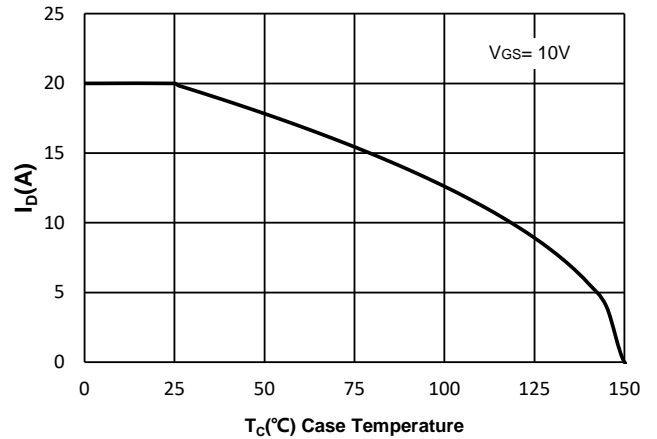


Figure 11: Normalized Maximum Transient Thermal Impedance

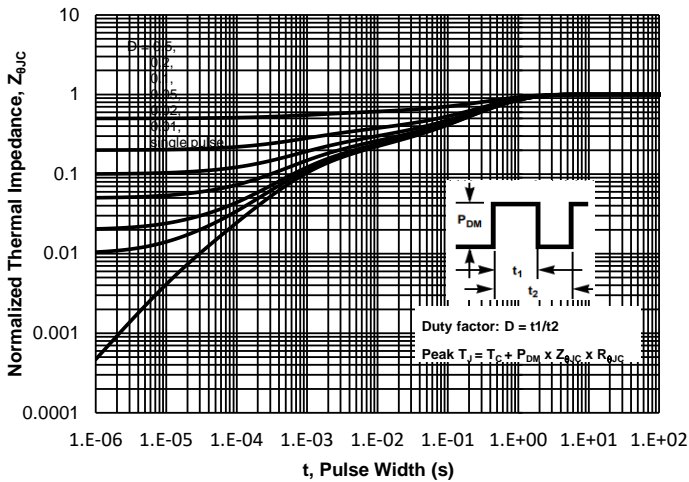
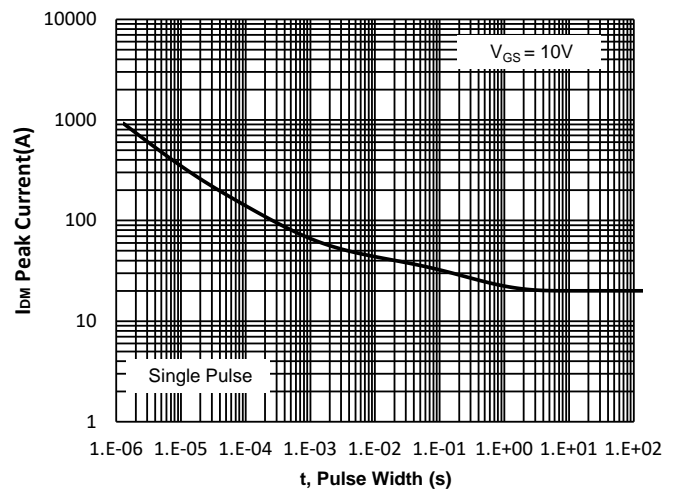


Figure 12: Peak Current Capacity





Test Circuit

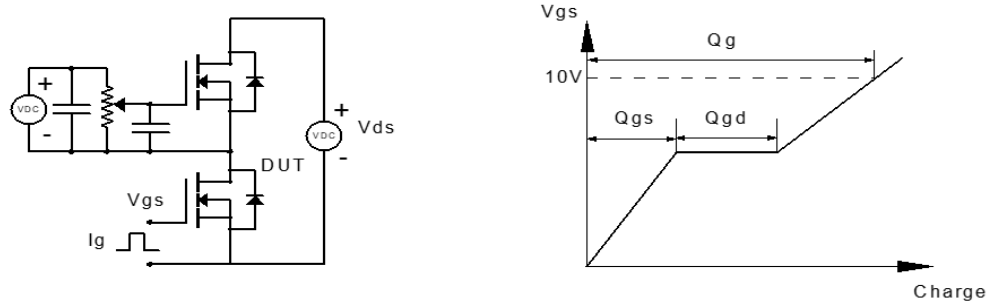


Figure 1: Gate Charge Test Circuit & Waveform

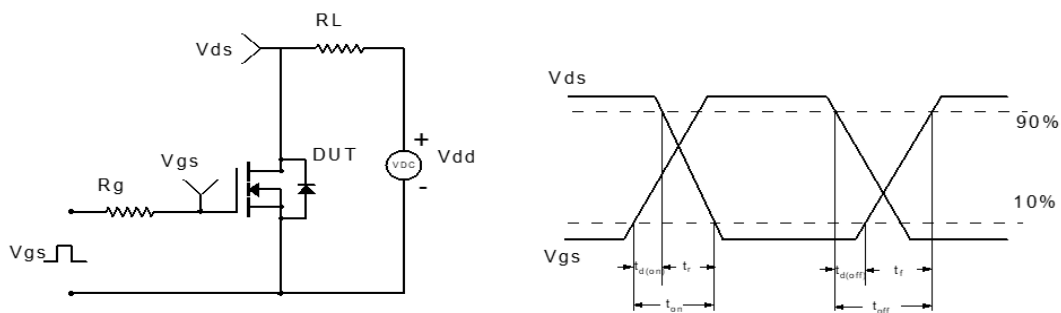


Figure 2: Resistive Switching Test Circuit & Waveform

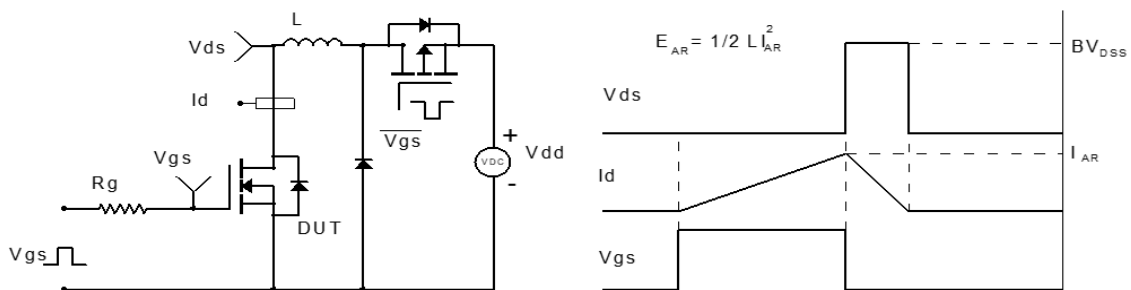


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

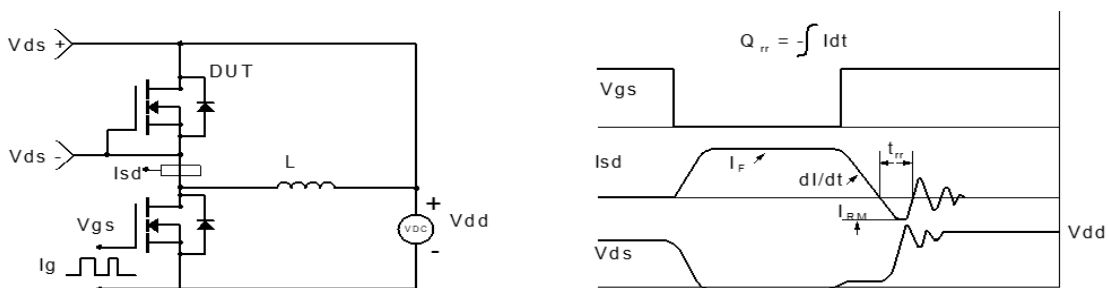
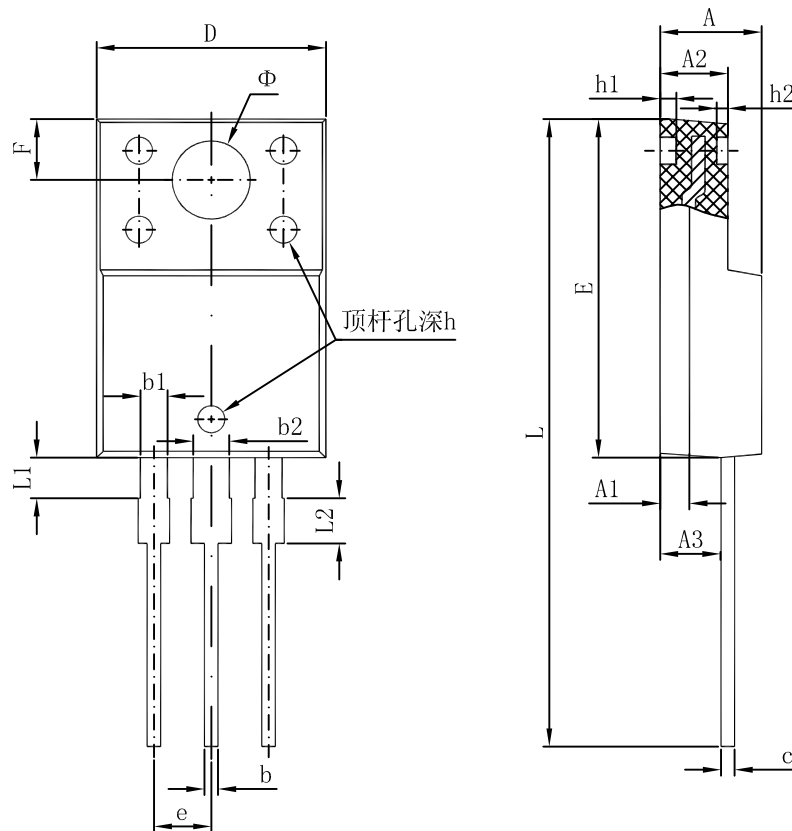


Figure 4: Diode Recovery Test Circuit & Waveform



Package Dimension TO-220F



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	1.300 REF.		0.051 REF.	
A2	2.800	3.200	0.110	0.126
A3	2.500	2.900	0.098	0.114
b	0.500	0.750	0.020	0.030
b1	1.100	1.350	0.043	0.053
b2	1.500	1.750	0.059	0.069
c	0.500	0.750	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540 TYP.		0.100 TYP.	
F	2.700 REF.		0.106 REF.	
Φ	3.500 REF.		0.138 REF.	
h	0.000	0.300	0.000	0.012
h1	0.800 REF.		0.031 REF.	
h2	0.500 REF.		0.020 REF.	
L	28.000	28.400	1.102	1.118
L1	1.700	1.900	0.067	0.075
L2	1.900	2.100	0.075	0.083



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