Features

- ±250mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift: ±0.3mV (max), ±0.9µV/°C (max)
- Fixed gain: 8
- Low gain error and drift: ±0.5% (max), ±30ppm/°C (max)
- Low nonlinearity and drift: 0.03%, ±1.5ppm/°C (typical)
- 3.3V to 5V operation on both sides
- System-level diagnostic features
- Safety-related certifications:

$4243V_{PK}$ basic isolation per DIN VDE V 0884-17: 2021-10

$3.0kV_{RMS}$ isolation for 1 minute per UL1577

- High CMTI: 150kV/µs (typical)

Applications

- Shunt-resistor-based current sensing in:
  - Motor drives
  - Frequency inverters
  - Uninterruptible power supplies

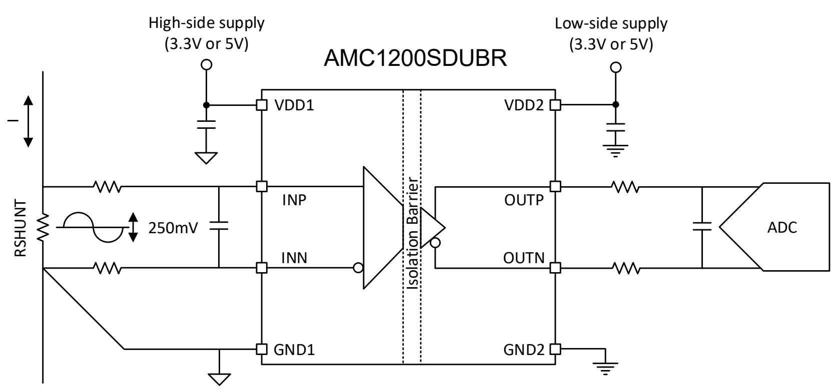
Description

The AMC1200SDUBR is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced or basic galvanic isolation of up to $5kV_{RMS}$ or $3kV_{RMS}$ according to VDE V 0884-17 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common- mode voltage levels and protects lower- voltage parts from damage.

The input of the AMC1200SDUBR is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings. The integrated missing high-side supply voltage detection and input common mode overvoltage detection simplify system- level design and diagnostics.

The AMC1200SDUBR is specified over the extended industrial temperature range of 40°C to +125°C.

PART NUMBER	PACKAGE	BODY SIZE
AMC1200SDUBR	NB SOIC-8	4.9mm*3.9mm



Simplified Schematic

1 Pin Configurations and Functions

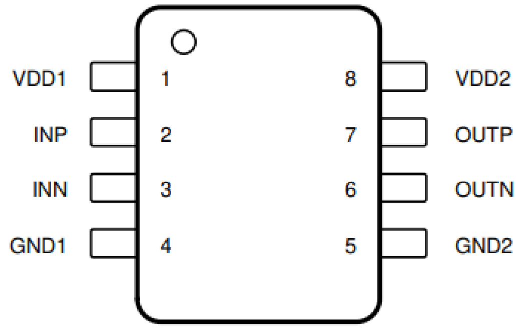


Figure 1. Pin Configuration, Top View

Pin Functions and Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	VDD1	High-side power	High-side power supply, 3.0V to 5.5V relative to GND1.
2	INP	Analog input	Noninverting analog input.
3	INN	Analog input	Inverting analog input.
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply, 3.0V to 5.5V relative to GND2.

2 Specifications

2.1 Absolute Maximum Ratings (1)

Parameter	Description	MIN	MAX	UNIT
Power supply	VDD1 to GND1	-0.3	6.5	V
	VDD2 to GND2	-0.3	6.5	V
Input voltage	INP, INN	GND1-6	VDD1+0.5	V
Output voltage	OUTP, OUTN	GND2-0.5	VDD2+0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Junction temperature, T_J	T_J	-40	150	°C
Storage temperature, T_{stg}	T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 ESD Ratings

Parameter		VALUE	UNIT
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

2.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	MIN	MAX	UNIT
High side power supply	VDD1 to GND1	3.0	5.5	V
Low side power supply	VDD2 to GND2	3.0	5.5	V
Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$	-320	320	mV
Specified linear differential input full-scale		-250	250	mV
Absolute common-mode input voltage (1)	$(V_{INP} + V_{INN})$ / 2 to GND1	-2	VDD1	V
Operating common-mode input voltage		-0.16	VDD1-2.1	
T_A	Ambient Temperature	-40	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the Absolute Maximum Ratings table.

2.4 Thermal Information

Parameter	Description	VALUE	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	85	°C/W
$R_{θJC (top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	43	°C/W

2.5 Insulation Specifications

Parameter	Description	Test Condition	W5R	SR	UNIT
CLR	External clearance	Shortest pin-to-pin distance through air	≥ 8	≥ 4	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	≥ 8	≥ 4	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	≥ 600	V
Material group		According to IEC 60664-1	I	I	
Overvoltage category		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-II	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I	

DIN V VDE V 0884-17 (VDE V 0884-17): 2021-10(2)

Parameter	Description	Test Condition	W5R	UNIT
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	1.2/50 µs waveform per IEC 62368-1 $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
$V_{pd(m)}$	Method a, after Input-Output safety test subgroup 2/3	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	2545	V_{PK}
	Method a, after Input-Output safety test subgroup 1	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	3394	V_{PK}
	Method b1, at routine test (100% production) and preconditioning (type test) (4)	Method b1: $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s partial discharge ≤ 5pC	3977	V_{PK}
C_{IO}	Barrier capacitance, input to output (5)	$V_{IO} = 0.4*\sin(2\pi ft)$, f =1MHz	~1.2	pF
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	Ω
		V_{IO} = 500V at T_S =150°C	$> 10^{9}$	Ω
Pollution degree			2	
Climatic category			40/125/21	

Parameter	Description	Test Condition	SR	UNIT
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	4243	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	1.2/50 µs waveform per IEC 62368-1 $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	5000	V_{PK}
$V_{pd(m)}$	Method a, after Input-Output safety test subgroup 2/3	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	1697	V_{PK}
	Method a, after Input-Output safety test subgroup 1	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	1838	V_{PK}
	Method b1, at routine test (100% production) and preconditioning (type test) (4)	Method b1: $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s partial discharge ≤ 5pC	2121	V_{PK}
C_{IO}	Barrier capacitance, input to output (5)	$V_{IO} = 0.4*\sin(2\pi ft)$, f =1MHz	~1.2	pF
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	Ω
		V_{IO} = 500V at T_S =150°C	$> 10^{9}$	Ω
Pollution degree			2	
Climatic category			40/125/21	

UL 1577

Parameter	Description	Test Condition	W5R	SR	UNIT
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

2.6 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon circuit failure.

Parameter	Description	Test Condition	MIN	TYP	MAX	UNIT
I_S	Safety input, output or supply current	$R_{θJA}$=85°C/W, T_J=150°C, T_A =25°C, VDD1=VDD2=5.5V	-	-	294	mA
		$R_{θJA}$=85°C/W, T_J=150°C, T_A=25°C, VDD1=VDD2=3.3V	-	-	445	mA
P_S	Safety input, output or supply power	$R_{θJA}$=85°C/W, T_J=150°C, T_A=25°C			1470	mW
T_S	Maximum Safety temperature				150	°C

Note: The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, $R_{θJA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{θJA} \times P$, where P is the power dissipated in the device. T_J (max) = $T_S = T_A + R_{θJA} \times P_S$, where T_J (max) is the maximum allowed junction temperature.$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high side and low side.

2.7 Electrical Characteristics

Minimum and maximum specifications of the AMC1200SDUBR apply from TA=-40°C to +125°C, VDD1=3.0V to 5.5V, VDD2=3.0V to 5.5V, INP=-250mV to +250mV, and INN=GND1=0V; typical specifications are at TA=25°C, VDD1=5V, and VDD2=3.3V (unless otherwise noted).

Parameter		Test Condition	MIN	TYP	MAX	UNIT
ANALOG INPUT and OUTPUT						
V_{CMov}	Common-mode overvoltage detection level		VDD1-2			V
	Hysteresis of common-mode overvoltage detection level			100		mV
V_{OS}	Input offset voltage (1)	W5R, T_A = 25°C, V_{INP} = V_{INN} = GND1	-0.2	±0.01	0.2	mV
		SR, T_A = 25°C, V_{INP} = V_{INN} = GND1	-0.3	±0.01	0.3	mV
TCV_{OS}	Input offset drift (1)		-0.9	±0.1	0.9	μV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		-85		dB
		f_{IN} =10KHz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		-85		dB
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275kHz		25		pF
C_{IND}	Differential input capacitance	f_{IN} = 275kHz		20		pF
R_{IN}	Single-ended input resistance	INN = GND1		30		kΩ
R_{IND}	Differential input resistance			35		kΩ
I_{IB}	Input bias current	INP = INN =GND1, I_{IB} = (I_{IBP} + I_{IBN}) / 2	-13	-10	-7	uA
I_{IO}	Input offset current			±5		nA
	Normal gain			8		V/V
E_G	Gain error (1)	W5R, T_A = 25°C, V_{INP} = V_{INN} = GND1	-0.3%	±0.05%	0.3%	
		SR, T_A = 25°C, V_{INP} = V_{INN} = GND1	-0.5%	±0.05%	0.5%	
TCE_G	Gain error drift (1)		-30	±5	30	ppm/°C
NL	Nonlinearity (1)		-0.03%	±0.01%	0.03%	
TC_{NL}	Nonlinearity drift			±1.5		ppm/°C
THD	Total harmonic distortion	V_{IN} = 0.5V, f_{IN} = 10kHz, BW = 100kHz		-88		dB
$NOISE_{OUT}$	Output noise	V_{INP} = V_{INN} = GND1, BW = 100kHz		280		uV_{RMS}
SNR	Signal-to-noise ratio	V_{IN} = 0.5V, f_{IN} = 1kHz, BW = 10kHz		86		dB
		V_{IN} = 0.5V, f_{IN} = 10kHz, BW = 100kHz		77		dB
PSRR		PSRR vs VDD1, at DC		-100		dB

Parameter		Test Condition	MIN	TYP	MAX	UNIT
ANALOG INPUT and OUTPUT						
	Power-supply rejection ratio (2)	PSRR vs VDD1, 100mV and 10kHz ripple		-100		
		PSRR vs VDD2, at DC		-110		
		PSRR vs VDD2, 100mV and 10kHz ripple		-100		
V_{CMout}	Common-mode output voltage		1.40	1.44	1.49	V
$V_{FAILSAFE}$	Failsafe differential output voltage			-2.6	-2.5	V
BW	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		0.2		Ω
I_{SC}	Output short-circuit current			±13		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1kV	100	150		kV/us
POWER SUPPLY						
$VDD1_{UVLO}$	VDD1 undervoltage detection threshold voltage	VDD1 Rising	2.3	2.5	2.7	V
	VDD1 undervoltage hysteresis	Hysteresis		0.15		V
$VDD2_{UVLO}$	VDD2 undervoltage detection threshold voltage	VDD2 Rising	2.2	2.4	2.6	V
	VDD2 undervoltage hysteresis	Hysteresis		0.35		V
IDD1	High-side supply current	3.0V ≤ VDD1 ≤ 5.5V		4	6	mA
IDD2	Low-side supply current	3.0V ≤ VDD2 ≤ 5.5V		3	5	mA

(1) The typical value includes one sigma statistical variation.

(2) This parameter is output referred.

2.8 Switching Characteristics

over operating ambient temperature range (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN	See Fig2		1.0		us
t_f	Fall time of OUTP, OUTN	See Fig2		1.0		us
t_{PD}	INP, INN to OUTP, OUTN signal delay (50% – 50%)	unfiltered output, see Fig2		1.2	1.5	us
	INP, INN to OUTP, OUTN signal delay (50% – 10%)	unfiltered output, see Fig2		0.7	1	us
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	unfiltered output, see Fig2		1.7	2	us
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0V, to OUTP, OUTN valid, 0.1% settling		350		us

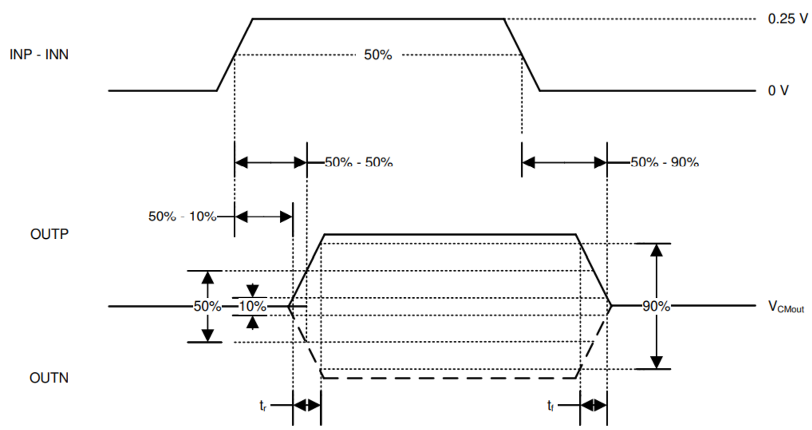


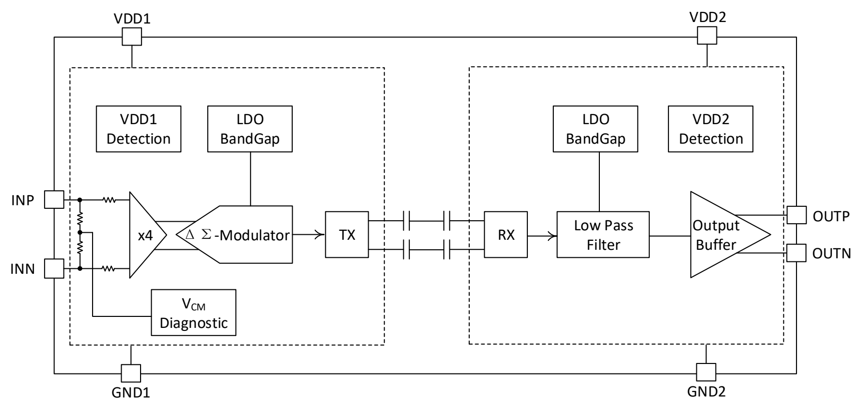
Figure 2. Rise, Fall, and Delay Time Waveforms

3 Detailed Description
3.1 Overview

The AMC1200SDUBR is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator generates data pulse. The drivers (called TX in the Functional Block Diagram) transfer the data pulse of the modulator across the isolation barrier. The received data pulse is synchronized and processed, as shown in the Functional Block Diagram, by a low pass filter and out buffer on the low-side and presented as a differential output of the device.

AMC1200SDUBR adopts single channel transfer architecture and saves one clock channel, compared with current other amplifiers products, AMC1200SDUBR has the lowest power consumption.

3.2 Function block diagram



3.3 Feature Description
3.3.1 Analog Input

The differential amplifier input stage of the AMC1200SDUBR feeds a second order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 35kΩ. The modulator converts the analog signal into data pulse that is transferred across the isolation barrier.

There are two restrictions on the analog input signals (VINP and VINN). First, if the input voltage exceeds the range GND1-6V to VDD1+0.5V, the input current must be limited to 10mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

3.3.2 Failsafe Output

The AMC1200SDUBR offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1200SDUBR is missing.
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN})/2$, exceeds the minimum common-mode overvoltage detection level V_{CMov} of VDD1–2V.

4 Application and Implementation

4.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the AMC1200SDUBR a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required.

4.2 Typical Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the AMC1200SDUBR is optimized for use with low-value shunt resistors in current sensing applications.

Figure 3 depicts a typical operation of the AMC1200SDUBR for current sensing in a frequency inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1200SDUBR ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive). The high impedance input and wide input voltage range make the AMC1200SDUBR suitable for DC bus voltage sensing.

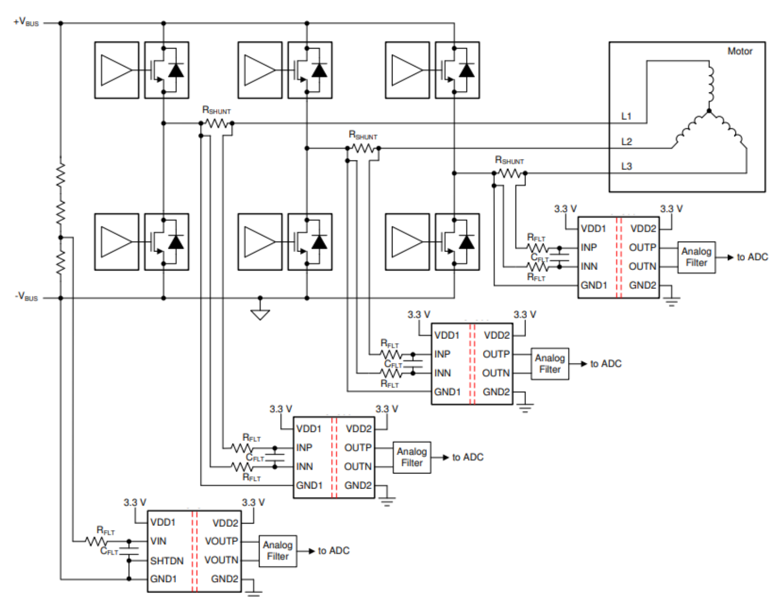


Figure 3. Using the AMC1200SDUBR for Current Sensing in Frequency Inverters

4.2.1 Design Requirements

Table1 lists the parameters for this typical application.

Table1 Design Requirement

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage-drop across the shunt for a linear response	± 250mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	2µs (maximum)

4.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1200SDUBR is derived from the power supply of the upper gate driver. Further details are provided in the Power Supply Recommendations section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1200SDUBR (INN). If a four-pin shunt is used, the inputs of the AMC1200SDUBR device are connected to the inner leads and GND1 is connected to one of the outer shunt-leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

• The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250mV$

• The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

For system using single-ended input ADC, Figure 4 shows an example of an amplifier-based signal conversion and filter circuit as used for recommended example. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

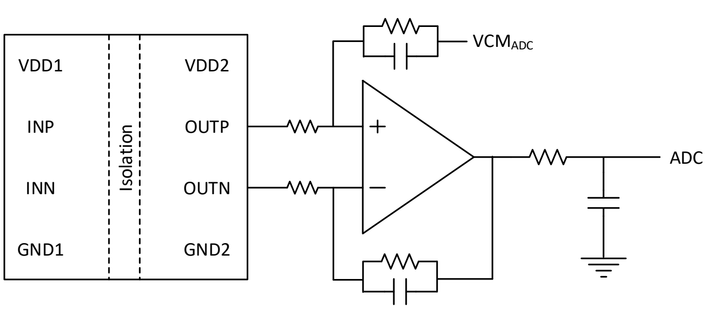


Figure 4. Connecting the AMC1200SDUBR Output to a Single-Ended Input ADC

4.3 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5V or 3.3V ± 10%. Alternatively, a low-cost low-dropout (LDO) regulator may be used to minimize noise on the power supply. A low-ESR decoupling capacitor 0.1 µF to filter this power-supply path is recommended. Place this capacitor (C2 in Figure 5) as close as possible to the VDD1 pin of the AMC1200SDUBR for best performance. If better filtering is required, an additional 2.2 µF capacitor may be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt. To decouple the low-side power supply on the controller side, use a 0.1 µF capacitor placed as close to the VDD2 pin of the AMC1200SDUBR as possible, followed by an additional capacitor from 1
µF to 10 µF.

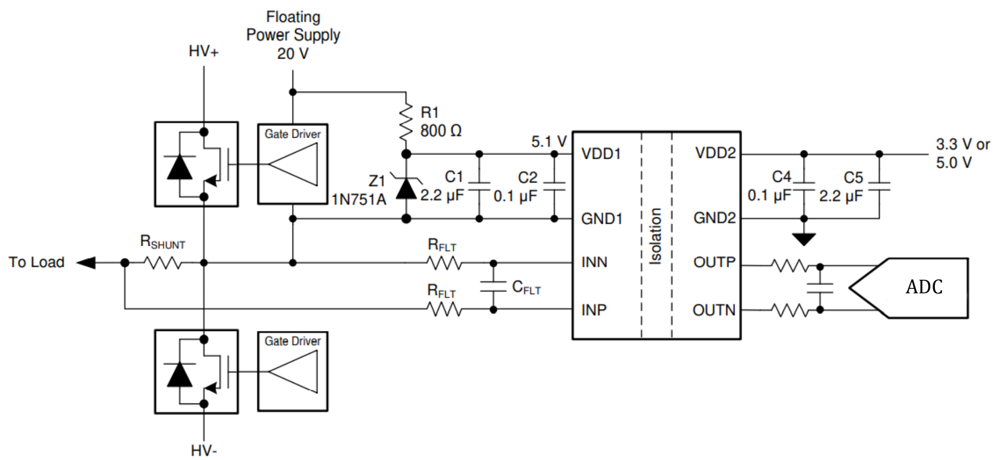


Figure 5. Zener-Diode-Based, High-Side Power Supply

4.4 Layout

Figure 6 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1200SDUBR supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1200SDUBR and keep the layout of both connections symmetrical.

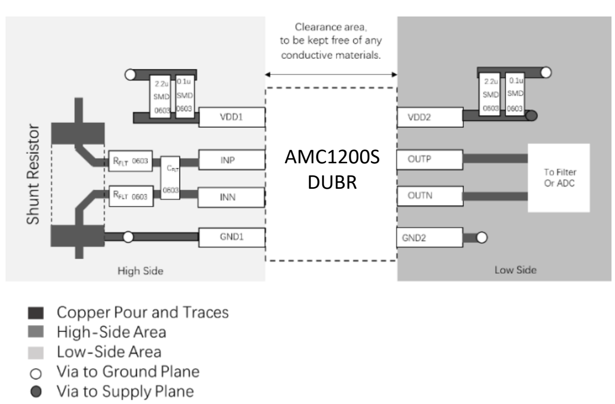


Figure 6. Recommended Layout of the AMC1200SDUBR

5 Outline Dimensions

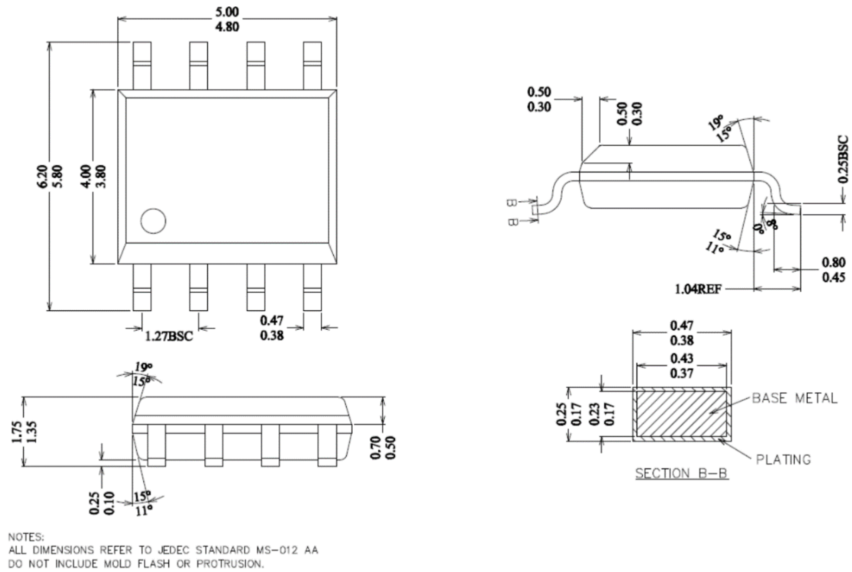


Figure 7. 8-Lead Narrow Body SOIC [NB SOIC-8] Outline Package

6 Land Patterns

The Figure 7 illustrates the recommended land pattern details for the AMC1200SDUBR in a wide-body SOIC-8 package.

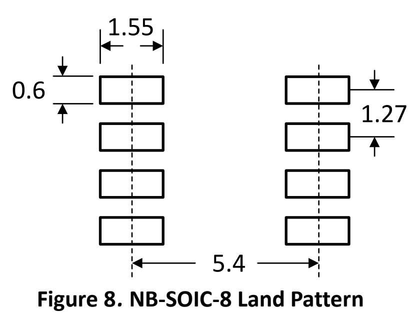


Figure 8. NB-SOIC-8 Land Pattern

Note: All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

7 Reel Information

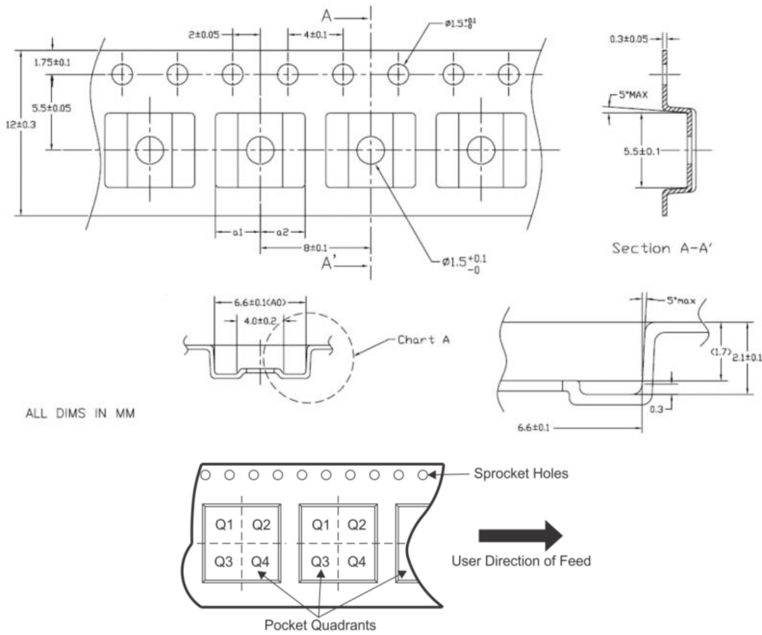


Figure 9. NB-SOIC-8 Reel Information

Note: The Pin 1 of the chip is in the quadrant Q1.

8 Ordering Guide

Model Name	Temperature Range	Withstand Voltage Rating (kV_{RMS})	Package	MSL Peak Temp[1]	Quantity per Reel
AMC1200SDUBR	−40~125°C	3.0	NB SOIC-8	Level-3-260C-168 HR	4000

(1) The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.