MAXINMICRO ELECTRONICS

MX10T03EHP

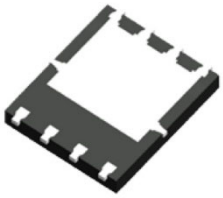
100V N-Channel Power MOSFET

Product Summary

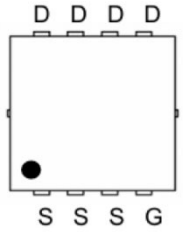
V_{DS}	$R_{DS(ON)\_TYP}$	I_{D_MAX}
100V	3.2 mΩ @VGS = 10V	135A

PDFN5060-8L

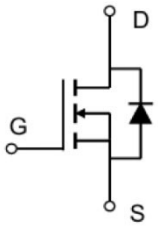
Top View



Bottom View



PIN Configuration
(Top View)



Schematic Diagram

Features

♦Low On-Resistance

♦Excellent FoM (figure of merit)

♦100% ΔVDS & UIS & Rg Tested

Applications

♦Motor controls

♦DC/DC in Telecoms and Inductrial

♦High frequency switching, synchronous rectification

Mechanical Data

♦Green Molding Compound

♦Moisture Sensitivity: Level 3 per J-STD-020

♦UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
MX10T03EHP	PDFN5060-8L	10T03EH	13" Tape&Reel	5,000

Maximum Ratings (@ TC = 25°C, unless otherwise specified.)

Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	100	V
Gate - Source Voltage		V_{GS}	±20	V
Continuous Drain Current (V_{GS} = 10V) (1)	T_C = 25℃	I_D	135	A
	T_C = 100℃		85	
Pulsed Drain Current (2)		I_{DM}	539	A
Single Pulse Avalanche Energy (3)		E_{AS}	640	mJ
Single Pulse Avalanche Current (L= 0.1mH)		I_{AS}	72	A
Power Dissipation	T_C = 25℃	P_D	125	W
	T_C = 100℃		50	
Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ +150	℃

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient (4)	$R_{\theta JA}$	35	43	℃/W
Thermal Resistance, Junction-to-Case (5)	$R_{\theta JC}$	0.8	1.0	℃/W

Electrical Characteristics (@ TJ = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics (6)						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100			A
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V T_J = 25℃			1.0	μA
		V_{DS} = 100V, V_{GS} = 0V T_J = 125℃			100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} =0V			±100	nA
On Characteristics (6)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		3.2	3.8	mΩ
Forward Transconductance	g_{fs}	V_{DS} = 5.0V, I_D = 20A		46		S
Diodes Forward Voltage	V_{SD}	I_S = 2.0A, V_{GS} = 0V		0.7	1.2	V
Dynamic Characteristics (7)						
Input Capacitance	C_{iss}	V_{DS} = 50V, V_{GS} = 0V, f= 1MHz		4799		pF
Output Capacitance	C_{oss}			1256		pF
Reverse Transfer Capacitance	C_{rss}			50		pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS}=0V, f =1MHz		1.7		Ω
Switching Characteristics (7)						
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 50V I_D = 20A, R_{GEN} = 3.0 Ω		10		ns
Rise Time	t_r			17		ns
Turn-Off DelayTime	$t_{d(off)}$			44		ns
Fall Time	t_f			23		ns
Gate Charge Characteristics (7)						
Total Gate Charge (V_{GS} = 10V)	Q_g	V_{DS} = 50V, I_D = 20A V_{GS} = 10V		68		nC
Total Gate Charge (V_{GS} = 6.0V)	Q_g			44		nC
Gate-Source Charge	Q_{gs}			19		nC
Gate-Drain Charge	Q_{gd}			15		nC
Gate Plateau Voltage	$V_{plateau}$			4.3		V
Drain-Source Diode Characteristics (7)						
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20A, dI/dt = 100A/ μ s, T_J = 25℃		62		ns
Body Diode Reverse Recovery Charge	Q_{rr}			130		nC
Diode Forward Current	I_S	T_C = 25℃			135	A

Notes:

1. This current is chip limited, which is calculated based on Rthjc.
2. This current is calculated on single pulse with 10us Single Pulse.
3. Defined by design, not subject to production test, EAs condition: T_J=25°C, V_{DD}50V, V_{GS}=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

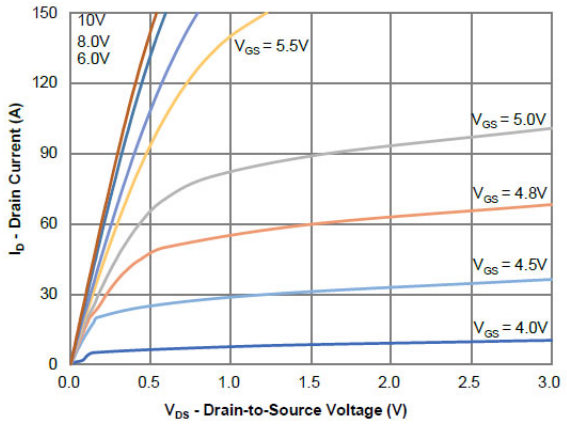


Figure 1: Output Characteristics

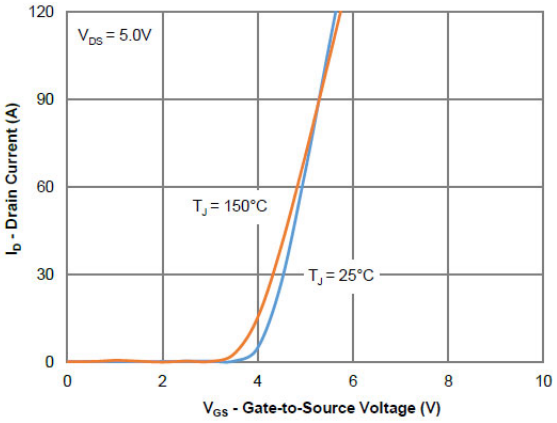


Figure 2: Transfer Characteristics

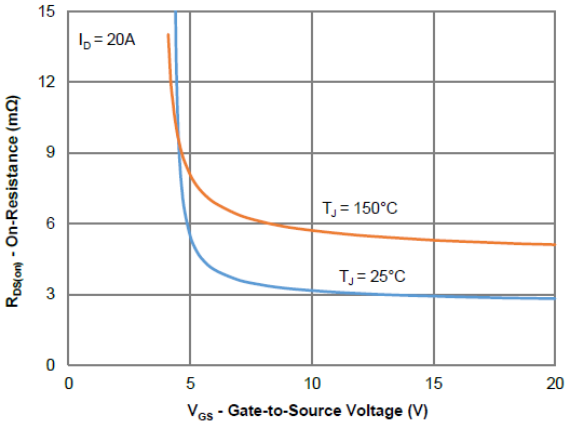


Figure 3: On-Resistance vs. Gate-Source Voltage

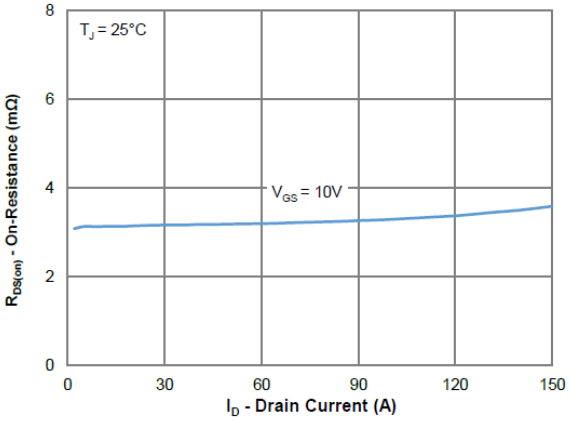


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

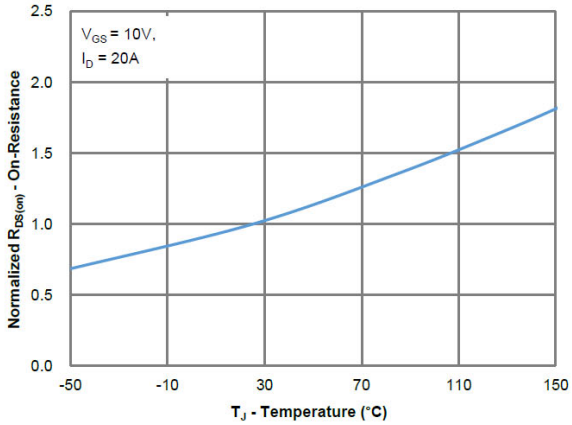


Figure 5: On-Resistance vs. Junction Temperature

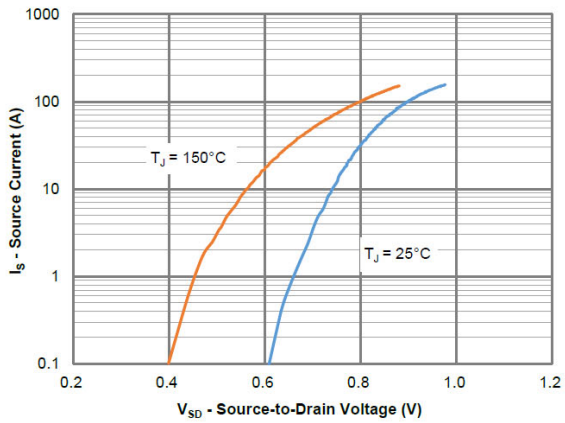


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

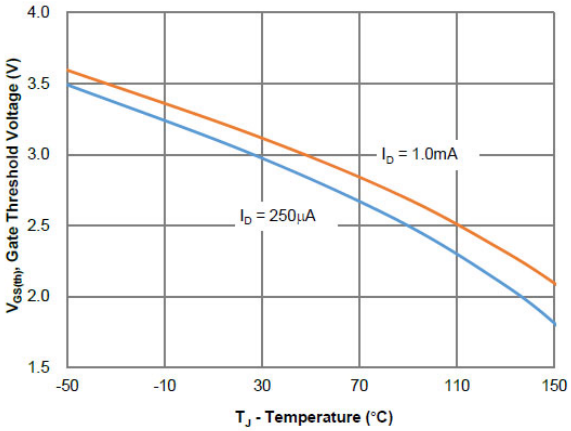


Figure 7: Gate Threshold Variation vs. Junction Temperature

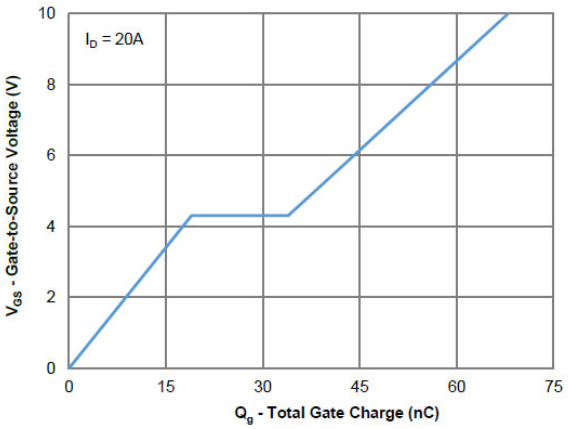


Figure 8: Gate Charge Characteristics

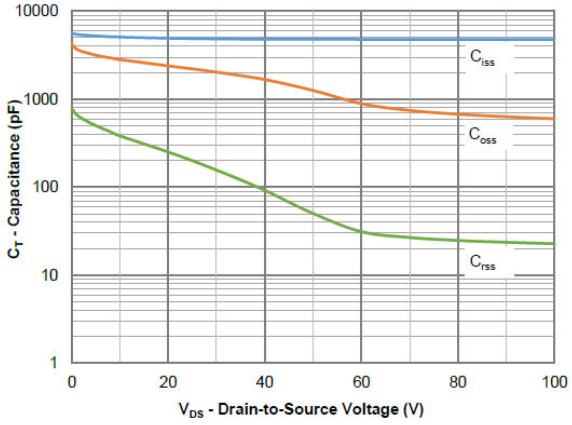


Figure 9: Capacitance Characteristics

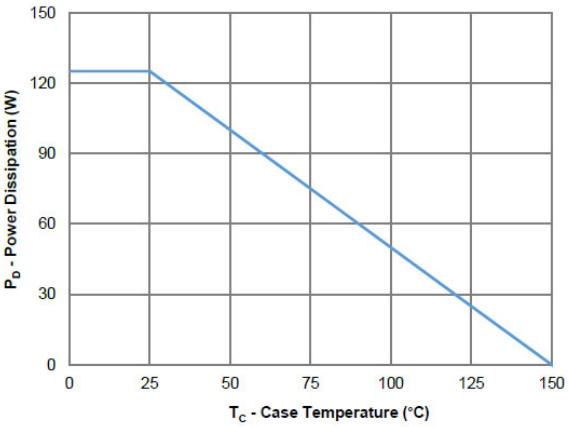


Figure 10: Power Derating

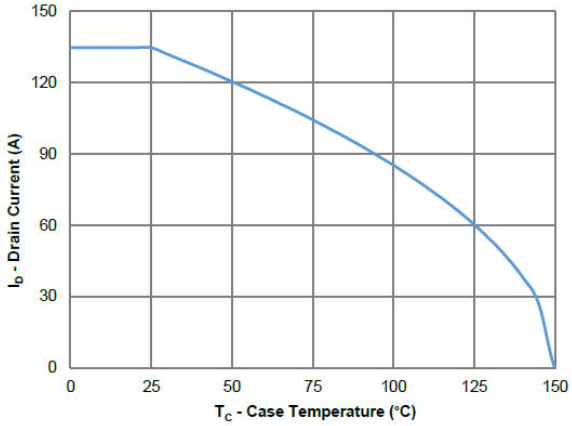


Figure 11: Current Derating

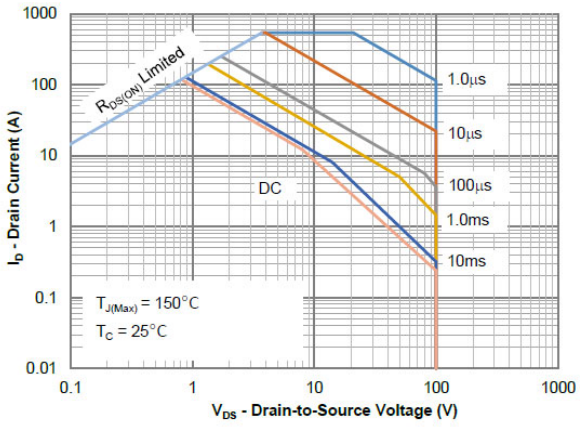


Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

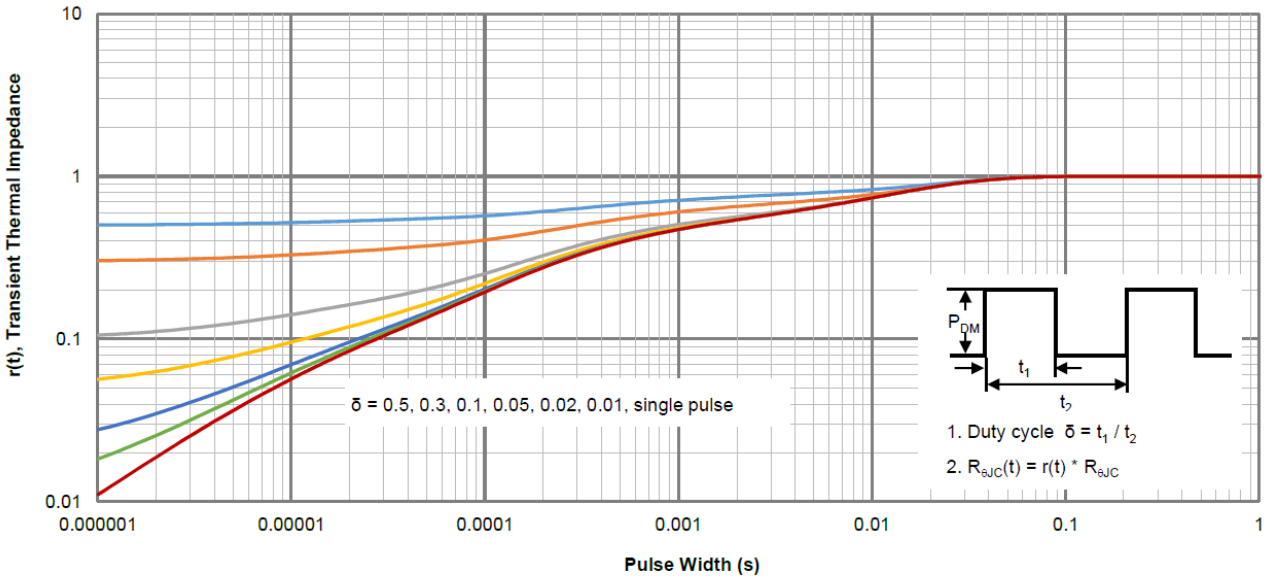
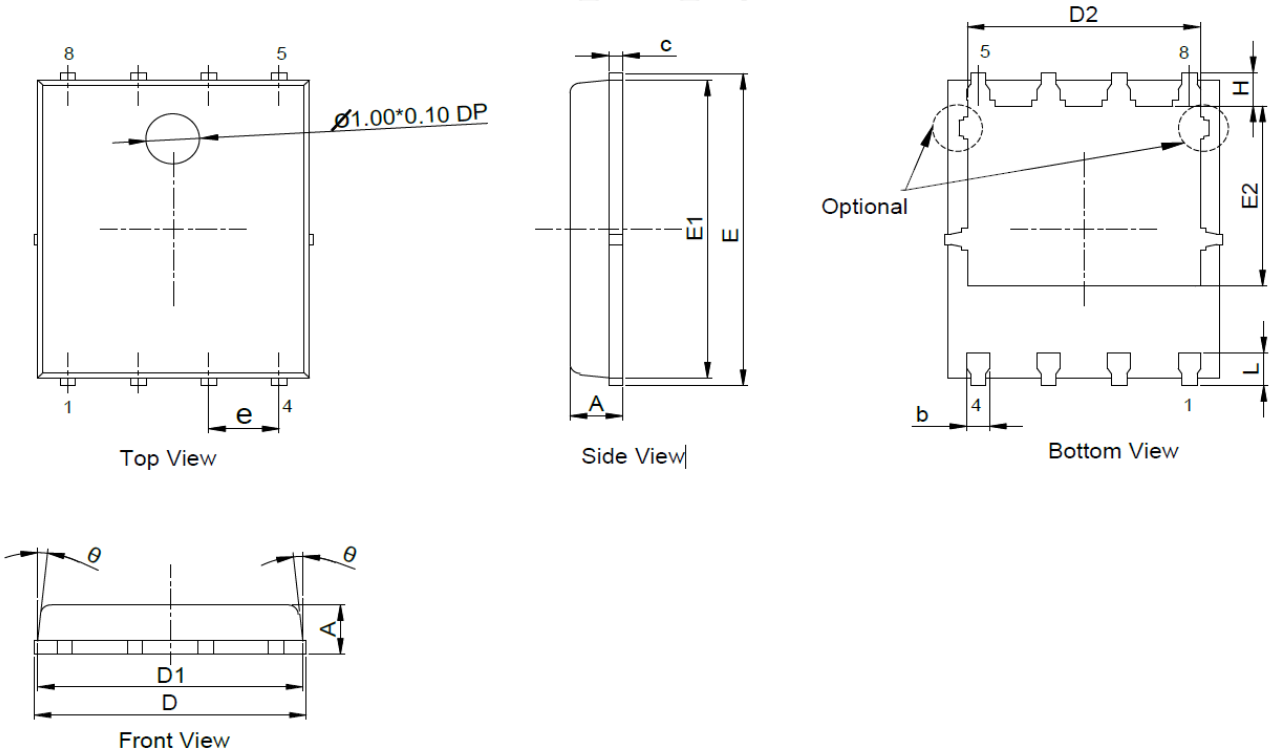


Figure 13: Normalized Maximum Transient Thermal Impedance

PDFN5060-8L Package Outline

Package Outline

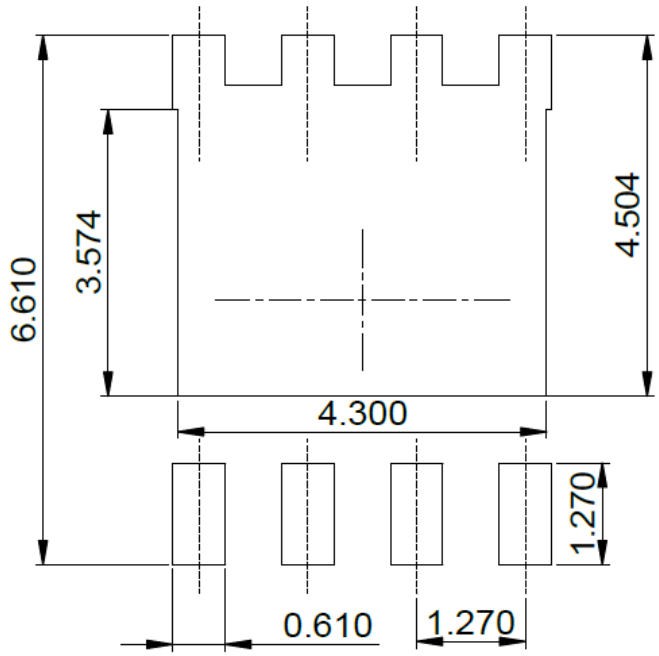


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
B	0.20	0.41	0.51
c			
D	4.80	--	5.40
D1	4.65	--	5.30
D2	3.60	--	4.30
E	5.90	--	6.30
E1	5.60	--	6.00
E2	3.37	--	3.92
e	1.27BSC		
H	0.40	0.60	0.75
L	0.40	0.60	0.84
θ	0°	--	12°

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS