



## U74HC595A

CMOS IC

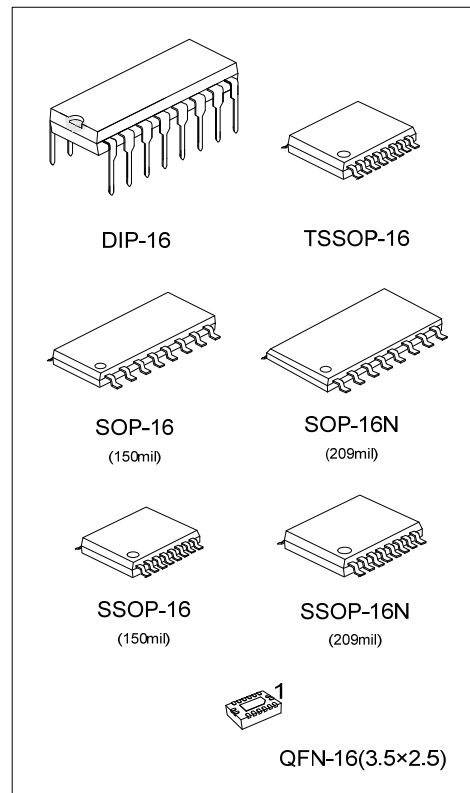
### 8-BIT SERIAL-IN SHIFT REGISTER WITH LATCHED 3-STATE PARALLEL OUTPUTS, PROVIDING SERIAL OUTPUT

#### DESCRIPTION

The UTC **U74HC595A** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output. The Serial Data Input (SER) will shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

#### FEATURES

- \* Operation Voltage Range: 2V ~ 6V
- \* High Noise Immunity
- \* Output Compatibility with CMOS and TTL
- \* Specified from -40°C ~ +125°C

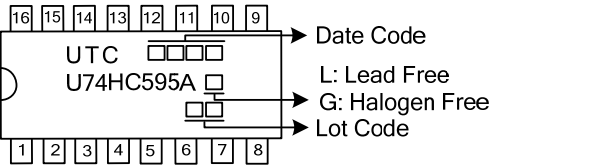
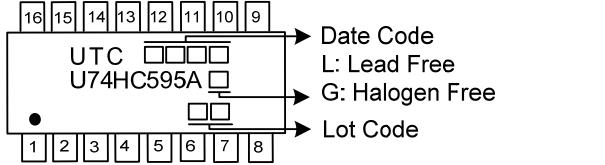
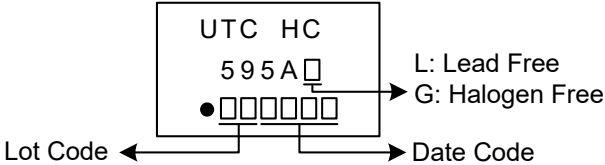


#### ORDERING INFORMATION

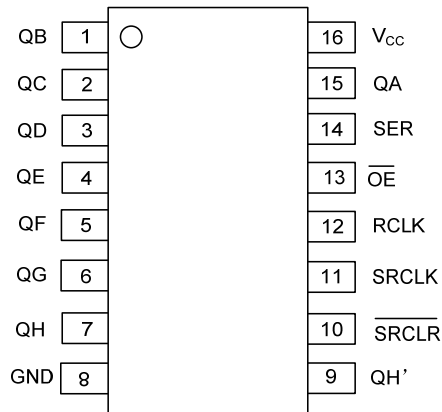
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC595AL-D16-T	U74HC595AG-D16-T	DIP-16	Tube
U74HC595AL-S16-R	U74HC595AG-S16-R	SOP-16	Tape Reel
U74HC595AL-S16N-R	U74HC595AG-S16N-R	SOP-16N	Tape Reel
U74HC595AL-R16-R	U74HC595AG-R16-R	SSOP-16	Tape Reel
U74HC595AL-R16N-R	U74HC595AG-R16N-R	SSOP-16N	Tape Reel
U74HC595AL-P16-R	U74HC595AG-P16-R	TSSOP-16	Tape Reel
U74HC595AL-QAH-R	U74HC595AG-QAH-R	QFN-16(3.5x2.5)	Tape Reel

<p>U74HC595AG-D16-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D16: DIP-16, S16: SOP-16, S16N: SOP-16N R16: SSOP-16, R16N: SSOP-16N P16: TSSOP-16, QAH: QFN-16(3.5x2.5) (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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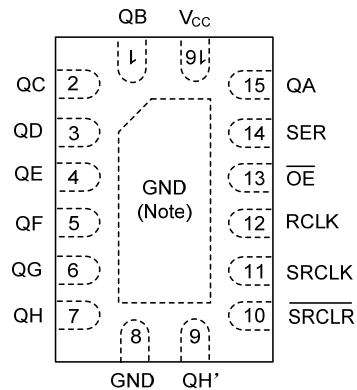
■ MARKING

PACKAGE	MARKING
DIP-16	 <p>Diagram showing a DIP-16 package with pins 1-16. Marking includes: UTC, U74HC595A, and a date code (□□□□). Legend: L: Lead Free, G: Halogen Free. Lot Code is indicated by a square symbol.</p>
SOP-16 / SOP-16N SSOP-16 SSOP-16N / TSSOP-16	 <p>Diagram showing a SOP-16 package with pins 1-16. Marking includes: UTC, U74HC595A, and a date code (□□□□). Legend: L: Lead Free, G: Halogen Free. Lot Code is indicated by a square symbol.</p>
QFN-16(3.5×2.5)	 <p>Diagram showing a QFN-16 package. Marking includes: UTC HC, 595A, and a date code (□□□□□□). Legend: L: Lead Free, G: Halogen Free. Lot Code is indicated by a square symbol.</p>

■ PIN CONFIGURATION



DIP-16 / SOP-16 / SOP-16N  
SSOP-16 / SSOP-16N / TSSOP-16



Note: Connect exposed pad to GND

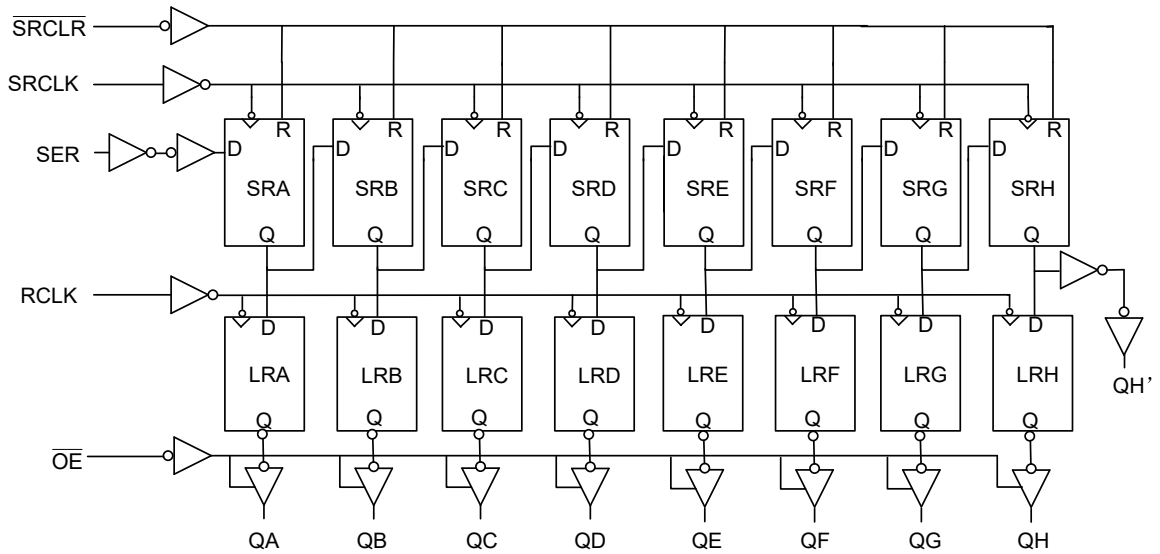
QFN-16(3.5x2.5)  
(TOP VIEW)

■ FUNCTION TABLE

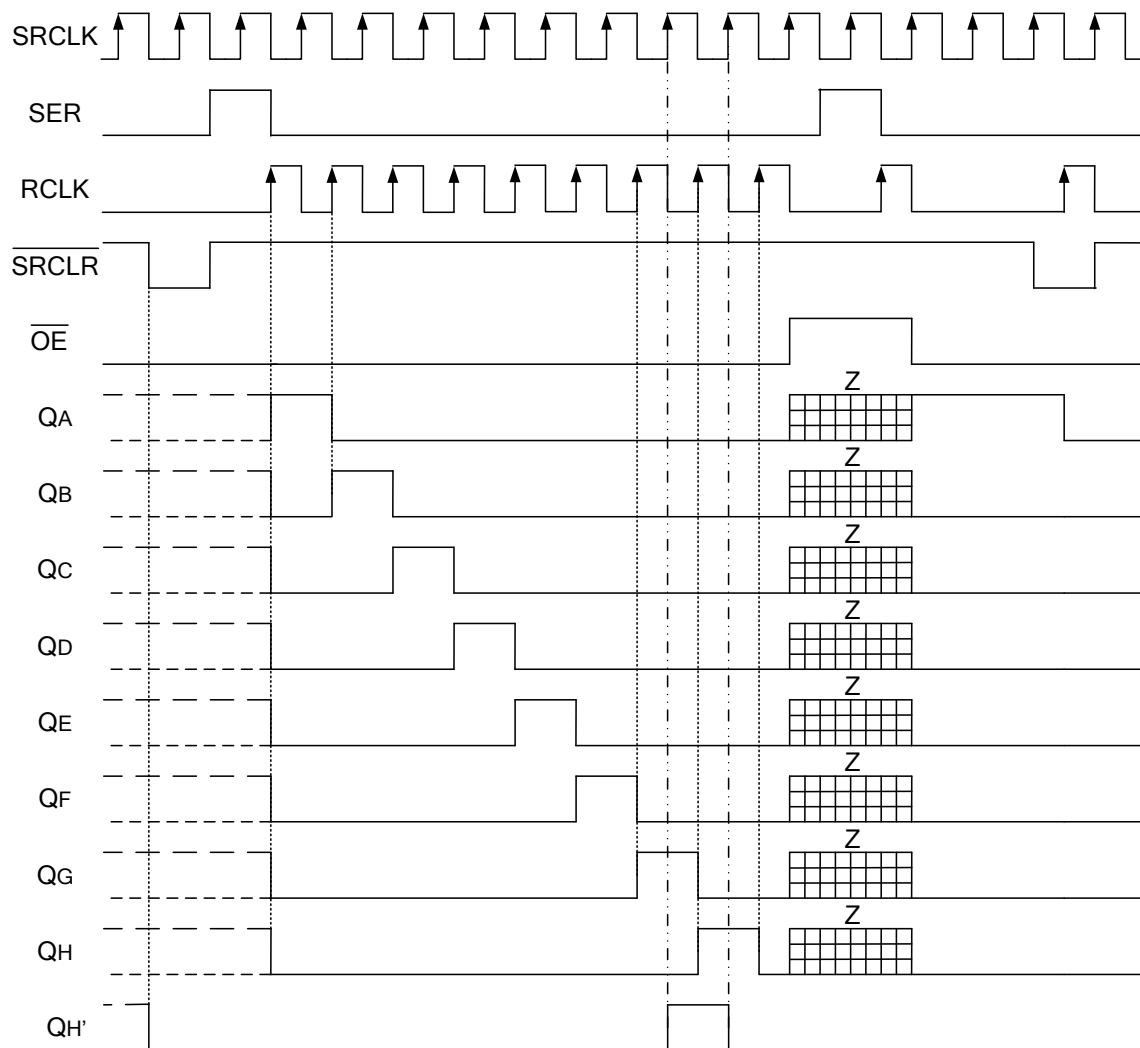
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	OE	SRCLR	SER	QH'	Qn
A Low-Level on $\overline{\text{SRCLR}}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note: H : HIGH voltage level.  
 L : LOW voltage level.  
 X : Don't care.  
 Z : High impedance OFF-state.  
 NC: No change.  
 ↑ : Low-to-High transition.  
 ↓ : High-to-Low transition.

■ LOGIC DIAGRAM



■ TIMING DIAGRAM



### ■ ABSOLUTE MAXIMUM RATING (Note 1)

PARAMETER		SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage		$V_{CC}$		-0.5~7.0	V
Input Clamp Current (Note 2)		$I_{IK}$	$V_{IN}<0$ or $V_{IN}>V_{CC}$	$\pm 20$	mA
Output Clamp Current (Note 2)		$I_{OK}$	$V_{OUT}<0$ or $V_{OUT}>V_{CC}$	$\pm 20$	mA
Output Current		$I_{OUT}$	$V_{OUT}=0$ to $V_{CC}$	$\pm 35$	mA
$V_{CC}$ or GND Current		$I_{CC}$		$\pm 75$	mA
Power Dissipation	DIP-16	$P_D$		750	mW
	SOP-16			500	mW
	SOP-16N			550	mW
	SSOP-16			450	mW
	SSOP-16N				
	TSSOP-16				
QFN-16(3.5×2.5)				500	mW
Storage Temperature		$T_{STG}$		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### ■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$		2		6	V
Input Voltage	$V_{IN}$		0		$V_{CC}$	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
Operating Temperature	$T_A$		-40		+125	°C
Input Transition Rise or Fall Time	$t_R / t_F$	$V_{CC}=2V$			100	ns
		$V_{CC}=4.5V$			20	ns
		$V_{CC}=6V$			20	ns

### ■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub> =25°C			T <sub>A</sub> =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V <sub>IH</sub>	V <sub>CC</sub> =2V	1.5			1.5			V
		V <sub>CC</sub> =3V	2.1			2.1			V
		V <sub>CC</sub> =4.5V	3.15			3.15			V
		V <sub>CC</sub> =6V	4.2			4.2			V
Low-Level Input Voltage	V <sub>IL</sub>	V <sub>CC</sub> =2V			0.5			0.5	V
		V <sub>CC</sub> =3V			0.9			0.9	V
		V <sub>CC</sub> =4.5V			1.35			1.35	V
		V <sub>CC</sub> =6V			1.8			1.8	V
High-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>OH</sub>	V <sub>CC</sub> =2V, I <sub>OH</sub> =-20μA	1.9	2.0		1.9			V
		V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-20μA	4.4	4.5		4.4			V
		V <sub>CC</sub> =6V, I <sub>OH</sub> =-20μA	5.9	6.0		5.9			V
		V <sub>CC</sub> =3V, I <sub>OH</sub> =-2.4mA	2.48			2.3			V
		V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-6mA	3.98			3.7			V
		V <sub>CC</sub> =6V, I <sub>OH</sub> =-7.8mA	5.48			5.2			V
Low-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>OL</sub>	V <sub>CC</sub> =2V, I <sub>OL</sub> =20μA		0.002	0.1			0.1	V
		V <sub>CC</sub> =4.5V, I <sub>OL</sub> =20μA		0.001	0.1			0.1	V
		V <sub>CC</sub> =6V, I <sub>OL</sub> =20μA		0.001	0.1			0.1	V
		V <sub>CC</sub> =3V, I <sub>OL</sub> =2.4mA			0.26			0.4	V
		V <sub>CC</sub> =4.5V, I <sub>OL</sub> =6mA			0.26			0.4	V
		V <sub>CC</sub> =6V, I <sub>OL</sub> =7.8mA			0.26			0.4	V
High-Level Output Voltage, Q <sub>H</sub> '	V <sub>OH</sub>	V <sub>CC</sub> =2V, I <sub>OH</sub> =-20μA	1.9	2.0		1.9			V
		V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-20μA	4.4	4.5		4.4			V
		V <sub>CC</sub> =6V, I <sub>OH</sub> =-20μA	5.9	6.0		5.9			V
		V <sub>CC</sub> =3V, I <sub>OH</sub> =-2.4mA	2.48			2.3			V
		V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-4mA	3.98			3.7			V
		V <sub>CC</sub> =6V, I <sub>OH</sub> =-5.2mA	5.48			5.2			V
Low-Level Output Voltage, Q <sub>H</sub> '	V <sub>OL</sub>	V <sub>CC</sub> =2V, I <sub>OL</sub> =20μA		0.002	0.1			0.1	V
		V <sub>CC</sub> =4.5V, I <sub>OL</sub> =20μA		0.001	0.1			0.1	V
		V <sub>CC</sub> =6V, I <sub>OL</sub> =20μA		0.001	0.1			0.1	V
		V <sub>CC</sub> =3V, I <sub>OL</sub> =2.4mA			0.26			0.4	V
		V <sub>CC</sub> =4.5V, I <sub>OL</sub> =4mA			0.26			0.4	V
		V <sub>CC</sub> =6V, I <sub>OL</sub> =5.2mA			0.26			0.4	V
Input Leakage Current	I <sub>I(LEAK)</sub>	V <sub>CC</sub> =6V, V <sub>IN</sub> =V <sub>CC</sub> or GND			±0.1			±1	μA
Output Off-State Current	I <sub>OZ</sub>	V <sub>CC</sub> =6V, V <sub>OUT</sub> =V <sub>CC</sub> or GND			±0.5			±10	μA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>CC</sub> =6V, V <sub>IN</sub> =V <sub>CC</sub> or GND, I <sub>OUT</sub> =0			8			160	μA

## ■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub> =25°C			T <sub>A</sub> =-40°C~+125°C			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
Maximum Clock Pulse Frequency	f <sub>max</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V	6	26		4		MHz	
			V <sub>CC</sub> =4.5V	30	38		20		MHz	
			V <sub>CC</sub> =6V	35	42		24		MHz	
Propagation Delay From Input (SRCLK) to Output (Q <sub>H</sub> )	t <sub>PD</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		50	140			265	ns
			V <sub>CC</sub> =4.5V		17	28			53	ns
			V <sub>CC</sub> =6V		14	24			45	ns
Propagation Delay From Input (RCLK) to Output (Q <sub>A</sub> -Q <sub>H</sub> )	t <sub>PD</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		50	140			265	ns
			V <sub>CC</sub> =4.5V		17	28			53	ns
			V <sub>CC</sub> =6V		14	24			45	ns
	C <sub>L</sub> =150pF	V <sub>CC</sub> =2V		60	200			250	ns	
		V <sub>CC</sub> =4.5V		22	40			50	ns	
		V <sub>CC</sub> =6V		19	34			43	ns	
Propagation Delay From Input ( $\overline{\text{SRCLK}}$ ) to Output (Q <sub>H</sub> )	t <sub>PHL</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		51	145			265	ns
			V <sub>CC</sub> =4.5V		18	29			53	ns
			V <sub>CC</sub> =6V		15	25			45	ns
Propagation Delay From Input (OE) to Output (Q <sub>A</sub> -Q <sub>H</sub> )	t <sub>en</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		40	135			225	ns
			V <sub>CC</sub> =4.5V		15	27			45	ns
			V <sub>CC</sub> =6V		13	23			38	ns
	C <sub>L</sub> =150pF	V <sub>CC</sub> =2V		70	200			250	ns	
		V <sub>CC</sub> =4.5V		23	40			50	ns	
		V <sub>CC</sub> =6V		19	34			43	ns	
Propagation Delay From Input ( $\overline{\text{OE}}$ ) to Output (Q <sub>A</sub> -Q <sub>H</sub> )	t <sub>dis</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		42	150			250	ns
			V <sub>CC</sub> =4.5V		23	30			50	ns
			V <sub>CC</sub> =6V		20	26			43	ns
Output Transition Time (Q <sub>A</sub> -Q <sub>H</sub> )	t <sub>t</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		28	60			75	ns
			V <sub>CC</sub> =4.5V		8	12			15	ns
			V <sub>CC</sub> =6V		6	10			13	ns
	C <sub>L</sub> =150pF	V <sub>CC</sub> =2V		45	210			265	ns	
		V <sub>CC</sub> =4.5V		17	42			53	ns	
		V <sub>CC</sub> =6V		13	36			45	ns	
Output Transition Time (Q <sub>H</sub> )	t <sub>t</sub>	C <sub>L</sub> =50pF	V <sub>CC</sub> =2V		28	75			95	ns
			V <sub>CC</sub> =4.5V		8	15			19	ns
			V <sub>CC</sub> =6V		6	13			16	ns

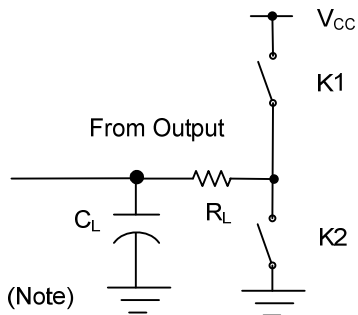
### ■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub> =25°C			T <sub>A</sub> =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse Duration, SRCLK or RCLK High or Low	t <sub>w</sub>	V <sub>CC</sub> =2V	80			110			ns
		V <sub>CC</sub> =4.5V	16			22			ns
		V <sub>CC</sub> =6V	14			19			ns
Pulse Duration, SRCLR Low		V <sub>CC</sub> =2V	80			110			ns
		V <sub>CC</sub> =4.5V	16			22			ns
		V <sub>CC</sub> =6V	14			19			ns
Setup Time, SER Before SRCLK↑	t <sub>su</sub>	V <sub>CC</sub> =2V	100			125			ns
		V <sub>CC</sub> =4.5V	20			25			ns
		V <sub>CC</sub> =6V	17			21			ns
Setup Time, SRCLK↑ Before RCLK↑		V <sub>CC</sub> =2V	75			94			ns
		V <sub>CC</sub> =4.5V	15			19			ns
		V <sub>CC</sub> =6V	13			16			ns
Setup Time, SRCLR Low Before RCLK↑		V <sub>CC</sub> =2V	50			65			ns
		V <sub>CC</sub> =4.5V	10			13			ns
		V <sub>CC</sub> =6V	9			11			ns
Setup Time, SRCLR High (inactive) Before SRCLK↑		V <sub>CC</sub> =2V	50			60			ns
		V <sub>CC</sub> =4.5V	10			12			ns
		V <sub>CC</sub> =6V	9			11			ns
Hold Time, SER After SRCLK↑	t <sub>h</sub>	V <sub>CC</sub> =2V	3			3			ns
		V <sub>CC</sub> =4.5V	3			3			ns
		V <sub>CC</sub> =6V	3			3			ns

### ■ OPERATING CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>CC</sub> =6V, V <sub>IN</sub> =V <sub>CC</sub> or GND			10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	No load		400		pF

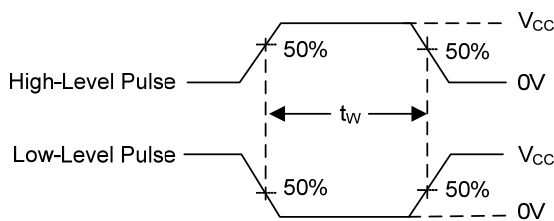
## TEST CIRCUIT AND WAVEFORMS



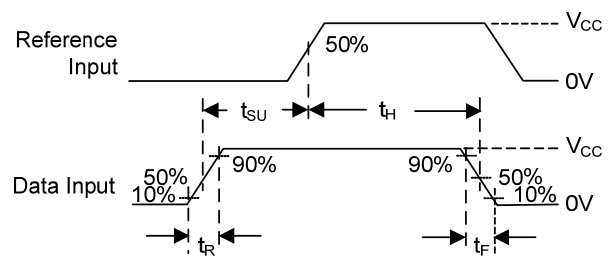
TEST	K1	K2
$t_{PLH}/t_{PHL}$	Open	Open
$t_{PHZ}/t_{PZH}$	Open	Close
$t_{PLZ}/t_{PZL}$	Close	Open

$t_{PD}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

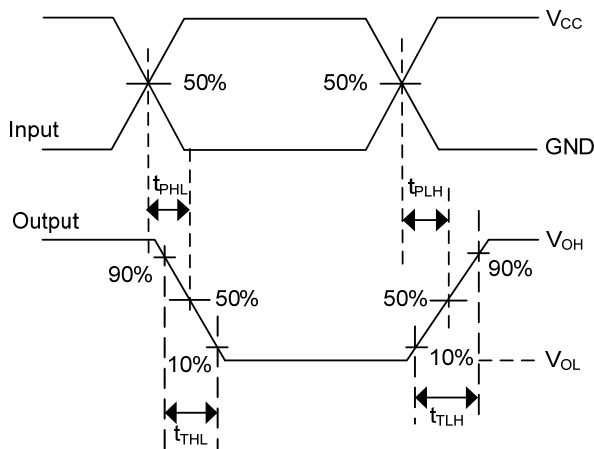
Note:  $C_L$  includes probe and jig capacitance.  $C_L=50pF$  or  $150pF$ ,  $R_L=1K\Omega$



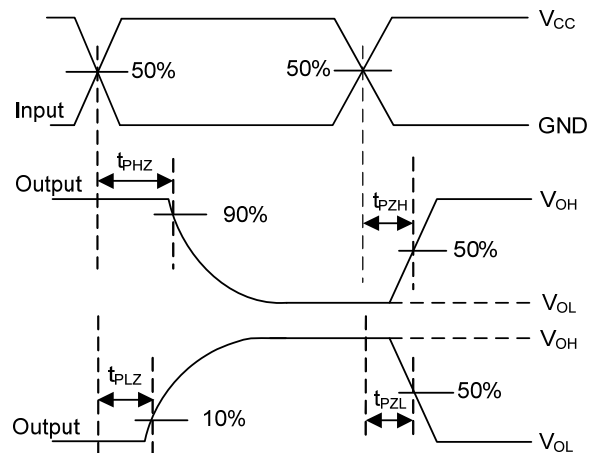
Voltage Waveforms, Pulse Duration



Voltage Waveforms



Voltage Waveforms Propagation Delays



Voltage Waveforms Propagation Delays

Note: All input pulses are supplied by generators having the following characteristics:  
 $P_{RR} \leq 1MHz$ ,  $Z_0 = 50\Omega$ ,  $t_r \leq 3ns$ ,  $t_f \leq 3ns$ .

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