



BK7239N Datasheet

DS-BK7239N-E09 V1.8

2026/1/28

Contents

Contents.....	2
1 Features.....	6
2 Overview.....	12
3 Pin Descriptions	17
3.1 QFN48 Pin Descriptions	17
3.2 BK7239N QFN40 Pin Descriptions.....	20
3.3 BK7239NL QFN40 Pin Descriptions.....	23
3.4 Pin Multiplexing	26
3.4.1 I/O Pin Predefined States at Reset and After Reset.....	27
3.4.2 I/O Matrix.....	28
3.4.3 Pin Multiplexing of Analog Functions.....	31
4 Functional Description	33
4.1 Arm STAR-MC1 Processor.....	33
4.1.1 Nested Vectored Interrupt Controller (NVIC).....	33
4.1.2 Memory Protection Unit (MPU).....	33
4.1.3 Security Attribution Unit (SAU).....	34
4.2 Memory Organization.....	34
4.3 Wi-Fi Subsystem	36
4.3.1 Wi-Fi Baseband	36
4.3.2 Wi-Fi MAC	37
4.3.3 Wi-Fi Radio.....	38
4.4 Bluetooth LE Subsystem	39
4.4.1 Bluetooth LE Features.....	39
4.4.2 Bluetooth Interfaces.....	39
4.5 IEEE 802.15.4 PHY and MAC.....	40
4.6 RF Transceivers.....	41



- 4.7 FEM Support.....41
- 4.8 Clock Management.....41
- 4.9 Reset.....45
- 4.10 Power Management.....45
 - 4.10.1 Power Scheme45
 - 4.10.2 Power Supply Supervisor49
 - 4.10.3 Power Modes49
- 4.11 I/O Multiplexer (IOMUX).....50
- 4.12 General-purpose I/Os (GPIO).....50
- 4.13 SPI Interfaces (SPI).....51
- 4.14 Quad SPI Interface (QSPI).....51
- 4.15 UART Interfaces (UART).....51
- 4.16 SDIO Interface (SDIO).....52
- 4.17 I2C Interfaces (I2C)52
- 4.18 GDMA Controller (GDMA).....53
- 4.19 RGB LED Controller (LED)54
- 4.20 PWM Module (PWM).....54
- 4.21 I2S Interface (I2S).....55
- 4.22 Auxiliary ADC (AUX ADC).....55
- 4.23 Timer Groups (TIMG).....56
- 4.24 Watchdog Timer (WDT).....56
- 4.25 Real-time Counter (RTC).....57
- 4.26 Temperature Sensor.....57
- 4.27 Anti-tamper Module57
- 4.28 Security57
 - 4.28.1 Secure Boot.....58
 - 4.28.2 Secure Debug58
 - 4.28.3 FOTA.....58
 - 4.28.4 Provisioning58
 - 4.28.5 Secure Connection59
 - 4.28.6 BootROM.....59



- 4.28.7 Bootloader.....59
- 4.28.8 TEE_M.....59
- 4.28.9 TrustEngine60
 - 4.28.9.1 Features60
 - 4.28.9.2 Supported Standards and Specifications.....60
 - 4.28.9.3 Components61
- 5 Electrical Characteristics..... 62
 - 5.1 Absolute Maximum Ratings62
 - 5.2 ESD Ratings.....62
 - 5.3 Recommended Operating Conditions63
 - 5.4 Digital I/O Characteristics.....64
 - 5.5 IO LDO.....65
 - 5.6 Analog LDO.....65
 - 5.7 Core LDO65
 - 5.8 EXMEM LDO65
 - 5.9 Analog Buck65
 - 5.10 Brown-out Detector (BOD)66
 - 5.11 40 MHz Crystal Characteristics.....66
 - 5.12 32.768 kHz Crystal Characteristics.....66
 - 5.13 Current Consumption.....67
 - 5.14 RF Characteristics69
 - 5.14.1 WLAN RF Characteristics.....70
 - 5.14.1.1 WLAN 2.4 GHz Receiver Characteristics70
 - 5.14.1.2 WLAN 2.4 GHz Transmitter Characteristics73
 - 5.14.1.3 WLAN 5 GHz Receiver Characteristics74
 - 5.14.1.4 WLAN 5 GHz Transmitter Characteristics77
 - 5.14.2 Bluetooth LE RF Characteristics78
 - 5.14.2.1 Bluetooth LE Receiver Characteristics78
 - 5.14.2.2 Bluetooth LE Transmitter Characteristics81
 - 5.14.3 IEEE 802.15.4 RF Characteristics82



5.14.3.1	IEEE 802.15.4 Receiver Characteristics	82
5.14.3.2	IEEE 802.15.4 Transmitter Characteristics	83
5.15	BK7239N Module Throughput.....	84
5.16	AUX ADC Characteristics.....	84
6	Package Information.....	86
6.1	QFN48 6 x 6 x 0.75 mm Package.....	86
6.2	QFN40 5 x 5 x 0.75 mm Package.....	88
7	Reflow Soldering Profile.....	90
8	Certifications and Compliance.....	92
9	Ordering Information.....	93
	Revision History.....	95

1 Features

Wi-Fi® 6 Dual-band Connectivity

Low power design

- IEEE power save mode: 39 μ A @ DTIM 10
- Active RX: 9 mA (2.4 GHz), 12 mA (5 GHz)
- Deep sleep0: 2.5 μ A

IEEE 802.11ax (Wi-Fi 6)

- 1T1R operation in 2.4 GHz and 5 GHz bands
- 2.4 GHz operating frequency range: 2412–2484 MHz
- 5 GHz operating frequency range: 4900–5925 MHz
- 20 MHz and 40 MHz channel bandwidths
- 20 MHz channel up to MCS9
- Uplink and downlink Orthogonal Frequency Division Multiple Access (OFDMA) for improved efficiency in dense IoT environments
- Downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO) with Beamformee support for higher capacity and better signal quality
- Target Wake Time (iTWT/bTWT) for optimized power saving and reduced collisions
- Spatial reuse and BSS coloring for higher throughput in crowded deployments
- Dual Carrier Modulation (DCM) and SU Extended Range (ER) for robust long range links

IEEE 802.11ac compliant

- 20 MHz and 40 MHz channel bandwidths in 5 GHz band
- Data rates up to 180 Mbps (MCS8, 40 MHz, short GI)
- Downlink MU-MIMO for higher aggregate throughput
- Beamformee support to improve link robustness and signal quality
- High throughput aggregation: TX/RX A-MPDU (Aggregated MAC Protocol Data Unit) and A-MSDU (Aggregated MAC Service Data Unit)
- Block ACK (BA) with immediate response for efficient retransmission
- Frame fragmentation and defragmentation
- Transmission opportunity (TXOP) support for prioritized channel access



- Wi-Fi Multimedia (WMM) for QoS in voice, video, and data traffic

Backward compatibility with IEEE 802.11a/b/g/n

- Fully interoperable with legacy Wi-Fi standards in both 2.4 GHz and 5 GHz bands
- 20 MHz and 40 MHz channel bandwidths (HT20/HT40)
- Short Guard Interval (SGI) support for improved throughput
- Greenfield and Mixed Mode preambles for compatibility and efficiency
- STBC (Space-Time Block Coding) for improved reliability in multipath environments
- Wi-Fi Multimedia (WMM) for traffic prioritization
- Block ACK, A-MPDU, A-MSDU aggregation for higher efficiency
- Automatic beacon monitoring with hardware TSF (Timing Synchronization Function)
- Over 10 virtual Wi-Fi interfaces for simultaneous STA, SoftAP, STA+AP, and promiscuous modes
- Antenna diversity for better reception in challenging RF conditions
- 802.11mc Fine Timing Measurement (FTM) for precise indoor positioning

Advanced Wi-Fi features

- Channel State Information (CSI) for Wi-Fi sensing applications
- STA, SoftAP, Wi-Fi Direct (P2P), and concurrent STA + SoftAP modes
- PTA coexistence with integrated Bluetooth/802.15.4

Bluetooth® Low Energy (LE)

- Bluetooth Core 6.0 certified
- Support for Bluetooth LE 5.2 features
- Supports Bluetooth LE 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- LE Audio with isochronous channels (CIS/BIS)
- Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, antenna array support up to 16 antennas
- LE power control
- LE privacy 1.2 with resolvable private addresses
- LE secure connections pairing with ECDH for stronger link security
- Advertising extensions with multiple advertising sets
- Concurrent roles: Central, Peripheral, Broadcaster, Observer
- Bluetooth Mesh 1.1 support for large-scale IoT networks
- High-power TX mode up to +25 dBm



- Adaptive Frequency Hopping (AFH) for coexistence with Wi-Fi/802.15.4

IEEE 802.15.4

- 2.4 GHz IEEE 802.15.4 compliant
- Operating frequency range: 2400–2483.5 MHz
- O-QPSK with 250 kbps data rate
- Thread V1.4.0 certified
- Zigbee® 3.0 support
- Matter over Thread
- Low latency channel access with CSMA-CA and guaranteed time slots (GTS) for time critical applications
- AES-128 link layer security for encrypted communication

Core

- Arm®v8-M STAR-MC1 core at up to 240 MHz:
 - 32 KB I-cache, 8 KB D-cache
 - Embedded TrustZone®
 - Supports DSP instructions with SIMD
 - 3.84 CoreMark®/MHz
- UART flash download
- Serial Wire Debug (SWD) interface

Memories

- Flash (XIP): SiP flash up to 16 MB, external flash up to 32 MB
- SiP PSRAM: up to 8 MB
- 512 KB share SRAM
- 64 KB ROM
- 4 KB OTP (One Time Programmable)

Security

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning



- TEE_M
- TrustEngine, including the following features:
 - Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
 - Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
 - Digest schemes, SHA1/224/256
 - Digest scheme, SM3
 - Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
 - Asymmetric scheme, SM2
 - Key ladder for key management
 - Lifecycle management
 - True random number generator

Clock Management

- External oscillators: 40 MHz crystal oscillator (XTALH), 32.768 kHz crystal oscillator (X32K)
- Internal oscillator: 32 kHz ring oscillator (ROSC)
- 480 MHz PLL (DPLL)

Power Management

- 2.2 to 5.5 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converter (QFN48 and BK7239NL QFN40 only) and LDO regulators
- Low power consumption:
 - Active mode RX, 2.4 GHz: 9 mA
 - Active mode RX, 5 GHz: 12 mA
 - Standby associated, DTIM = 10 without TCP keep-alive, 2.4 GHz: 39 μ A
 - Standby associated, DTIM = 10 without TCP keep-alive, 5 GHz: 40 μ A
 - Sleep mode: 47 μ A
 - Deep sleep0 mode: 2.5 μ A
 - Deep sleep1 mode: 13 μ A
 - Shutdown mode: 0.5 μ A

Peripherals

- GPIOs: 19 in QFN48, 21 in BK7239N QFN40, 20 in BK7239NL QFN40



- Configurable 2.2–3.6 V VIO supply or 1.8–1.95 V VDDRAM supply (QFN48 and BK7239NL QFN40 only)
- 2x SPI
- 1x QSPI
- 4x UART, 2 with hardware flow control and 1 with flash download support
- 1x SDIO
- 2x I2C
- 1x general-purpose DMA controller (GDMA) with 8 channels
- 1x RGB LED controller
- 12x 32-bit PWM channel
- 1x I2S
- 14-bit AUX ADC, up to 9 channels
- 6x 32-bit general-purpose timer
- 1x watchdog timer
- 1x real-time counter (RTC)
- 1x temperature sensor
- 1x anti-tamper module

Packaging

- QFN48 package, 6 x 6 x 0.75 mm
- QFN40 package, 5 x 5 x 0.75 mm
- Operating temperature range: -40 to +105 °C

Applications

The BK7239N is designed for the next generation of smart, connected, and battery-efficient devices. With Wi-Fi 6, Bluetooth LE 6.0, and IEEE 802.15.4 (Thread/Zigbee/Matter) all integrated into a single chip, it enables seamless interoperability across ecosystems while delivering ultra-low power consumption for long battery life.

- Smart home and appliances: door locks, sensors, lighting, and connected appliances that run reliably for years on batteries.
- Consumer electronics: wearables, audio devices with LE Audio, toys, and drones that need responsive, low latency wireless.
- Industrial IoT: factory sensors, smart meters, and automation systems that demand secure, always on connectivity with minimal energy use.



- Healthcare and medical: portable monitors and medical devices that combine secure data transfer with extended operating time.
- Edge devices: Matter enabled hubs, controllers, and gateways that unify Wi-Fi, Bluetooth, and Thread in one secure platform.

With its deep sleep⁰ current as low as 2.5 μA , the BK7239N makes it possible to design smaller, longer lasting, and more secure IoT products across consumer, industrial, and healthcare markets.

2 Overview

The BK7239N is a highly integrated, low-power multi-protocol wireless MCU that combines an advanced MCU subsystem with Wi-Fi 6 (802.11a/b/g/n/ac/ax), Bluetooth Low Energy (LE) 6.0, and IEEE 802.15.4 connectivity. It is designed for a wide range of connected applications, including smart home and appliances, industrial automation, smart energy, healthcare, and secure payment systems.

The MCU subsystem is built around a 240 MHz Armv8-M STAR-MC1 core with TrustZone and DSP extension, delivering high performance for protocol stacks, edge computing, and real-time control. The device integrates 512 KB SRAM, 64 KB ROM, and flexible memory options including up to 8 MB SiP PSRAM and up to 16 MB SiP flash, enabling efficient execution of complex applications. A Quad SPI interface supports high-bandwidth external memory access, while secure on-the-fly decryption ensures protection of code and data stored in off-chip XIP flash or PSRAM.

The wireless subsystem includes a 1×1 dual-band Wi-Fi 6 (802.11a/b/g/n/ac/ax) radio supporting 20 MHz/40 MHz channels in both 2.4 GHz and 5 GHz bands. This provides higher throughput, improved spectral efficiency, lower latency, and extended range compared to previous Wi-Fi generations. The Bluetooth LE 6.0 radio supports 1 Mbps, 2 Mbps, and long-range PHYs, as well as advanced features such as LE Audio and AoA/AoD for high-precision positioning. The integrated 802.15.4 radio enables support for Zigbee, Thread, and Matter, making the BK7239N a versatile platform for multi-protocol IoT devices.

The BK7239N is well-suited for Matter applications across Wi-Fi and Thread, and can operate as a Matter end device within major ecosystems.

A comprehensive Secure Element (SE) is embedded, providing secure boot, secure debug, secure connection, FOTA, provisioning, TEE_M, and TrustEngine. The integrated TrustEngine accelerates cryptographic operations with support for AES, SM4, SHA, SM3, RSA, ECC, and SM2, while a true random number generator and key ladder ensure robust key management. Together, these features establish a strong hardware root of trust and lifecycle security management.

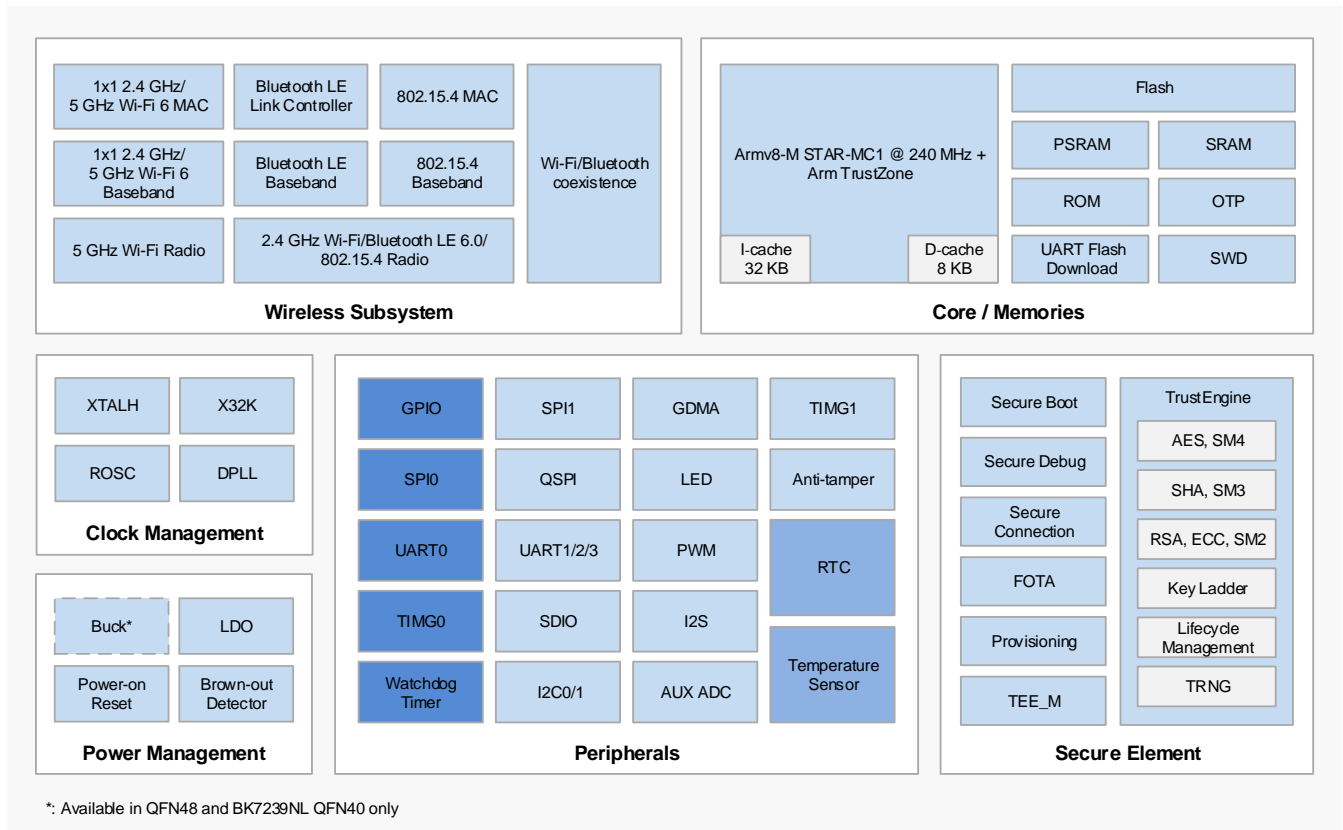
The BK7239N is optimized for low-power operation, with active receive current as low as 9 mA (2.4 GHz) and deep sleep0 current down to 2.5 μ A, enabling long battery life in portable and energy-constrained devices. Power management is simplified with an integrated buck converter and multiple LDO regulators, supporting a wide supply range of 2.2 to 5.5 V.

Available in compact QFN48 (6 × 6 mm) and QFN40 (5 × 5 mm) packages, the BK7239N supports an extended operating temperature range of -40 °C to +105 °C, making it suitable for both consumer and industrial environments.

The advanced design of the BK7239N delivers tight integration, low power, and strong security in a cost- and space-efficient wireless MCU platform, enabling developers to accelerate the deployment of next-generation IoT products.

Figure 2-1 shows the general block diagram of the BK7239N.

Figure 2-1 BK7239N Block Diagram

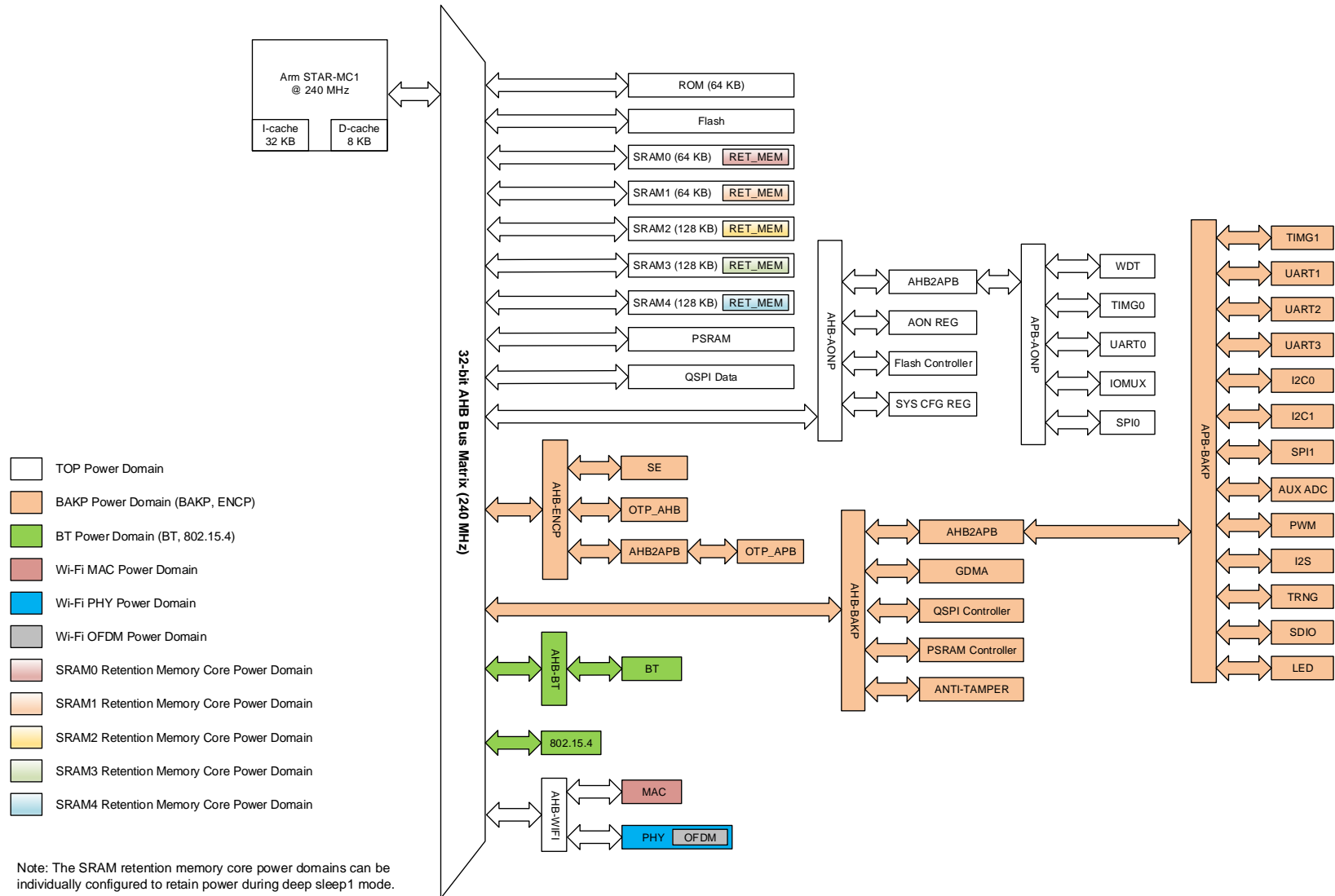


Peripheral Power Consumption

- Normal
- Low power consumption (0.875 V VDDDIG power supply)
- Low power consumption (2.2–3.6 V VIO power supply)

Figure 2-2 shows the BK7239N bus interconnect.

Figure 2-2 BK7239N Bus Interconnect



The BK7239N devices are offered in QFN40 and QFN48 packages.

- BK7239N QFN40: Includes BK7239NQN4050 and BK7239NQH4050.
- BK7239NL QFN40: Includes BK7239NLQN4050, BK7239NLQN4060, and BK7239NLQN4064.

The QFN48 and BK7239NL QFN40 both integrate a buck converter to enable enhanced power efficiency.

Table 2-1 provides a comparison of the features available for each device option.

Table 2-1 Device Options and Features

Feature		BK7239NQN48N8 QFN48	BK7239NQN/H4050 QFN40	BK7239NLQN4050/ 60/64 QFN40
SiP flash		-	4 MB	4 MB or 8 MB ⁽¹⁾
SiP PSRAM		8 MB	-	None or 4 MB ⁽¹⁾
Buck converter		Yes	-	Yes
GPIO		19	21	20
SPI	Master/Slave	2	2	2
QSPI		1	1	1
UART		4	4	4
SDIO		1	1	1
I2C	Master/Slave	2	2	2
GDMA		1	1	1
RGB LED controller		1	1	1
PWM	PWM0–11	12	12	12
I2S	Master/Slave	1	1	1
AUX ADC	14 bits	1	1	1
	Number of channels	7	9	9
General-purpose timer		6	6	6
Watchdog timer		1	1	1
Real-time counter (RTC)		1	1	1
Temperature sensor		1	1	1
Anti-tamper module		1	1	1



Feature	BK7239NQN48N8 QFN48	BK7239NQN/H4050 QFN40	BK7239NLQN4050/ 60/64 QFN40
Package	6 x 6 x 0.75 mm QFN48	5 x 5 x 0.75 mm QFN40	5 x 5 x 0.75 mm QFN40
Operating voltage	2.2 to 5.5 V		
Operating temperature	-40 to +105 °C		

(1) See Section 9 Ordering Information for detailed SiP flash/PSRAM configurations.

3 Pin Descriptions

The BK7239N provides Wi-Fi, Bluetooth LE, and IEEE 802.15.4 functionality in packages of 40 pins and 48 pins.

3.1 QFN48 Pin Descriptions

Figure 3-1 shows the pin assignments of the 6 x 6 mm, 48-pin QFN package for BK7239NQN48N8.

Figure 3-1 QFN48 Pin Assignments

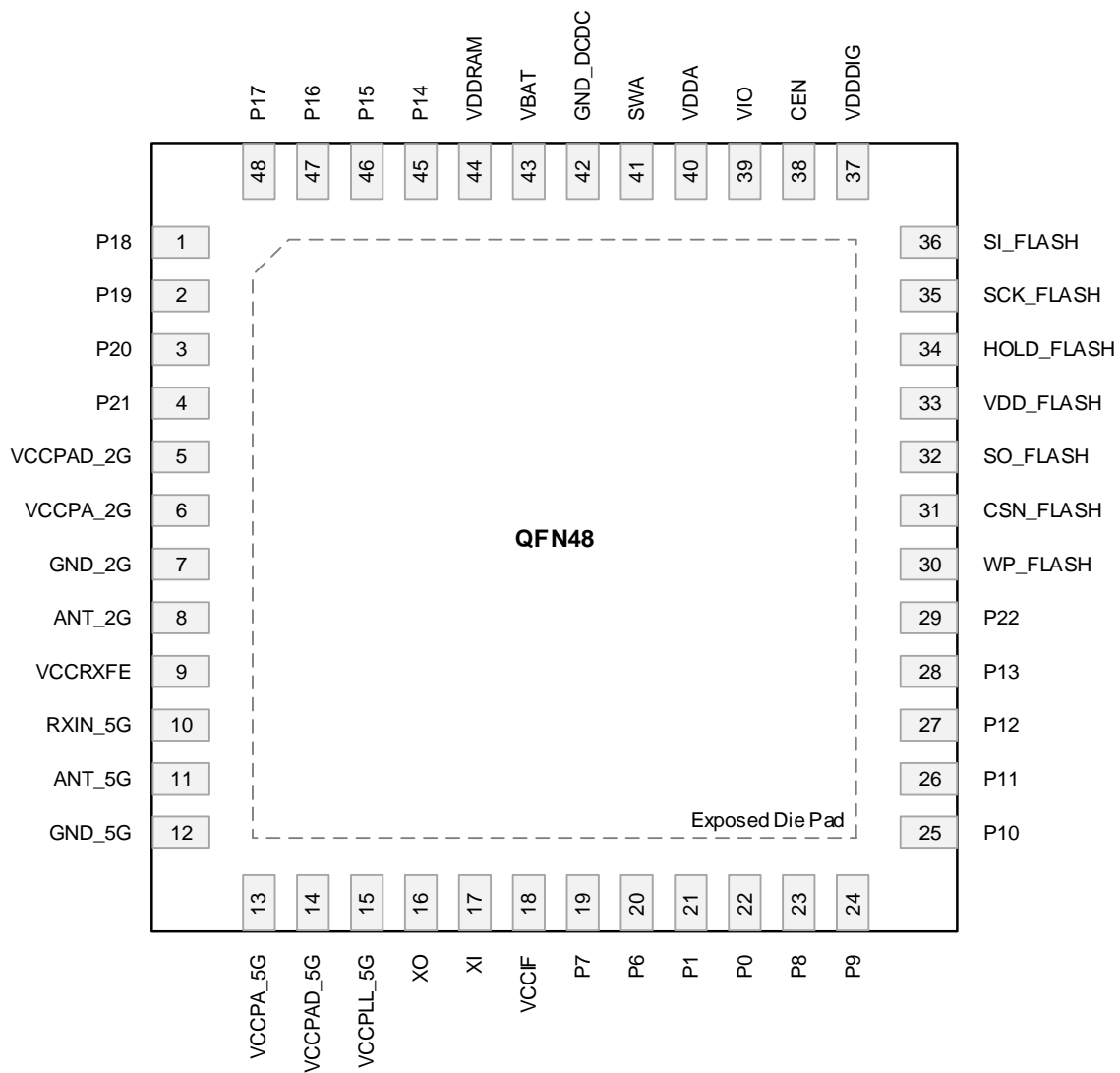


Table 3-1 shows the pin descriptions of the QFN48 package for BK7239NQN48N8.

Note: Due to power-up glitches, the following I/O pins are not recommended for applications sensitive to power-up fluctuations, such as LEDs or motor control: GPIO0, GPIO1, GPIO8, GPIO9, GPIO10, and GPIO11.

Table 3-1 QFN48 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P18	I/O	Digital	GPIO18: general-purpose I/O
2	P19	I/O	Digital	GPIO19: general-purpose I/O
3	P20	I/O	Digital	GPIO20: general-purpose I/O
4	P21	I/O	Digital	GPIO21: general-purpose I/O
5	VCCPAD_2G	-	Analog input	2.4 GHz RF PA driver power supply
6	VCCPA_2G	-	Analog input	2.4 GHz RF PA power supply
7	GND_2G	-	GND	Ground
8	ANT_2G	-	RF	2.4 GHz RF signal port
9	VCCRxFE	-	Analog input	RF receiver power supply
10	RXIN_5G	-	RF/GND	5 GHz RX input signal port When an external FEM is not present, this pin must be grounded.
11	ANT_5G	-	RF	5 GHz RF signal port
12	GND_5G	-	GND	Ground
13	VCCPA_5G	-	Analog input	5 GHz RF PA power supply
14	VCCPAD_5G	-	Analog input	5 GHz RF PA driver power supply
15	VCCPLL_5G	-	Analog input	5 GHz RF PLL power supply
16	XO	-	Analog output	40 MHz crystal output
17	XI	-	Analog input	40 MHz crystal input
18	VCCIF	-	Analog input	IF power supply
19	P7	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO7: general-purpose I/O ADC6: analog input channel
20	P6	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO6: general-purpose I/O ADC5: analog input channel
21	P1	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO1: general-purpose I/O ADC13: analog input channel

Pin #	Name	I/O	Type	Description
22	P0	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO0: general-purpose I/O ADC12: analog input channel
23	P8	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO8: general-purpose I/O ADC10: analog input channel 32K_XO: 32.768 kHz crystal output
24	P9	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO9: general-purpose I/O 32K_XI: 32.768 kHz crystal input
25	P10	I/O	Digital	<ul style="list-style-type: none"> GPIO10: general-purpose I/O DL_UART_RX: UART flash download receive data input
26	P11	I/O	Digital	<ul style="list-style-type: none"> GPIO11: general-purpose I/O DL_UART_TX: UART flash download transmit data output
27	P12	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO12: general-purpose I/O ADC14: analog input channel
28	P13	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO13: general-purpose I/O ADC15: analog input channel
29	P22	I/O	Digital	GPIO22: general-purpose I/O
30	WP_FLASH	-	Digital output	External flash write protect input
31	CSN_FLASH	-	Digital output	External flash chip select
32	SO_FLASH	-	Digital input	External flash data output
33	VDD_FLASH	-	Analog output	External flash power supply
34	HOLD_FLASH	-	Digital output	External flash hold input
35	SCK_FLASH	-	Digital output	External flash clock input
36	SI_FLASH	-	Digital output	External flash data input
37	VDDDIG	-	Analog output	Digital core LDO output
38	CEN	-	Analog input	Chip enable, active high
39	VIO	-	Analog output	IO LDO output
40	VDDA	-	Analog output	Analog buck/LDO output
41	SWA	-	Analog output	Analog buck switch output

Pin #	Name	I/O	Type	Description
42	GND_DCDC	-	GND	Buck ground
43	VBAT	-	Power	Chip power supply
44	VDDRAM	-	Analog output	EXMEM LDO output
45	P14	I/O	Digital	GPIO14: general-purpose I/O
46	P15	I/O	Digital	GPIO15: general-purpose I/O
47	P16	I/O	Digital	GPIO16: general-purpose I/O
48	P17	I/O	Digital	GPIO17: general-purpose I/O
Die pad	GND_SLUG	-	GND	Ground

3.2 BK7239N QFN40 Pin Descriptions

Figure 3-2 shows the pin assignments of the 5 x 5 mm, 40-pin QFN package for BK7239NQN4050 and BK7239NQH4050.

Figure 3-2 BK7239N QFN40 Pin Assignments

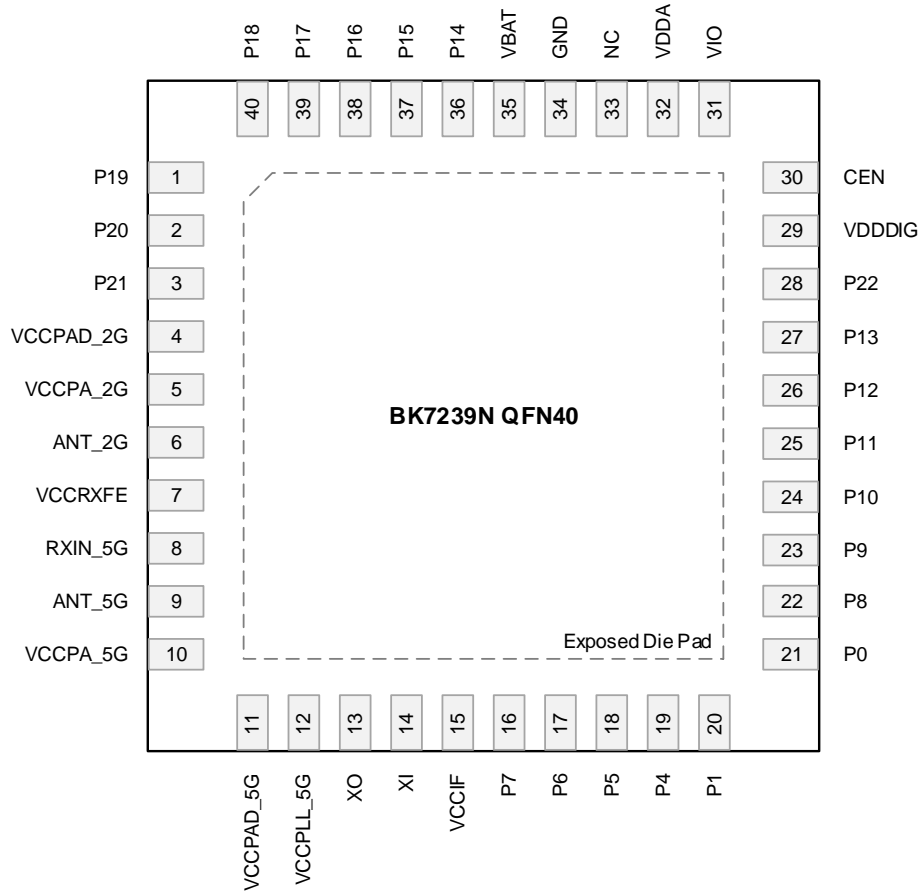


Table 3-2 shows the pin descriptions of the QFN40 package for BK7239NQN4050 and BK7239NQH4050.

Note: Due to power-up glitches, the following I/O pins are not recommended for applications sensitive to power-up fluctuations, such as LEDs or motor control: GPIO0, GPIO1, GPIO8, GPIO9, GPIO10, and GPIO11.

Table 3-2 BK7239N QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P19	I/O	Digital	GPIO19: general-purpose I/O
2	P20	I/O	Digital	GPIO20: general-purpose I/O
3	P21	I/O	Digital	GPIO21: general-purpose I/O
4	VCCPAD_2G	-	Analog input	2.4 GHz RF PA driver power supply
5	VCCPA_2G	-	Analog input	2.4 GHz RF PA power supply
6	ANT_2G	-	RF	2.4 GHz RF signal port

Pin #	Name	I/O	Type	Description
7	VCCRXFE	-	Analog input	RF receiver power supply
8	RXIN_5G	-	RF/GND	5 GHz RX input signal port When an external FEM is not present, this pin must be grounded.
9	ANT_5G	-	RF	5 GHz RF signal port
10	VCCPA_5G	-	Analog input	5 GHz RF PA power supply
11	VCCPAD_5G	-	Analog input	5 GHz RF PA driver power supply
12	VCCPLL_5G	-	Analog input	5 GHz RF PLL power supply
13	XO	-	Analog output	40 MHz crystal output
14	XI	-	Analog input	40 MHz crystal input
15	VCCIF	-	Analog input	IF power supply
16	P7	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO7: general-purpose I/O ADC6: analog input channel
17	P6	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO6: general-purpose I/O ADC5: analog input channel
18	P5	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO5: general-purpose I/O ADC4: analog input channel
19	P4	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO4: general-purpose I/O ADC3: analog input channel
20	P1	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO1: general-purpose I/O ADC13: analog input channel
21	P0	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO0: general-purpose I/O ADC12: analog input channel
22	P8	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO8: general-purpose I/O ADC10: analog input channel 32K_XO: 32.768 kHz crystal output
23	P9	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO9: general-purpose I/O 32K_XI: 32.768 kHz crystal input
24	P10	I/O	Digital	<ul style="list-style-type: none"> GPIO10: general-purpose I/O DL_UART_RX: UART flash download receive data input

Pin #	Name	I/O	Type	Description
25	P11	I/O	Digital	<ul style="list-style-type: none"> GPIO11: general-purpose I/O DL_UART_TX: UART flash download transmit data output
26	P12	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO12: general-purpose I/O ADC14: analog input channel
27	P13	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO13: general-purpose I/O ADC15: analog input channel
28	P22	I/O	Digital	GPIO22: general-purpose I/O
29	VDDDIG	-	Analog output	Digital core LDO output
30	CEN	-	Analog input	Chip enable, active high
31	VIO	-	Analog output	IO LDO output
32	VDDA	-	Analog output	Analog LDO output
33	NC	-	NC	No connect
34	GND	-	GND	Ground
35	VBAT	-	Power	Chip power supply
36	P14	I/O	Digital	GPIO14: general-purpose I/O
37	P15	I/O	Digital	GPIO15: general-purpose I/O
38	P16	I/O	Digital	GPIO16: general-purpose I/O
39	P17	I/O	Digital	GPIO17: general-purpose I/O
40	P18	I/O	Digital	GPIO18: general-purpose I/O
Die pad	GND_SLUG	-	GND	Ground

3.3 BK7239NL QFN40 Pin Descriptions

Figure 3-3 shows the pin assignments of the 5 x 5 mm, 40-pin QFN package for BK7239NLQN4050, BK7239NLQN4060, and BK7239NLQN4064.

Figure 3-3 BK7239NL QFN40 Pin Assignments

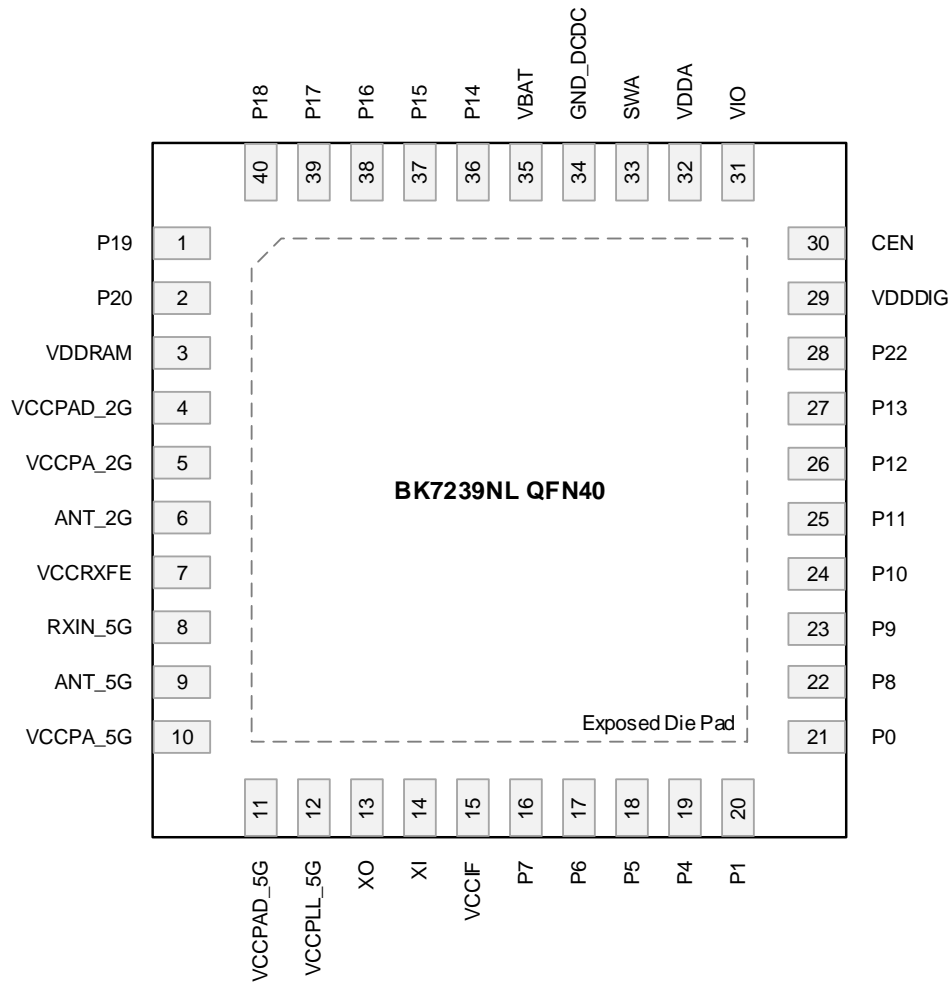


Table 3-3 shows the pin descriptions of the QFN40 package for BK7239NLQN4050, BK7239NLQN4060, and BK7239NLQN4064.

Note: Due to power-up glitches, the following I/O pins are not recommended for applications sensitive to power-up fluctuations, such as LEDs or motor control: GPIO0, GPIO1, GPIO8, GPIO9, GPIO10, and GPIO11.

Table 3-3 BK7239NL QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P19	I/O	Digital	GPIO19: general-purpose I/O
2	P20	I/O	Digital	GPIO20: general-purpose I/O
3	VDDRAM	-	Analog output	EXMEM LDO output
4	VCCPAD_2G	-	Analog input	2.4 GHz RF PA driver power supply



Pin #	Name	I/O	Type	Description
5	VCCPA_2G	-	Analog input	2.4 GHz RF PA power supply
6	ANT_2G	-	RF	2.4 GHz RF signal port
7	VCCRxFE	-	Analog input	RF receiver power supply
8	RXIN_5G	-	RF/GND	5 GHz RX input signal port When an external FEM is not present, this pin must be grounded.
9	ANT_5G	-	RF	5 GHz RF signal port
10	VCCPA_5G	-	Analog input	5 GHz RF PA power supply
11	VCCPAD_5G	-	Analog input	5 GHz RF PA driver power supply
12	VCCPLL_5G	-	Analog input	5 GHz RF PLL power supply
13	XO	-	Analog output	40 MHz crystal output
14	XI	-	Analog input	40 MHz crystal input
15	VCCIF	-	Analog input	IF power supply
16	P7	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO7: general-purpose I/O ADC6: analog input channel
17	P6	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO6: general-purpose I/O ADC5: analog input channel
18	P5	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO5: general-purpose I/O ADC4: analog input channel
19	P4	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO4: general-purpose I/O ADC3: analog input channel
20	P1	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO1: general-purpose I/O ADC13: analog input channel
21	P0	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO0: general-purpose I/O ADC12: analog input channel
22	P8	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO8: general-purpose I/O ADC10: analog input channel 32K_XO: 32.768 kHz crystal output
23	P9	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO9: general-purpose I/O 32K_XI: 32.768 kHz crystal input

Pin #	Name	I/O	Type	Description
24	P10	I/O	Digital	<ul style="list-style-type: none"> GPIO10: general-purpose I/O DL_UART_RX: UART flash download receive data input
25	P11	I/O	Digital	<ul style="list-style-type: none"> GPIO11: general-purpose I/O DL_UART_TX: UART flash download transmit data output
26	P12	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO12: general-purpose I/O ADC14: analog input channel
27	P13	I/O	Digital/Analog	<ul style="list-style-type: none"> GPIO13: general-purpose I/O ADC15: analog input channel
28	P22	I/O	Digital	GPIO22: general-purpose I/O
29	VDDDIG	-	Analog output	Digital core LDO output
30	CEN	-	Analog input	Chip enable, active high
31	VIO	-	Analog output	IO LDO output
32	VDDA	-	Analog output	Analog buck/LDO output
33	SWA	-	Analog output	Analog buck switch output
34	GND_DCDC	-	GND	Buck ground
35	VBAT	-	Power	Chip power supply
36	P14	I/O	Digital	GPIO14: general-purpose I/O
37	P15	I/O	Digital	GPIO15: general-purpose I/O
38	P16	I/O	Digital	GPIO16: general-purpose I/O
39	P17	I/O	Digital	GPIO17: general-purpose I/O
40	P18	I/O	Digital	GPIO18: general-purpose I/O
Die pad	GND_SLUG	-	GND	Ground

3.4 Pin Multiplexing

Each I/O pin of the BK7239N can be configured to perform multiple functions: GPIO function, peripheral functions, and analog functions.

The I/O pins can be configured as the following states:

- High impedance
- Input high-impedance
- Input pull-up
- Input pull-down
- Output push-pull with pull-up or pull-down
- Input/output
- Peripheral function push-pull with pull-up or pull-down
- Peripheral function open-drain with pull-up or pull-down
- Analog function

3.4.1 I/O Pin Predefined States at Reset and After Reset

Table 3-4 shows the predefined states at reset and after reset for I/Os.

Table 3-4 I/O Pin Predefined States at Reset and After Reset

I/O	Predefined State	
	At Reset	After Reset
GPIO0	Peripheral function (pull-down) (SWCLK)	Peripheral function (pull-down) (SWCLK)
GPIO1	Peripheral function (pull-up) (SWDIO)	Peripheral function (pull-up) (SWDIO)
GPIO4	High impedance	High impedance
GPIO5	High impedance	High impedance
GPIO6	High impedance	High impedance
GPIO7	High impedance	High impedance
GPIO8	High impedance	High impedance
GPIO9	Input pull-down	High impedance
GPIO10	Input pull-down	Peripheral function (DL_UART_RX)
GPIO11	Input pull-down	High impedance
GPIO12	High impedance	High impedance
GPIO13	High impedance	High impedance
GPIO14	High impedance	High impedance
GPIO15	High impedance	High impedance
GPIO16	High impedance	High impedance

I/O	Predefined State	
	At Reset	After Reset
GPIO17	High impedance	High impedance
GPIO18	High impedance	High impedance
GPIO19	High impedance	High impedance
GPIO20	High impedance	High impedance
GPIO21	High impedance	High impedance
GPIO22	High impedance	High impedance

3.4.2 I/O Matrix

The I/O multiplexer provides one configuration register for each I/O pin. Each I/O pin can be configured as a GPIO or an I/O for peripherals through the GPIOx_FUNC_SEL[6:0] field of the configuration register. Table 3-5 shows the I/O matrix.

Table 3-5 I/O Matrix

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
GPIO	7'd0	GPIO	High impedance	General-purpose I/O
	7'd1	GPIO	Input	General-purpose I/O
	7'd2	GPIO	Output	General-purpose I/O
	7'd3	GPIO	Input/output	General-purpose I/O
PTA	7'd4	BT_ACTIVE	Input	Bluetooth active
	7'd9	BT_PRIORPRITY	Input	Bluetooth priority
	7'd92	WIFI_ACTIVE	Output	Wi-Fi active
AoA/AoD	7'd5	BT_ANT0	Output	Bluetooth antenna select
	7'd6	BT_ANT1	Output	Bluetooth antenna select
	7'd7	BT_ANT2	Output	Bluetooth antenna select
	7'd8	BT_ANT3	Output	Bluetooth antenna select

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
Clock	7'd10	CLK_AUXS	Output	Clock output derived from 40 MHz CLK_XTAL/32 kHz CLK_32K/480 MHz CLK_DPLL480M (divide by 1 to 16)
	7'd11	CLK_XTALO	Output	40 MHz clock output
	7'd12	CLK_XTAL_DIV	Output	40 MHz clock output (divide by 1/2/4/8)
	7'd40	LPO_CLK	Output	32 kHz clock output
FEM support	7'd29	FEM_LNA_EN	Output	LNA bypass
	7'd93	WIFI_RX_EN	Output	Receive enable
	7'd94	WIFI_TX_EN	Output	Transmit enable
I2C0	7'd30	I2C0_SCL	Input/output	Serial clock
	7'd31	I2C0_SDA	Input/output	Serial data
I2C1	7'd32	I2C1_SCL	Input/output	Serial clock
	7'd33	I2C1_SDA	Input/output	Serial data
I2S	7'd34	I2S_MCLK	Output	Master clock
	7'd35	I2S_DIN	Input	Serial data input
	7'd36	I2S_DOUT	Output	Serial data output
	7'd37	I2S_SCK	Input/output	Serial clock
	7'd38	I2S_SYNC	Input/output	Frame synchronization
LED	7'd39	LED	Output	LED output
PWM	7'd44	PWM0	Input/output	PWM0 channel
	7'd45	PWM1	Input/output	PWM1 channel
	7'd46	PWM2	Input/output	PWM2 channel
	7'd47	PWM3	Input/output	PWM3 channel
	7'd48	PWM4	Input/output	PWM4 channel
	7'd49	PWM5	Input/output	PWM5 channel
	7'd50	PWM6	Input/output	PWM6 channel

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
	7'd51	PWM7	Input/output	PWM7 channel
	7'd52	PWM8	Input/output	PWM8 channel
	7'd53	PWM9	Input/output	PWM9 channel
	7'd54	PWM10	Input/output	PWM10 channel
	7'd55	PWM11	Input/output	PWM11 channel
QSPI	7'd56	QSPI_CS	Output	Chip select
	7'd57	QSPI_IO0	Input/output	Data
	7'd58	QSPI_IO1	Input/output	Data
	7'd59	QSPI_IO2	Input/output	Data
	7'd60	QSPI_IO3	Input/output	Data
	7'd61	QSPI_SCK	Input/output	Serial clock
SDIO	7'd62	SDIO_CLK	Input/output	Clock
	7'd63	SDIO_CMD	Input/output	Command/response
	7'd64	SDIO_DATA0	Input/output	Data
	7'd65	SDIO_DATA1	Input/output	Data
	7'd66	SDIO_DATA2	Input/output	Data
	7'd67	SDIO_DATA3	Input/output	Data
SPI0	7'd68	SPI0_MISO	Input/output	Master in slave out
	7'd69	SPI0_MOSI	Input/output	Master out slave in
	7'd70	SPI0_CSN	Input/output	Chip select
	7'd71	SPI0_SCK	Input/output	Serial clock
SPI1	7'd72	SPI1_MISO	Input/output	Master in slave out
	7'd73	SPI1_MOSI	Input/output	Master out slave in
	7'd74	SPI1_CSN	Input/output	Chip select
	7'd75	SPI1_SCK	Input/output	Serial clock
SWD	7'd76	SWCLK	Input	Serial wire clock
	7'd77	SWDIO	Input/output	Serial wire data

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
Anti-tamper	7'd78	TAMP_RX	Input	Receive data input
	7'd79	TAMP_TX	Output	Transmit data output
UART0	7'd80	UART0_CTS	Input	Clear to send
	7'd81	UART0_RTS	Output	Request to send
	7'd82	UART0_RX	Input	Receive data input
	7'd83	UART0_TX	Output	Transmit data output
UART1	7'd84	UART1_RX	Input	Receive data input
	7'd85	UART1_TX	Output	Transmit data output
UART2	7'd86	UART2_RX	Input	Receive data input
	7'd87	UART2_TX	Output	Transmit data output
UART3	7'd88	UART3_CTS	Input	Clear to send
	7'd89	UART3_RTS	Output	Request to send
	7'd90	UART3_RX	Input	Receive data input
	7'd91	UART3_TX	Output	Transmit data output

3.4.3 Pin Multiplexing of Analog Functions

Table 3-6 shows the pin multiplexing of analog functions. The I/O pins must be set to input pull-up or input pull-down to enable analog functions.

All GPIOs can be configured as wake-up (WKUP) function to wake the system from deep sleep and sleep modes.

Table 3-6 Pin Multiplexing of Analog Functions

GPIO	Analog Function	
	Analog1	Analog2
	AUX ADC	X32K
GPIO0	ADC12	
GPIO1	ADC13	
GPIO4	ADC3	
GPIO5	ADC4	



GPIO	Analog Function	
	Analog1	Analog2
	AUX ADC	X32K
GPIO6	ADC5	
GPIO7	ADC6	
GPIO8	ADC10	32K_XO
GPIO9		32K_XI
GPIO10		
GPIO11		
GPIO12	ADC14	
GPIO13	ADC15	
GPIO14		
GPIO15		
GPIO16		
GPIO17		
GPIO18		
GPIO19		
GPIO20		
GPIO21		
GPIO22		

4 Functional Description

4.1 Arm STAR-MC1 Processor

The Arm STAR-MC1 processor with TrustZone is a low gate count, highly energy efficient processor based on the Armv8-M architecture and is primarily for use in environments where security is an important consideration.

The BK7239N implementation of the STAR-MC1 supports:

- Armv8-M architecture
- Arm TrustZone technology, using the Armv8-M security extension supporting secure and non-secure states.
- Digital Signal Processing (DSP) extension
- Debug extension
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with 64 interrupts and 8 levels of priority
- Memory Protection Unit (MPU) with up to 16 non-secure regions and 16 secure regions
- Security Attribution Unit (SAU) with up to 8 non-secure or non-secure callable memory regions
- 32 KB I-cache and 8 KB D-cache

4.1.1 Nested Vectored Interrupt Controller (NVIC)

The NVIC is closely integrated with the processor to achieve low-latency interrupt processing.

Functions of the NVIC include:

- 64 interrupts
- 8 configurable interrupt priority levels (3 bits of interrupt priority)
- Dynamic reprioritization of interrupts
- Priority grouping. This enables selection of preempting interrupt levels and non-preempting interrupt levels.
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Support for the Armv8-M security extension. Secure interrupts can be prioritized above any non-secure interrupt.

4.1.2 Memory Protection Unit (MPU)

The MPU protects regions of memory. It provides up to 16 non-secure regions and 16 secure regions.

The MPU handles both the instruction and data memory accesses. It is responsible for protection checking, address access permissions, and memory attributes for all accesses.

4.1.3 Security Attribution Unit (SAU)

The SAU is a programmable unit that determines the security of an address. Eight regions are included in the SAU.

For instructions and data, the SAU returns the security attribute that is associated with the address.

For instructions, the SAU returns the security attribute (secure or non-secure) and identifies whether the instruction address is in a non-secure callable region.

For data, the SAU returns the security attribute (secure or non-secure).

The security level returned by the SAU is a combination of the region type defined in the internal SAU, if configured, and the type that is returned on the associated Implementation Defined Attribution Unit (IDAU). If an address maps to regions defined by both internal and external attribution units, the region of the highest security level is selected.

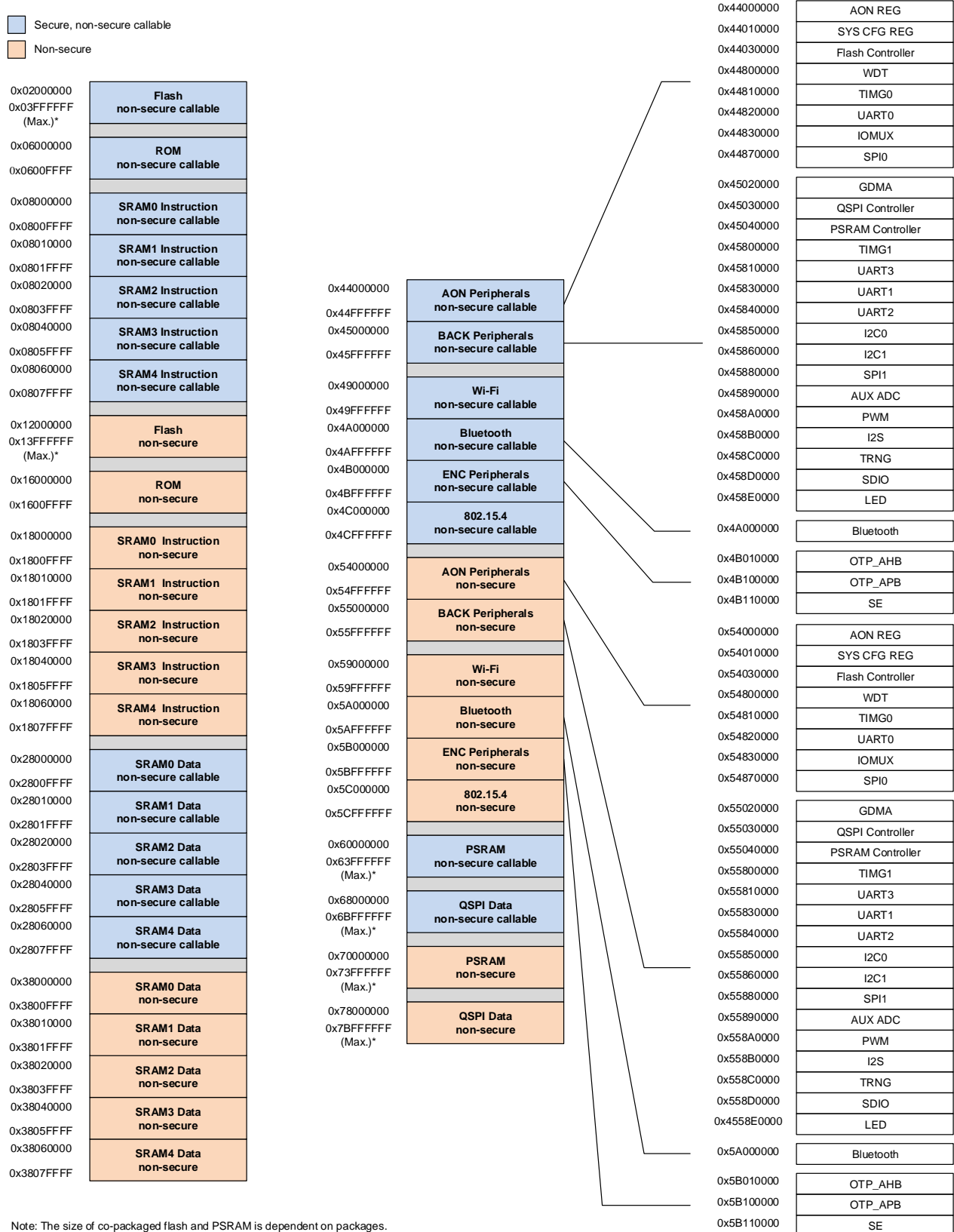
4.2 Memory Organization

When the TrustZone is enabled, the SAU and IDAU define the access permissions based on secure and non-secure states. According to IDAU security attribution, all memory spaces of the BK7239N are mapped twice for secure and non-secure states.

Both instruction and data are in little endian format. All buses have a 32-bit data width.

Figure 4-1 illustrates the memory map based on IDAU mapping.

Figure 4-1 Memory Map Based on IDAU Mapping



Note: The size of co-packaged flash and PSRAM is dependent on packages.

The internal memory of the BK7239N refers to the memory integrated onto the chip die or co-packaged within the chip, including:

- 64 KB ROM
- 512 KB share SRAM
 - 64 KB SRAM0
 - 64 KB SRAM1
 - 128 KB SRAM2
 - 128 KB SRAM3
 - 128 KB SRAM4
- 4 KB OTP, with 3 KB available for customer applications
- SiP flash: up to 16 MB, dependent on the package configuration
- SiP PSRAM: up to 8 MB, dependent on the package configuration

The STAR-MC1 core have direct access to these internal memories.

The STAR-MC1 core can access internal SRAMs (SRAM0, SRAM1, SRAM2, SRAM3, and SRAM4) via both the instruction bus and data bus with bytes, half-words (16 bits), or full words (32 bits).

4.3 Wi-Fi Subsystem

4.3.1 Wi-Fi Baseband

The BK7239N Wi-Fi baseband supports the following features:

- Standards and compatibility
 - 802.11ax (HE), backward compatible with 802.11ac (VHT), 802.11n (HT), 802.11a/g/b
- Channel bandwidths
 - 20 MHz and 40 MHz
- Modulation and coding
 - 802.11ax: MCS 0–9 (up to 256-QAM)
 - 802.11ac: MCS 0–8 (up to 256-QAM)
 - 802.11n: MCS 0–7 (up to 64-QAM)
 - Legacy: BPSK, QPSK, 16-QAM, 64-QAM
 - Dual Carrier Modulation (DCM)
 - BCC coding

- Frame formats
 - HE_SU, HE_MU, HE_ER_SU, HE_TB
 - VHT (ac), HT (n), OFDM (a/g), DSSS/CCK (b)
 - Channel State Information (CSI) feedback
- Multi-user features
 - Uplink MU-MIMO and OFDMA TX (STA)
 - Downlink MU-MIMO and OFDMA RX (STA)
- Performance enhancements
 - Guard intervals: 0.8 μ s, 1.6 μ s, 3.2 μ s (HE-LTF variants)
 - Short GI (0.4 μ s, legacy n/ac)
 - RIFS (Reduced Inter-Frame Spacing, 802.11n)
 - Aggressive packet extension
 - Extended Range (ER SU)
- Optional PHY features
 - VHT MU-PPDU receive
 - 20 MHz coexistence with mid-packet detection (enhanced CCA)
 - Receiver beam change
- Spectral intelligence
 - Spectrum monitoring
 - Interference identification/classification
 - 5G DFS Client/Slave mode with radar detection
- Power efficiency
 - Legacy PS, U-APSD, TWT
 - Dynamic bandwidth management

4.3.2 Wi-Fi MAC

The BK7239N Wi-Fi MAC supports the following features:

- Core MAC functions
 - CSMA/CA with backoff, NAV, dual-NAV (HE dual-NAV)
 - Fragmentation/reassembly
 - Block Acknowledgment (BA): M-BA, C-BA
 - QoS support (802.11e/WMM)



- Power save modes: legacy PS, U-APSD, Target Wake Time (TWT)
- Management Information Base (MIB) counters
- Agile Multiband (MBO) and Optimized Connectivity Experience (OCE)
- Frame types and control
 - Trigger frames (basic, MU-BAR, MU-RTS, BFRP, BSRP, padding)
 - HE variants of HT Control (UL Power Headroom, Receive Operation Mode)
 - Operating Mode Indication (OMI)
 - Buffer Status Reports (BSR)
 - MU frame exchange sequences
 - MU acknowledgment (ACK)
 - A-MPDU aggregation/de-aggregation (including single-MPDU A-MPDU)
- Multi-user and scheduling
 - MU-MIMO MAC (UL/DL)
 - OFDMA scheduling (UL/DL)
 - Target Wake Time scheduling
 - Multiple BSS/Station operation
- Security and management
 - WPA2/WPA3 (802.11i/802.11w)
 - Protected Management Frames (PMF)
 - Association, authentication, roaming support

4.3.3 Wi-Fi Radio

The BK7239N Wi-Fi radio supports the following features:

- 802.11ax 1x1 operation in 2.4 GHz and 5 GHz bands
- Integrated 2.4 GHz and 5 GHz PAs and LNAs
- Integrated 2.4 GHz and 5 GHz T/R switches
- Integrated 2.4 GHz and 5 GHz baluns
- Supports both internal and external PAs
- Adjustable TX power
- Antenna diversity

4.4 Bluetooth LE Subsystem

4.4.1 Bluetooth LE Features

The Bluetooth LE features are as follows:

- Bluetooth Core Specification compliant, targeting LE features
- Supports Bluetooth LE 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Bluetooth LE Class 1, Class 1.5, Class 2, and Class 3
- Single-ended, shared TX/RX path for Bluetooth LE
- All packet types (Broadcasting/Advertising/Data/Control)
- Advertising extensions
- Isochronous channel/audio over Bluetooth LE operations support
- Encryption/decryption (AES-CCM)
- Bit stream processing (CRC, whitening)
- Frequency hopping calculation
- FDMA/TDMA/events formatting and synchronization
- All device roles support (Broadcaster, Central, Observer, Peripheral)
- Direction finding (AoA/AoD)
- Device discovery (advertising and scanning)
- Up to 10 connections
- Asynchronous data reception and transmission
- Concurrent roles: Central, Peripheral, Broadcaster, Observer
- Adaptive frequency hopping and channel assessment
- LE power control
- Connection parameter update
- Data length extension up to 251 bytes
- LE secure connections
- LE privacy 1.2
- LE ping

4.4.2 Bluetooth Interfaces

- UART HCI interface, up to 10 Mbps
- PCM/I2S audio interface

4.5 IEEE 802.15.4 PHY and MAC

The BK7239N implements IEEE 802.15.4 specification and supports multiple PHY and MAC functionalities.

The 802.15.4 PHY supports Energy detection(ED), Link quality indication(LQI), channel selection, clear channel assessment (CCA), and transmitting as well as receiving packets across the physical medium.

The 802.15.4 MAC supports beacon management, channel access, GTS management, frame validation, acknowledged frame delivery, association, and disassociation. In addition, the MAC sublayer provides hooks for implementing application-appropriate security mechanisms.

802.15.4 Personal Area Networks (PANs) are of two kinds, Beacon Enabled (Slotted) and Non-Beacon Enabled (Unslotted).

In Beacon Enabled PAN, channel time is defined by superframe structure. Superframe have an active and inactive portion, bounded by beacon transmission. Active portion is divided into aNumSuperframeSlots (=16) equally spaced slots and composed of a Contention Access Period (CAP) and a Contention Free Period (CFP). Beacon frame is transmitted as part of the first slot in CAP. GTS slots are located within CFP. Beacon transmission and GTS transmission/reception happens at slot boundary. PAN coordinator only transmits beacon frame. Device only need to receive/track beacon frame. Coordinator tracks beacon of its coordinator and transmits beacon frame for its network. MAC Command Frames and Data (not marked by Higher Layer to be transmitted only during GTS) are transmitted during CAP. For transmission during CAP, CSMA-CA channel access mechanism is used. Two types of CSMA-CA algorithm used. For the beacon enabled PAN, slotted version of CSMA-CA. For the non-beacon enabled PAN, un-slotted version of CSMA-CA.

Non-beacon enabled PAN can be viewed as special case of beacon enabled PAN, where Beacon Interval (BI) is infinite, there is no CFP (GTS) and no inactive portion. Entire period is CAP. And during this CAP, un-slotted version of CSMA-CA is used. Device transmits Command Frame or Data to its coordinator during CAP. In beacon enabled PAN, Coordinator informs the availability of Command Frame or Data in its Beacon and devices requests for the Data based on this information. In non-beacon enabled PAN, higher layer will initiate MLME-POLL request for devices to send data request to coordinator and see if the ACK response suggests data available for the device, based on the Frame Pending field.

Higher layer sets up a PAN, by configuring a device as PAN coordinator. Following that for any device to participate in the PAN operation, need to Associate with one of the coordinator in the PAN. Association is applicable in both beacon enabled and non-beacon enabled PAN.

4.6 RF Transceivers

The BK7239N integrates a high-performance 2.4 GHz Wi-Fi/Bluetooth/802.15.4 transceiver and a high-performance 5 GHz Wi-Fi transceiver. Each transceiver integrates on-chip baluns. On the receive side, the balun converts the single-ended RF signal from the antenna into a differential signal, and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with either only one ANT pin or one ANT pin (transmit output) and one RXIN pin (when using an external FEM) connected to the antenna. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.7 FEM Support

The BK7239N supports the use of an external Front-End Module (FEM). The external FEM is controlled by three signals WIFI_TX_EN, WIFI_RX_EN, and FEM_LNA_EN.

Table 4-1 FEM Operating Modes

Operating Mode	WIFI_TX_EN	WIFI_RX_EN	FEM_LNA_EN
Transmit mode	1	0	0
Receive mode	0	1	1
LNA bypass mode	0	1	0
	1	1	X
Standby mode	0	0	0
Not supported	All other states		

4.8 Clock Management

The primary clock sources available in the BK7239N are as follows:

- High-frequency clocks
 - 40 MHz crystal oscillator: it outputs clock signal CLK_XTALH
 - 480 MHz digital PLL (DPLL): it outputs clock signal CLK_DPLL480M
- Low-frequency clocks
 - 32 kHz (32.768 kHz) crystal oscillator: it outputs clock signal CLK_X32K

- 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC

The system generates a low-power clock source CLK_32K for standby. The CLK_32K can be selected from CLK_DIVD, CLK_X32K, or CLK_ROSC.

Figure 4-2 shows the clock generation diagram.

Figure 4-2 Clock Generation

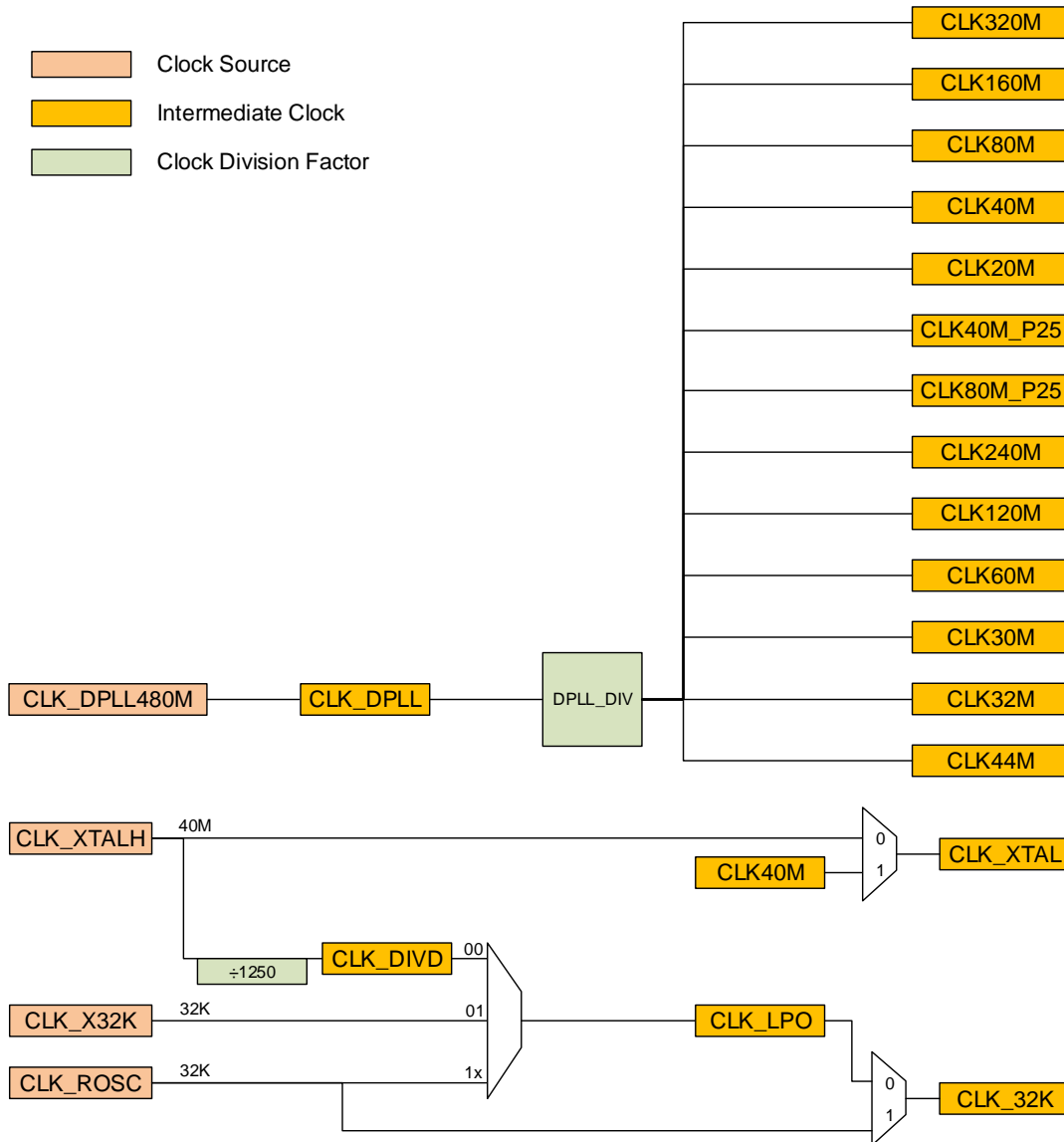


Figure 4-3 shows the clock tree for CPU and peripherals.

Figure 4-3 Clock Tree for CPU and Peripherals

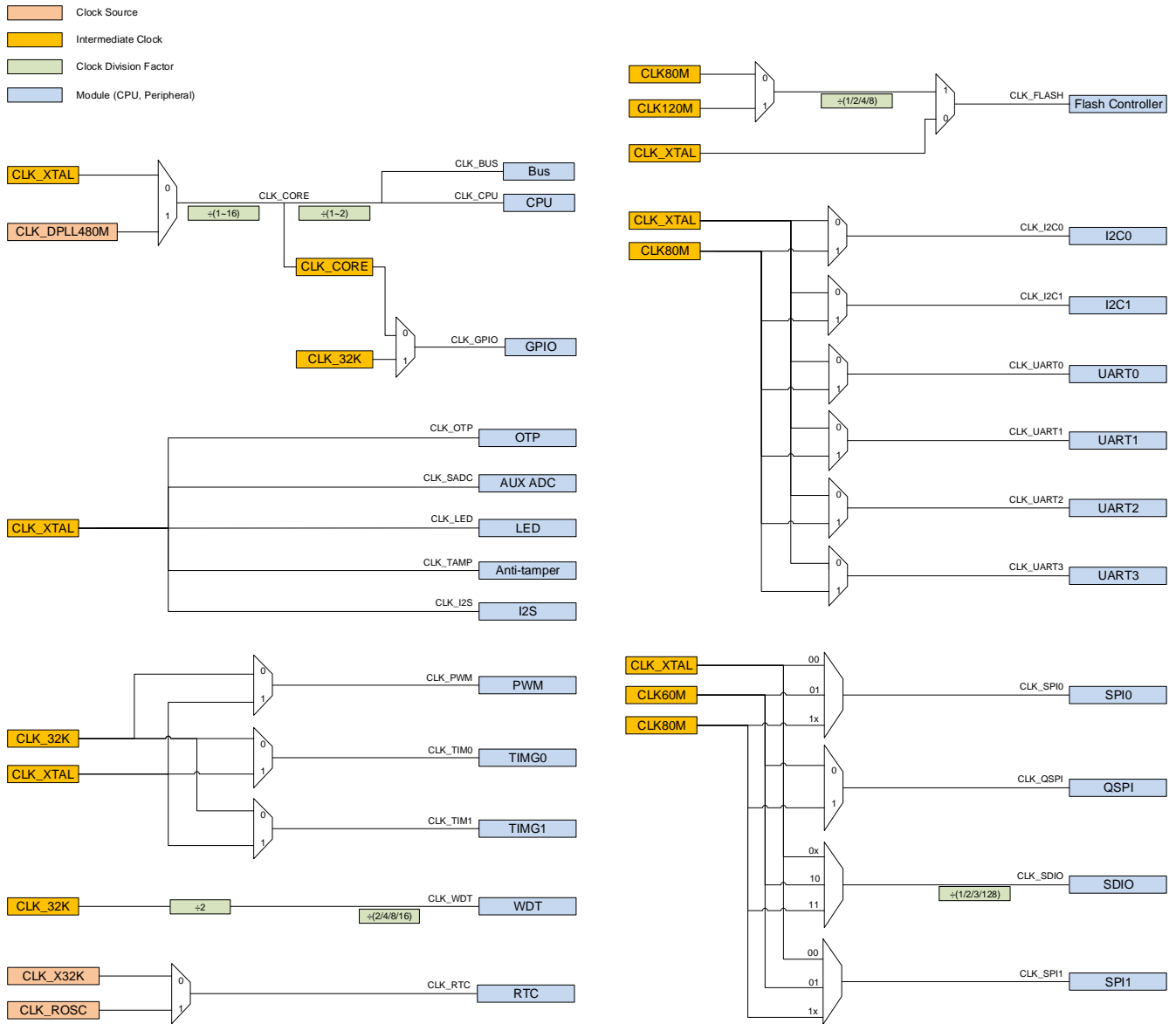
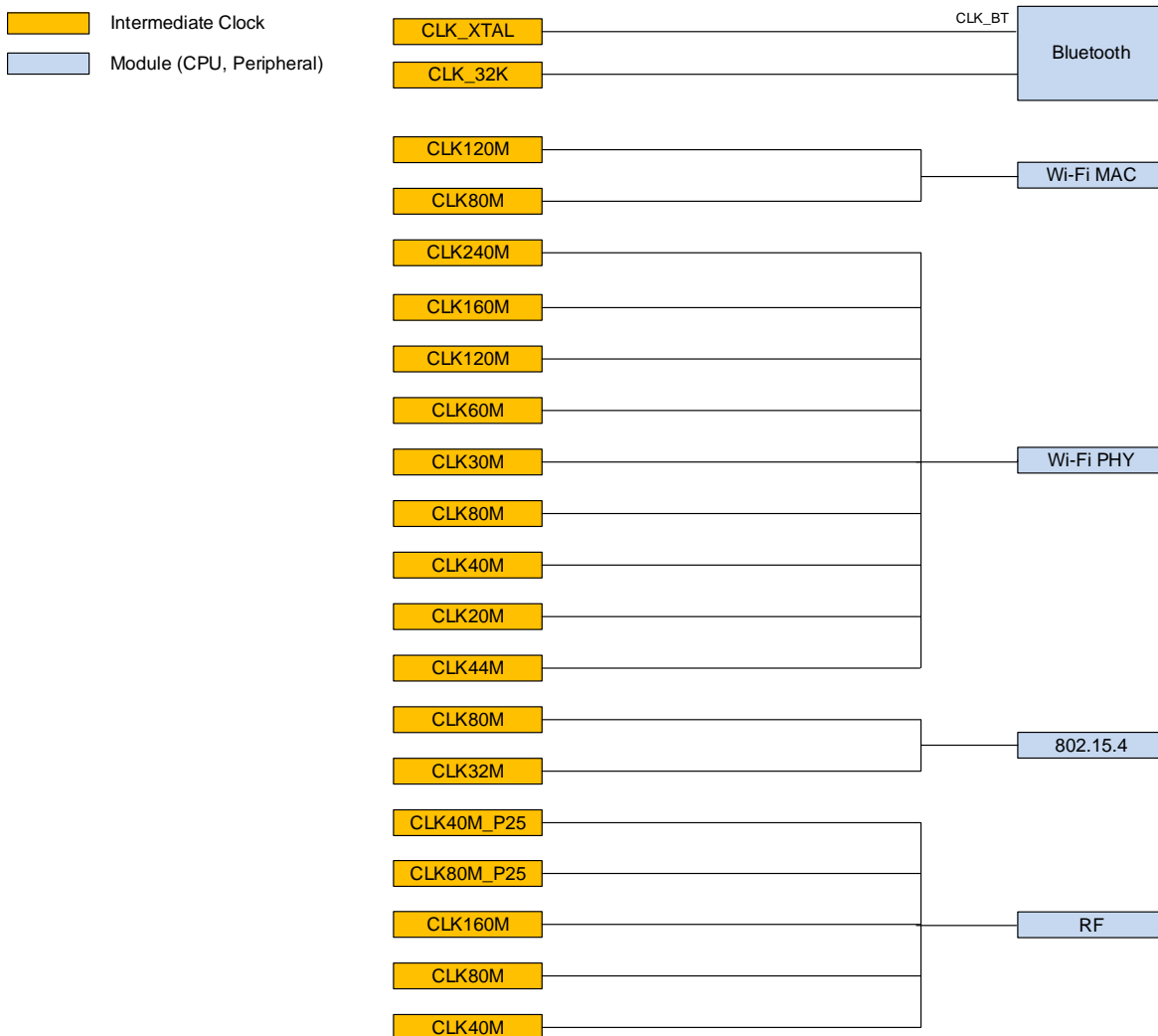


Figure 4-4 shows the clock tree for wireless subsystem.

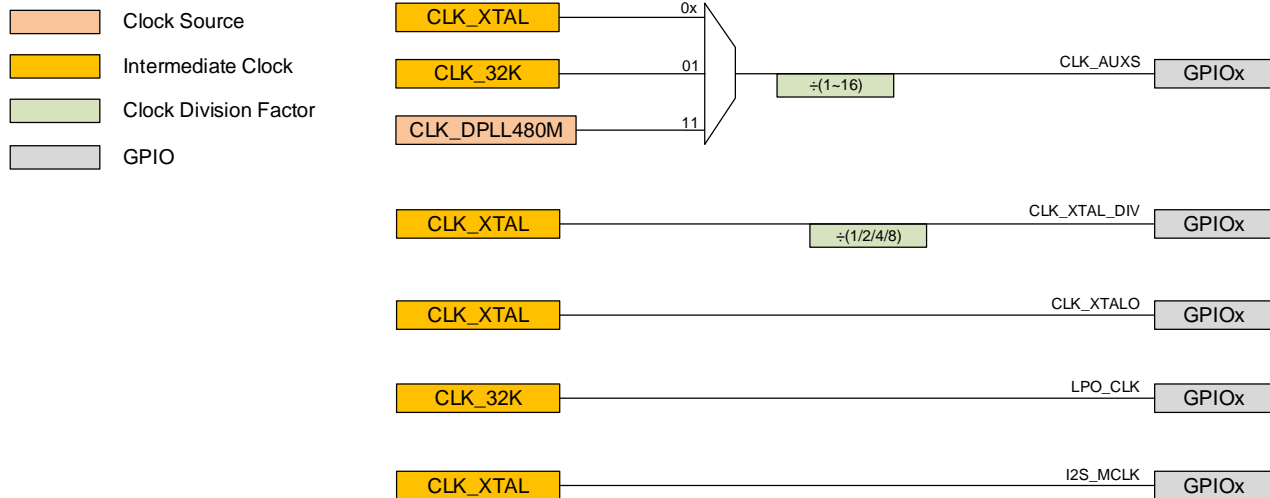
Figure 4-4 Clock Tree for Wireless Subsystem



The BK7239N also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- CLK_XTALO: clock derived from 40 MHz CLK_XTAL
- CLK_XTAL_DIV: clock derived from 40 MHz CLK_XTAL (division factor 1/2/4/8)
- CLK_AUXS: clock derived from 40 MHz CLK_XTAL/32 kHz CLK_32K/480 MHz CLK_DPLL480M (division factor 1 to 16)
- LPO_CLK: clock derived from 32 kHz CLK_32K
- I2S_MCLK: reference clock for external audio codec, derived from 40 MHz CLK_XTAL

Figure 4-5 shows the clock tree for clock output.

Figure 4-5 Clock Tree for Clock Output


4.9 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown, deep sleep0, or deep sleep1 mode.

Power-on reset and brown-out reset reset the whole chip to its initial state. The watchdog reset's reset scope is configurable and can be configured to reset the whole chip.

Wake-up from shutdown or deep sleep0 mode triggers the whole system reset, while wake-up from deep sleep1 mode triggers the reset of digital blocks.

4.10 Power Management

4.10.1 Power Scheme

The power management system on the BK7239N includes a buck converter (QFN48 and BK7239NL QFN40 only) and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

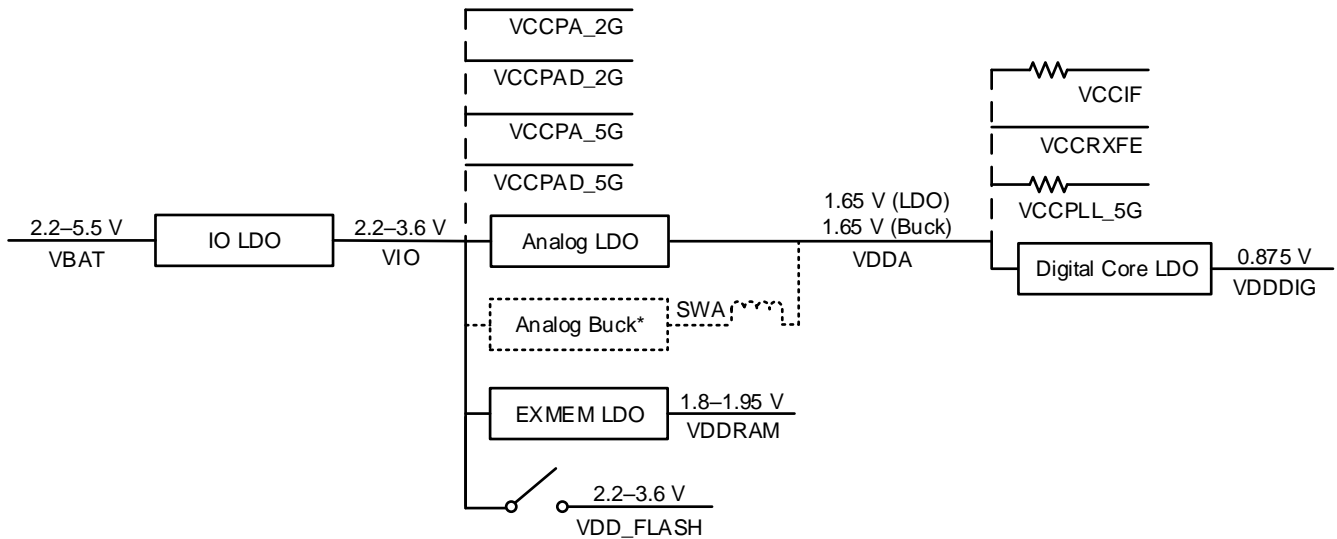
The VBAT is the external main chip supply ranging from 2.2 to 5.5 V. The VBAT generates VIO through the IO LDO regulator. In addition to being the power supply for RF PAs, GPIOs, and external flash, the VIO is also the input supply of analog LDO, analog buck, and EXMEM LDO. The buck and LDOs generate the following main power supplies:

- VDDA: power supply for RF/analog blocks. It is externally connected to VCCIF, VCCRFE, and VCCPLL_5G to supply power to the RF transceivers, and internally provides power supply to XTALH directly.

- VDDDIG: power supply for digital domain. It provides power supply for the processor, memories, basebands of Wi-Fi, Bluetooth, and 802.15.4, as well as various peripherals.
- VDDRAM: power supply for PSRAM and GPIOs.

Figure 4-6 shows the power distribution of the BK7239N.

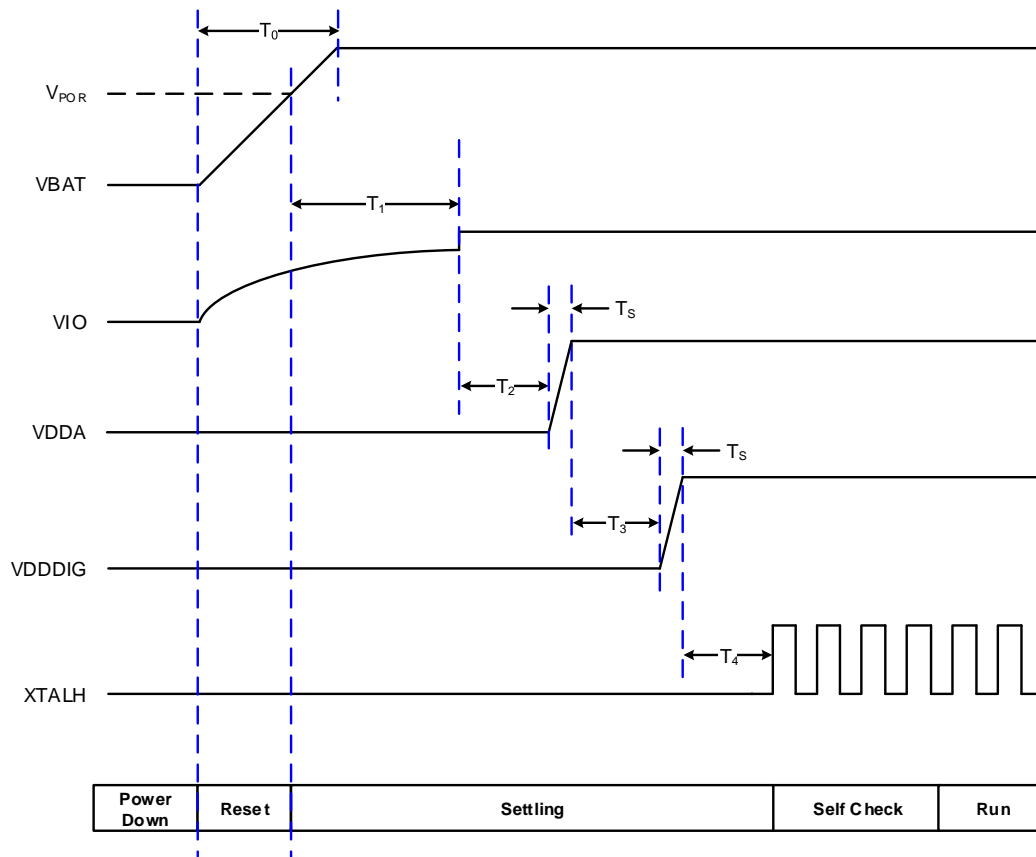
Figure 4-6 Internal Power Distribution



*: Available in QFN48 and BK7239NL QFN40 only

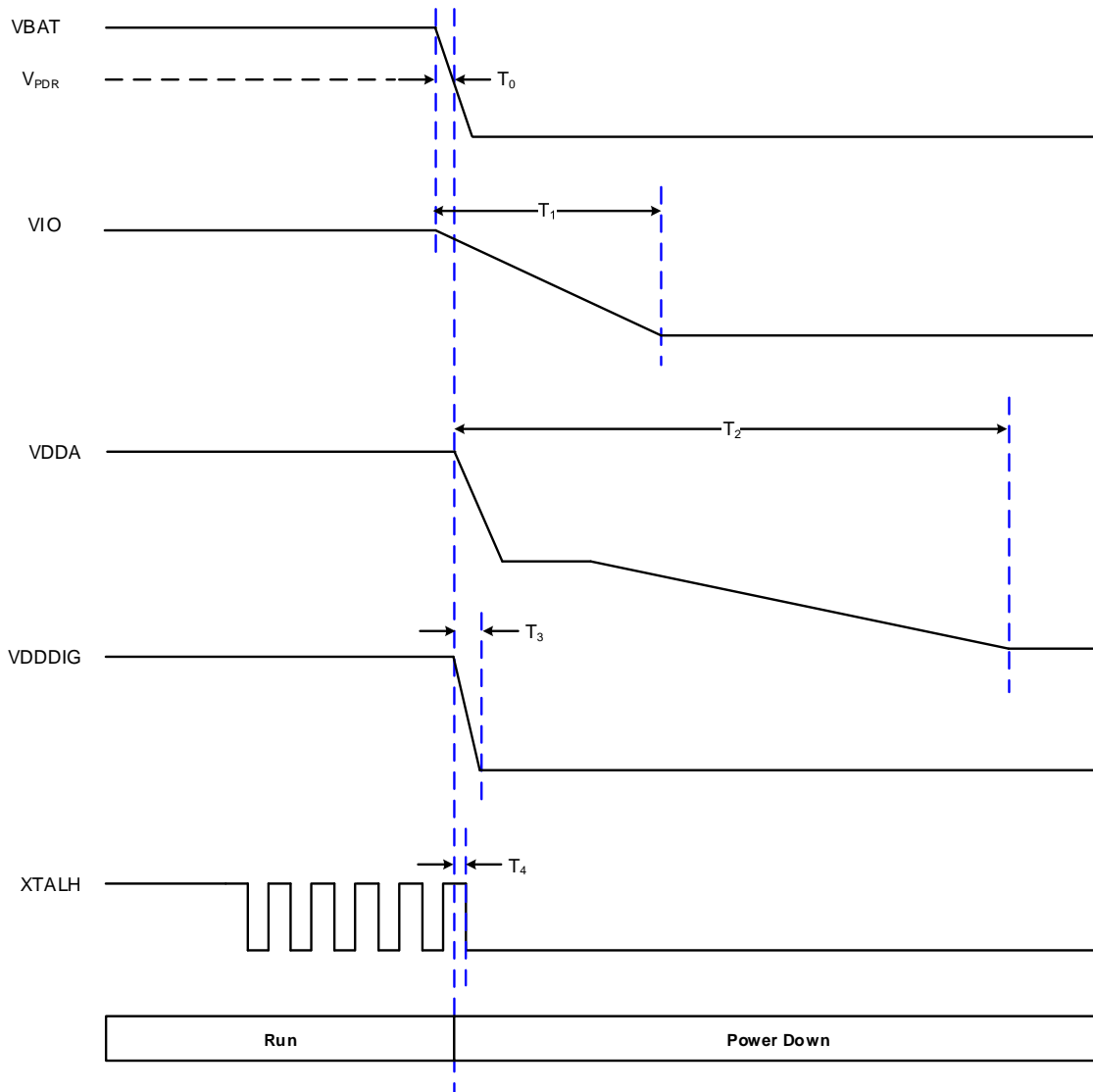
Note: Outputs from the buck converter and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-7 shows the power-up sequence of the BK7239N.

Figure 4-7 BK7239N Power-up Sequence

Table 4-2 Timing Parameters of Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V _{POR}	VBAT POR threshold	-	1.85	-	V
T ₀	VBAT power-up time	100	-	-	μs
T ₁	IO LDO ready time	-	2	-	ms
T ₂	Analog buck/LDO ready time	-	250	-	μs
T ₃	Digital core LDO ready time	-	250	-	μs
T ₄	XTALH settle time	100	-	-	μs
T _S	LDO (excl. IO LDO) settle time	0	-	-	μs

Figure 4-8 shows the power-down sequence of the BK7239N.

Figure 4-8 BK7239N Power-down Sequence

Table 4-3 Timing Parameters of Power-down Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{PDR}	VBAT PDR threshold	-	1.72	-	V
T_0	VBAT power-down time	100	-	-	μ s
T_1	IO LDO power-down time	-	50	-	ms
T_2	Analog buck/LDO power-down time	-	400	-	ms
T_3	Digital core LDO power-down time	-	3	-	ms

Parameter	Description	Min.	Typ.	Max.	Unit
T ₄	XTALH power-down time	-	100	-	μs

4.10.2 Power Supply Supervisor

The BK7239N integrates a power-on reset (POR)/power-down reset (PDR)/brown-out detector (BOD) circuit. The POR, PDR, and BOD all monitor VBAT power supply.

Power-on reset (POR)

The POR supervisor monitors VBAT power supply and compares it to a fixed threshold of 1.85 V. The system remains in reset mode when VBAT is below this threshold.

Power-down reset (PDR)

The PDR supervisor monitors VBAT power supply. A reset is generated when VBAT drops below a fixed threshold of 1.72 V.

Brown-out detector (BOD)

The BOD supervisor monitors VBAT power supply and compares it to programmable threshold levels (from 2.6 to 2.8 V). The system remains in reset mode when VBAT drops below the selected threshold. During reset:

- All circuits are powered down except the ROOSC and RTC.
- The RTC provides continuous timekeeping.

4.10.3 Power Modes

The BK7239N supports four low-power modes except active mode, namely shutdown mode, deep sleep₀ mode, deep sleep₁ mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep₀ Mode: All circuits are powered down except the RTC. A GPIO edge transition (WKUP) or an RTC event can power up the system again. The 32-bit retention register retains its contents.

Deep Sleep₁ Mode: All circuits are powered down except for the SRAM retention memory core power domains, which are individually configurable for power retention. A GPIO edge transition (WKUP) or an RTC event can power up the system again.

Sleep Mode: The MCU and all digital blocks stop their clocks. All digital blocks are in retention state. A GPIO edge transition (WKUP) or an RTC event can bring the system back to active mode.

Active Mode: The MCU is active, and all peripherals are available.

4.11 I/O Multiplexer (IOMUX)

The BK7239N has an I/O multiplexer (IOMUX) that allows the use of I/O pins as either GPIOs or I/Os for peripherals. The I/O multiplexer provides one configuration register for each I/O pin. The GPIOx_FUNC_SEL[6:0] field of the configuration register selects I/O functions:

- When GPIOx_FUNC_SEL[6:0] is set to 0 to 3, the I/O is configured as a GPIO. The GPIO type can be configured as:
 - High impedance
 - Input
 - Output
 - Input/output
- When GPIOx_FUNC_SEL[6:0] is set to 4 to 94, the I/O is configured as an I/O of a peripheral. It's should be noted that multiple I/Os cannot be configured as the same peripheral I/O.

The I/O multiplexer provides additional registers that, in GPIO mode, allow for simultaneous querying of the interrupt status and input status of all GPIOs, as well as simultaneous configuration of the output of all GPIOs.

4.12 General-purpose I/Os (GPIO)

The BK7239N has up to 21 GPIOs, which can be configured as high-impedance, input, output, or input/output. All GPIOs are shared with peripheral and/or analog functions.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Peripheral function
- Analog function
- Interrupt generation:
 - High or low level
 - Rising or falling edge
- Configurable 2.2–3.6 V VIO supply or 1.8–1.95 V VDDRAM supply (QFN48 and BK7239NL QFN40 only)

4.13 SPI Interfaces (SPI)

The BK7239N integrates two SPI interfaces that can operate in master or slave mode. The SPI interfaces allow a clock frequency up to 40 MHz in both master and slave modes.

The SPI interfaces support the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

4.14 Quad SPI Interface (QSPI)

The BK7239N embeds a Quad SPI interface that provides support for communicating with external flash, PSRAM, or AMOLED displays. The QSPI interface allows communicating up to 80 MHz.

The features of the QSPI interface are listed below:

- Single, dual, or quad SPI input/output
- Two functional modes: indirect mode and memory-mapped mode
- Fully programmable opcode and frame format
- Integrated RX FIFO and TX FIFO
- Supports 8, 16, and 32-bit data accesses

4.15 UART Interfaces (UART)

The BK7239N includes four Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 10 Mbps.

UART0 supports flash download. When UART0 is used for flash download, UART0_RX and UART0_TX are mapped to GPIO10 as DL_UART_RX and GPIO11 as DL_UART_TX, respectively.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)

- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0 and UART3)
- Flash download (UART0)
- Programmable digital filter

4.16 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7239N. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 80 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant
- SDIO card specification version 2.0 compliant
- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 40 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without CPU load

4.17 I2C Interfaces (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7239N embeds two I2C interfaces, which can operate in master or slave mode.

The features of the I2C interfaces are listed below:

- Master and slave modes
- Standard-mode (up to 100 kbps)
- Fast-mode (up to 400 kbps)
- Fast-mode Plus (up to 1 Mbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

4.18 GDMA Controller (GDMA)

The BK7239N has a general-purpose DMA controller (GDMA) with 8 DMA channels to unload CPU activity. The 8 channels are shared by peripherals that have DMA capabilities.

The GDMA controller has the features below:

- Supports transfer of the following types:
 - Single block transfer
 - Repeated block transfer
- Memory-mapped data transfers from a source to a destination:
 - Peripheral-to-memory
 - Memory-to-peripheral
 - Memory-to-memory
 - Peripheral-to-peripheral
- Programmable data width for destination and source:
 - 8 bits (byte)
 - 16 bits (half-word)
 - 32 bits (word)
- Eight-grade priority for transfers arbitration at a channel level
- Per channel event generation on the following events:
 - Transfer complete
 - Half transfer complete
 - Internal FIFO error
 - Bus error
- Each channel can be independently configured to generate interrupts for specific events.
- 8 concurrent DMA channels:
 - Each channel has a FIFO for queuing source and destination transfers.
- Secure/non-secure support:
 - A non-secure channel performs non-secure DMA transfers.
 - A secure channel can perform secure or non-secure DMA transfers.
 - TrustZone-aware DMA AHB master port
- Privileged/unprivileged support:
 - An unprivileged channel performs unprivileged DMA transfers.

- A privileged channel performs privileged DMA transfers.
- Privileged-aware AHB master port
- Privileged-aware AHB slave port

A selection of peripherals on the BK7239N have DMA capabilities, including UART0, UART1, UART2, UART3, SPI0, SPI1, SDIO, and I2S.

4.19 RGB LED Controller (LED)

The BK7239N has a RGB LED controller that supports Return-to-Zero (RZ) communication protocol. With an external LED driver IC, the RGB LED controller can support up to 1024 LED beads. The duty cycle of code 0 and code 1 of RZ communication can be configured by register. The reset signal length is also configurable.

4.20 PWM Module (PWM)

The BK7239N has an advanced-control PWM module (PWM). The PWM module consists of 12 32-bit auto-reload counters driven by 12 programmable prescalers. The PWM module has 12 independent channels for input capture, pulse edge counting, or generation of output waveforms (output compare).

The 12 independent channels can be allocated to any counter comparator output. Each of the 12 channels can generate independent waveforms or complementary waveforms when coupled with any other channels.

The features of the PWM module are listed here:

- 12 32-bit up, down, up-and-down auto-reload counters
- 12 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- 12 independent channels for:
 - Input capture
 - Pulse edge counting
 - PWM generation (edge or center-aligned mode)
- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Dedicated hardware support for smooth and precise LED dimming/fading
- Interrupt generation on the following events:

- Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
- Counter start
- Input capture
- Output compare
- LED fading end
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

4.21 I2S Interface (I2S)

The BK7239N integrates an I2S interface that supports master and slave modes with a sampling rate from 8 kHz to 384 kHz. The I2S interface supports both PCM mono channel mode and I2S stereo channel mode.

Listed here are the I2S features:

- Master or slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler
- Multiple I2S protocols supported:
 - I2S Philips standard
 - MSB-Justified standard (Left-Justified)
 - LSB-Justified standard (Right-Justified)
 - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Programmable clock polarity
- Integrated 32-bit RX FIFO and 32-bit TX FIFO, each with a depth of 32 words
- Master clock can be output to drive external audio devices.

4.22 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 14-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rates from 51.28 kHz to 1.538 MHz
- 14-bit resolution
- Up to 9 external analog input channels: ADC3/4/5/6/10/12/13/14/15
- Five internal dedicated channels:
 - VBAT monitoring channel (VBAT/4), connected to ADC0
 - Internal temperature sensor (VTEMP), connected to ADC7
 - Two internal calibration channels, connected to ADC8/11
 - Internal debug channel, connected to ADC9
- Conversion modes:
 - One-shot mode
 - Continuous mode

4.23 Timer Groups (TIMG)

The BK7239N includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, division factor between 1 and 16
- The real-time value of the counter can be read.

4.24 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect and recover from failures or malfunctions. The watchdog timer triggers a reset on expiry of a specified time period.

The watchdog timer runs on a 16 kHz clock derived from CLK_32K (CLK_32K/2). The division ratio for the 16 kHz clock can be 2, 4, 8, or 16, allowing for a maximum programmable period of up to 65.536 ($2^{16}/1$ kHz) seconds.

4.25 Real-time Counter (RTC)

The real-time counter (RTC) module features a 36-bit counter and a tick event generator. The RTC clock source can be selected from CLK_X32K or CLK_ROSC. It is used for low-power timing, and it keeps running even when the system is in deep sleep0 mode.

4.26 Temperature Sensor

The BK7239N integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ± 5 °C. The digital results can be read from the AUX ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

4.27 Anti-tamper Module

The anti-tamper module is designed to prevent, detect, and respond to physical attacks on the BK7239N chip. Once a tampering attempt is detected, it reports an interrupt to the MCU.

4.28 Security

The BK7239N provides state-of-the-art security based on a powerful security architecture. It integrates a Secure Element (SE) for cryptograph and system security control. The SE embeds all-round and robust security features to set up a top-secret execution environment for IoT devices.

The key features of the SE include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine

System Architecture

The SE software implements an all-round device-to-cloud security architecture, including:

- Provisioning mechanism in the manufacturing stage.
- Secure boot, secure debug, TRNG calibration, and FOTA update in the device boot stage.
- Secure connection and FOTA download in the device run-time stage.

The SE also introduces a remote management solution to enable users to access, monitor and manage IoT devices in a secure manner. The remote management solution includes FOTA SaaS, Secure Debug SaaS, and Provisioning SaaS.

4.28.1 Secure Boot

The secure boot solution provides the legitimacy and trustworthiness for images running on devices. It ensures that only official images which are published from OEMs are executable.

The secure boot functions include following aspects:

- Image verification
- Image encryption
- Extended program execution
- Image anti-rollback protection

4.28.2 Secure Debug

Secure debug provides a reliable mechanism for enabling the debug feature of a device after the device deployment.

Debug is one of the most commonly-used features in the device. With the debug feature, you can access all the device data, including the device firmware and the device root key.

4.28.3 FOTA

The FOTA solution implements a series of light-weight and trustworthy firmware upgrade interaction between IoT devices and servers, which includes downloading, verification, and installation.

4.28.4 Provisioning

Provisioning is the process to initialize secure credentials onto devices. It is required to happen in a secure environment such as the product line in the manufacturing stage.

The provisioning solution provides a full secure mechanism from the cloud server to devices. It keeps the security and integrity of provisioning materials, such as the device ID, model key, and the secure boot/secure debug public key hash, also keeps the device top secret such as the device root key that occurs only on the device side.

4.28.5 Secure Connection

The secure connection feature uses Mbed TLS to provide connection security in the transport layer over UDP. The key exchange method is Pre-Shared Key (PSK). The PSK's deployment happens in the manufacturing stage.

Mbed TLS provides cryptograph and SSL/TLS capabilities with TLS 1.1 and TLS 1.2.

4.28.6 BootROM

The SE includes the BootROM reference code which is integrated with the secure boot solution.

There are primary boot and recovery boot paths in the BootROM.

- Primary boot is the main boot path. Normally devices should boot to the primary path.
- Recovery boot is the secondary boot path.

4.28.7 Bootloader

The SE includes the Bootloader reference code which is integrated with the secure debug, provisioning, TRNG calibration, and FOTA solution.

In the primary bootloader, the secure debug agent, provisioning agent, and TRNG agent are integrated. The primary bootloader boots to the next image—TEE_M.

In the recovery bootloader, both the secure debug agent, TRNG agent, and the FOTA update agent are integrated. The recovery bootloader does not boot to any images.

4.28.8 TEE_M

The SE introduces TEE_M. TEE_M provides an implementation of secure world software for Armv8-M, which follows Arm Platform Security Architecture (PSA) PSA_Firmware_Framework_1.0-bet0. TEE_M provides the following services by default:

- Secure Storage: The Secure Storage (Only supports Protected Storage) service supports PSA_Storage_API-1.0-bet2 without extended functions.
- Crypto: The Crypto service supports PSA_Cryptography_API_Reference_1.0_bet1.
- DTLS: DTLS (leverages Mbed TLS) is integrated in TEE_M.

4.28.9 TrustEngine

The SE introduces TrustEngine as a secure component in the system. It provides the following features:

- High security assurance. The crypto engine supports key ladders, lifecycle management and True Random Number Generator (TRNG) which enhance the system security.
- High performance and low power for encryption/decryption operation. This is achieved by TrustEngine internal cryptography engines.
- Reduction of software complicity in security. Some security functions are implemented in TrustEngine hardware, which can reduce the risk of sensitive information leakage to non-secure hosts.

4.28.9.1 Features

TrustEngine includes the following features:

- Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
- Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
- Digest schemes, SHA1/224/256
- Digest scheme, SM3
- Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
- Asymmetric scheme, SM2
- Key ladder for key management
- Lifecycle management
- True random number generator

4.28.9.2 Supported Standards and Specifications

TrustEngine is compliant with the following standards:

- FIPS PUB 180-4: Secure Hash Standard (SHS)
- FIPS PUB 197: Advanced Encryption Standard (AES)
- NIST SP 800-38A Recommendation for Block Cipher Modes of Operation-Methods and Techniques
- NIST SP 800-38B Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication
- NIST SP 800-38C Recommendation for Block Cipher Modes of Operation-the CCM Mode for Authentication and Confidentiality
- NIST SP 800-38D, Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC

- NIST SP 800-90B Recommendation for the Entropy Sources Used for Random Bit Generation
- SM2 Public Key Cryptographic Algorithm Based on Elliptic Curves (GB/T 32918-2016)
- SM3 Cryptographic Hash Algorithm (GB/T 32905-2016)
- SM4 Block Cipher Algorithm (GB/T 32907-2016)

4.28.9.3 Components

TrustEngine consists of five major function blocks.

- Symmetric Cryptography Accelerator (SCA)
- Asymmetric Cryptography Accelerator (ACA)
- HASH engine
- One-time programmable storage access controller
- True random number generator

Symmetric Cryptography Accelerator (SCA)

SCA in TrustEngine is responsible for data encryption/decryption using the symmetric cryptography algorithm. The data encryption/decryption operations are performed through the SCA engine by sending special commands to TrustEngine.

Asymmetric Cryptography Accelerator (ACA)

The ACA engine in TrustEngine is responsible for accelerating the asymmetric cryptography, such as:

- Asymmetric encryption and decryption: RSA and ECC
- Digital signature and verification: RSA signatures and ECDSA
- Key exchange: DH (Diffie-Hellman) and ECDH

HASH Accelerator

The HASH engine in TrustEngine is responsible for digest calculation. The digest of certain data can be calculated through the HASH engine by sending special commands to TrustEngine.

True Random Number Generator

The True Random Number Generator (TRNG) generates the random bits using the internal entropy source (ring oscillator inverter chain) or the external entropy source. The random bits are required by both secure and non-secure hosts.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Chip power supply voltage	-0.3	6.0	V
VIO	IO LDO output voltage	-0.3	4.0	V
VCCPA_2G	Supply voltage for 2.4 GHz RF PA	-0.3	4.0	V
VCCPAD_2G	Supply voltage for 2.4 GHz RF PA driver	-0.3	4.0	V
VCCPA_5G	Supply voltage for 5 GHz RF PA	-0.3	4.0	V
VCCPAD_5G	Supply voltage for 5 GHz RF PA driver	-0.3	4.0	V
VDD_FLASH	Supply voltage for external flash	-0.3	4.0	V
VDDA	Analog LDO output voltage	-0.3	1.8	V
	Analog buck output voltage	-0.3	1.8	V
VCCIF	Supply voltage for IF	-0.3	1.8	V
VCCRxFE	Supply voltage for RX	-0.3	1.8	V
VCCPLL_5G	Supply voltage for 5 GHz RF PLL	-0.3	1.8	V
VDDDIG	Digital core LDO output voltage	-0.3	1.1	V
VDDRAM	EXMEM LDO output voltage	-0.3	2.1	V
SWA	Analog buck switch output voltage	-0.3	4.0	V
P _{RX}	RX input power	-	10	dBm
T _{STR}	Storage temperature range	-55	150	°C

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM		GPIO pins	±3000	V

Parameter	Description	Test Condition	Value	Unit
	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001	RF/analog pins	±3000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002	GPIO pins	±1000	V
		RF/analog pins	±500	V
Latch-up	Latch-up sensitivity, per JESD78F.02	25 °C	±200	mA

5.3 Recommended Operating Conditions

Parameter	Description	Min. ⁽¹⁾	Typ.	Max.	Unit
VBAT ⁽²⁾	Chip power supply voltage	2.2	3.3	5.5	V
VBAT slew rate	-	300	-	-	mV/ms
VIO	IO LDO output voltage	2.2	3.0	3.6	V
VCCPA_2G	Supply voltage for 2.4 GHz RF PA	2.2	3.0	3.6	V
VCCPAD_2G	Supply voltage for 2.4 GHz RF PA driver	2.2	3.0	3.6	V
VCCPA_5G	Supply voltage for 5 GHz RF PA	2.2	3.0	3.6	V
VCCPAD_5G	Supply voltage for 5 GHz RF PA driver	2.2	3.0	3.6	V
VDD_FLASH	Supply voltage for external flash	2.2	3.0	3.6	V
VDDA	Analog LDO output voltage	-	1.65	-	V
	Analog buck output voltage	-	1.65	-	V
VCCIF	Supply voltage for IF	-	1.65	-	V
VCCRxFE	Supply voltage for RX	-	1.65	-	V
VCCPLL_5G	Supply voltage for 5 GHz RF PLL	-	1.65	-	V
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
T _{OPR}	Operating temperature range	-40	-	105	°C

(1) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. Care must be taken when operating at the minimum specified voltage.

(2) To ensure WLAN performance, the ripple on the supply must be less than $V_{pp} = 100$ mV.

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{IH}	High-level input voltage	-	0.7 V _{IO}	-	V _{IO} + 0.3	V
V _{IL}	Low-level input voltage	-	-0.3	-	0.3 V _{IO}	V
V _{OH}	High-level output voltage	-	0.8 V _{IO}	-	-	V
V _{OL}	Low-level output voltage	-	-	-	0.1 V _{IO}	V
V _{T+}	Schmitt-trigger high-level input voltage	V _{IO} = 3.3 V	1.425	1.585	1.735	V
		V _{IO} = 1.8 V	0.885	1.025	1.165	V
V _{T-}	Schmitt-trigger low-level input voltage	V _{IO} = 3.3 V	1.185	1.285	1.385	V
		V _{IO} = 1.8 V	0.685	0.735	0.785	V
I _{OH}	High-level source current	V _{OH} = 0.8 V _{IO} , GPIO_CAPACITY = 3	-	40	-	mA
		V _{OH} = 0.8 V _{IO} , GPIO_CAPACITY = 2	-	30	-	mA
		V _{OH} = 0.8 V _{IO} , GPIO_CAPACITY = 1	-	18	-	mA
		V _{OH} = 0.8 V _{IO} , GPIO_CAPACITY = 0	-	10	-	mA
I _{OL}	Low-level sink current	V _{OL} = 0.15 V _{IO} , GPIO_CAPACITY = 3	-	36	-	mA
		V _{OL} = 0.15 V _{IO} , GPIO_CAPACITY = 2	-	28	-	mA
		V _{OL} = 0.15 V _{IO} , GPIO_CAPACITY = 1	-	16	-	mA
		V _{OL} = 0.15 V _{IO} , GPIO_CAPACITY = 0	-	8	-	mA
R _{PU}	Weak pull-up resistor	-	-	40	-	kΩ
R _{PD}	Weak pull-down resistor	-	-	44	-	kΩ

5.5 IO LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO output voltage	2.2	3.0	3.6	V
Load current	-	-	-	300	mA

5.6 Analog LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog LDO output voltage	-	1.65	-	V
Load current	-	-	-	150	mA

5.7 Core LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
Load current	-	-	-	100	mA

5.8 EXMEM LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
Load current	-	-	-	50	mA

5.9 Analog Buck

Note: The parameters in this section are applicable only to QFN48 and BK7239NL QFN40.

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog buck output voltage	-	1.65	-	V
Load current	-	-	-	150	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz

Parameter	Description	Min.	Typ.	Max.	Unit
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	$\text{m}\Omega$
Inductor saturation current	-	200	-	-	mA

5.10 Brown-out Detector (BOD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BOD}	BOD threshold	Supply falling	2.6	-	2.8	V
		Supply rising	2.8	-	3.0	V
$V_{\text{BOD_HYST}}$	BOD hysteresis	-	-	200	-	mV
$I_{\text{BOD_RST}}$	Supply current in BOD reset state	$V_{\text{BAT}} < V_{\text{BOD}}$, ROOSC and RTC active	-	2.3	-	μA

5.11 40 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	40	-	MHz
$\Delta\text{F}/\text{F0}$	Frequency tolerance	25 °C	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 °C crystal	-20	-	+20	ppm
		-30 to 85 °C crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	8	9	pF
TS	Trim sensitivity	3225 package	-	26	-	ppm/pF
		2016 package	-	17	-	ppm/pF

5.12 32.768 kHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	32.768	-	kHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\Delta F/F_0$	Frequency tolerance	25 °C	-20	-	+20	ppm
T _{OPR}	Operating temperature range	-	-40	-	85	°C
CL	Load capacitance	-	-	12.5	-	pF
ESR	Equivalent series resistance	25 °C	-	-	70	k Ω

5.13 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Band	Condition	Min.	Typ.	Max.	Unit
Active Mode						
QFN48 and BK7239NL QFN40						
RX current	2.4 GHz	-	-	9	-	mA
	5 GHz	-	-	12	-	mA
TX current	WLAN 2.4 GHz	11b: 11 Mbps DSSS @ 18 dBm	-	270	-	mA
		11g: 54 Mbps OFDM @ 16 dBm	-	255	-	mA
		11n: MCS7, HT20 @ 15 dBm	-	250	-	mA
		11ax: MCS7, HE20 @ 15 dBm	-	235	-	mA
	WLAN 5 GHz	11a: 54 Mbps OFDM @ 16 dBm	-	300	-	mA
		11n: MCS7, HT20 @ 15 dBm	-	295	-	mA
		11ax: MCS7, HE20 @ 15 dBm	-	285	-	mA
	Bluetooth LE	15 dBm	-	210	-	mA
		6 dBm	-	120	-	mA
		0 dBm	-	100	-	mA
-15 dBm		-	90	-	mA	
BK7239N QFN40						
RX current	2.4 GHz	-	-	19	-	mA
	5 GHz	-	-	30	-	mA



Parameter	Band	Condition	Min.	Typ.	Max.	Unit
TX current	WLAN 2.4 GHz	11b: 11 Mbps DSSS @ 18 dBm	-	300	-	mA
		11g: 54 Mbps OFDM @ 16 dBm	-	275	-	mA
		11n: MCS7, HT20 @ 15 dBm	-	270	-	mA
		11ax: MCS7, HE20 @ 15 dBm	-	255	-	mA
	WLAN 5 GHz	11a: 54 Mbps OFDM @ 16 dBm	-	320	-	mA
		11n: MCS7, HT20 @ 15 dBm	-	315	-	mA
		11ax: MCS7, HE20 @ 15 dBm	-	300	-	mA
	Bluetooth LE	15 dBm	-	240	-	mA
		6 dBm	-	150	-	mA
		0 dBm	-	130	-	mA
-15 dBm		-	120	-	mA	
Wi-Fi IEEE Power Save Mode						
QFN48 and BK7239NL QFN40						
Standby associated, DTIM = 1	2.4 GHz	Without TCP keep-alive	-	195	-	μA
Standby associated, DTIM = 3		Without TCP keep-alive	-	80	-	μA
Standby associated, DTIM = 10		Without TCP keep-alive	-	39	-	μA
Standby associated, DTIM = 1	5 GHz	Without TCP keep-alive	-	210	-	μA
Standby associated, DTIM = 3		Without TCP keep-alive	-	85	-	μA
Standby associated, DTIM = 10		Without TCP keep-alive	-	40	-	μA

Parameter	Band	Condition	Min.	Typ.	Max.	Unit
BK7239N QFN40						
Standby associated, DTIM = 1	2.4 GHz	Without TCP keep-alive	-	400	-	μA
Standby associated, DTIM = 3		Without TCP keep-alive	-	155	-	μA
Standby associated, DTIM = 10		Without TCP keep-alive	-	66	-	μA
Standby associated, DTIM = 1	5 GHz	Without TCP keep-alive	-	420	-	μA
Standby associated, DTIM = 3		Without TCP keep-alive	-	180	-	μA
Standby associated, DTIM = 10		Without TCP keep-alive	-	70	-	μA
Sleep Mode						
Deep sleep0		Only RTC is active	-	2.5	-	μA
Deep sleep1		128 KB SRAM retention	-	13	-	μA
Sleep		-	-	47	-	μA
Shutdown Mode						
Shutdown		-	-	0.5	-	μA

5.14 RF Characteristics

Unless otherwise noted, the RF data is measured at the chip port, where RF cable is connected, including the front-end loss. The front-end circuit is a matching network designed to ensure that the product complies with wireless regulations in various countries.

5.14.1 WLAN RF Characteristics

5.14.1.1 WLAN 2.4 GHz Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER)	1 Mbps DSSS	-	-100	-	dBm
	2 Mbps DSSS	-	-97	-	dBm
	5.5 Mbps DSSS	-	-95	-	dBm
	11 Mbps DSSS	-	-91	-	dBm
Sensitivity - IEEE 802.11g (10% PER)	6 Mbps OFDM	-	-94	-	dBm
	9 Mbps OFDM	-	-93	-	dBm
	12 Mbps OFDM	-	-92	-	dBm
	18 Mbps OFDM	-	-90	-	dBm
	24 Mbps OFDM	-	-87	-	dBm
	36 Mbps OFDM	-	-84	-	dBm
	48 Mbps OFDM	-	-80	-	dBm
	54 Mbps OFDM	-	-78	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER)	HT20, MCS0	-	-94	-	dBm
	HT20, MCS1	-	-92	-	dBm
	HT20, MCS2	-	-89	-	dBm
	HT20, MCS3	-	-87	-	dBm
	HT20, MCS4	-	-83	-	dBm
	HT20, MCS5	-	-79	-	dBm
	HT20, MCS6	-	-78	-	dBm
	HT20, MCS7	-	-76	-	dBm
	HT40, MCS0	-	-90	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity - IEEE 802.11n, 40 MHz (10% PER)	HT40, MCS1	-	-88	-	dBm
	HT40, MCS2	-	-86	-	dBm
	HT40, MCS3	-	-84	-	dBm
	HT40, MCS4	-	-80	-	dBm
	HT40, MCS5	-	-77	-	dBm
	HT40, MCS6	-	-75	-	dBm
	HT40, MCS7	-	-73	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER)	HE20, MCS0	-	-94	-	dBm
	HE20, MCS1	-	-92	-	dBm
	HE20, MCS2	-	-90	-	dBm
	HE20, MCS3	-	-87	-	dBm
	HE20, MCS4	-	-83	-	dBm
	HE20, MCS5	-	-80	-	dBm
	HE20, MCS6	-	-78	-	dBm
	HE20, MCS7	-	-76	-	dBm
	HE20, MCS8	-	-73	-	dBm
	HE20, MCS9	-	-70	-	dBm
Maximum Receive Level					
Maximum receive level @ 2.4 GHz	11b: 1 Mbps (8% PER, 1024 octets)	-	10	-	dBm
	11b: 11 Mbps (8% PER, 1024 octets)	-	10	-	dBm
	11g: 6 Mbps (10% PER, 1000 octets)	-	10	-	dBm
	11g: 54 Mbps (10% PER, 1000 octets)	-	5	-	dBm
	11n: HT20 MCS0 (10% PER, 4096 octets)	-	10	-	dBm
	11n: HT20 MCS7 (10% PER, 4096 octets)	-	0	-	dBm



Parameter	Condition	Min.	Typ.	Max.	Unit	
	11n: HT40 MCS0 (10% PER, 4096 octets)	-	10	-	dBm	
	11n: HT40 MCS7 (10% PER, 4096 octets)	-	0	-	dBm	
	11ax: HE20 MCS0 (10% PER, 4096 octets)	-	10	-	dBm	
	11ax: HE20 MCS9 (10% PER, 4096 octets)	-	0	-	dBm	
Adjacent Channel Rejection						
Adjacent channel (± 30 MHz) rejection - IEEE 802.11b (8% PER with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	35	44	-	dB
	2 Mbps DSSS	-74 dBm	35	44	-	dB
Adjacent channel (± 25 MHz) rejection - IEEE 802.11b (8% PER with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	35	41	-	dB
	11 Mbps DSSS	-70 dBm	35	40	-	dB
Adjacent channel (± 25 MHz) rejection - IEEE 802.11g (10% PER with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	16	43	-	dB
	54 Mbps OFDM	-62 dBm	-1	24	-	dB
Adjacent channel (± 25 MHz) rejection - IEEE 802.11n (10% PER with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	16	40	-	dB
	HT20, MCS7	-61 dBm	-2	20	-	dB
Adjacent channel (± 40 MHz) rejection - IEEE 802.11n (10% PER with desired signal level as specified in Condition)	HT40, MCS0	-76 dBm	16	33	-	dB
	HT40, MCS7	-58 dBm	-2	19	-	dB
Adjacent channel (± 20 MHz) rejection - IEEE 802.11ax (10% PER with desired signal level as specified in Condition)	HE20, MCS0	-79 dBm	16	40	-	dB
	HE20, MCS9	-54 dBm	-9	14	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
Spurious Emissions					
Spurious emissions	< 1 GHz	-	-	-60	dBm
	> 1 GHz	-	-	-55	dBm

5.14.1.2 WLAN 2.4 GHz Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX Power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	20	-	dBm
	11 Mbps DSSS	-	20	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	17	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	18	-	dBm
	HT20, MCS7	-	17	-	dBm
	HT40, MCS0	-	16	-	dBm
	HT40, MCS7	-	14	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	18	-	dBm
	HE20, MCS9	-	14	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-55	-	dBm
	> 1 GHz	-	-45	-	dBm

5.14.1.3 WLAN 5 GHz Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	4900	-	5925	MHz
Sensitivity					
Sensitivity - IEEE 802.11a (10% PER)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-77	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER)	HT20, MCS0	-	-91	-	dBm
	HT20, MCS1	-	-90	-	dBm
	HT20, MCS2	-	-87	-	dBm
	HT20, MCS3	-	-84	-	dBm
	HT20, MCS4	-	-81	-	dBm
	HT20, MCS5	-	-77	-	dBm
	HT20, MCS6	-	-75	-	dBm
	HT20, MCS7	-	-74	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz (10% PER)	HT40, MCS0	-	-89	-	dBm
	HT40, MCS1	-	-87	-	dBm
	HT40, MCS2	-	-84	-	dBm
	HT40, MCS3	-	-82	-	dBm
	HT40, MCS4	-	-78	-	dBm
	HT40, MCS5	-	-74	-	dBm
	HT40, MCS6	-	-73	-	dBm



Parameter	Condition	Min.	Typ.	Max.	Unit
	HT40, MCS7	-	-71	-	dBm
Sensitivity - IEEE 802.11ac, 20 MHz (10% PER)	VHT20, MCS0	-	-91	-	dBm
	VHT20, MCS1	-	-89	-	dBm
	VHT20, MCS2	-	-86	-	dBm
	VHT20, MCS3	-	-83	-	dBm
	VHT20, MCS4	-	-80	-	dBm
	VHT20, MCS5	-	-75	-	dBm
	VHT20, MCS6	-	-74	-	dBm
	VHT20, MCS7	-	-73	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER)	HE20, MCS0	-	-91	-	dBm
	HE20, MCS1	-	-89	-	dBm
	HE20, MCS2	-	-87	-	dBm
	HE20, MCS3	-	-85	-	dBm
	HE20, MCS4	-	-81	-	dBm
	HE20, MCS5	-	-77	-	dBm
	HE20, MCS6	-	-75	-	dBm
	HE20, MCS7	-	-73	-	dBm
	HE20, MCS8	-	-69	-	dBm
	HE20, MCS9	-	-67	-	dBm
Maximum Receive Level					
Maximum receive level @ 5 GHz	11a: 6 Mbps (10% PER, 1000 octets)	-	10	-	dBm
	11a: 54 Mbps (10% PER, 1000 octets)	-	5	-	dBm
	11n: HT20 MCS0 (10% PER, 4096 octets)	-	10	-	dBm
	11n: HT20 MCS7 (10% PER, 4096 octets)	-	0	-	dBm
	11n: HT40 MCS0 (10% PER, 4096 octets)	-	10	-	dBm



Parameter	Condition	Min.	Typ.	Max.	Unit	
	11n: HT40 MCS7 (10% PER, 4096 octets)	-	0	-	dBm	
	11ac: VHT20 MCS0 (10% PER, 4096 octets)	-	10	-	dBm	
	11ac: VHT20 MCS7 (10% PER, 4096 octets)	-	0	-	dBm	
	11ax: HE20 MCS0 (10% PER, 4096 octets)	-	10	-	dBm	
	11ax: HE20 MCS9 (10% PER, 4096 octets)	-	0	-	dBm	
Adjacent Channel Rejection						
Adjacent channel (± 20 MHz) rejection - IEEE 802.11a (10% PER with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	16	39	-	dB
	54 Mbps OFDM	-62 dBm	-1	26	-	dB
Adjacent channel (± 20 MHz) rejection - IEEE 802.11n (10% PER with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	16	38	-	dB
	HT20, MCS7	-61 dBm	-2	21	-	dB
Adjacent channel (± 40 MHz) rejection - IEEE 802.11n (10% PER with desired signal level as specified in Condition)	HT40, MCS0	-76 dBm	16	33	-	dB
	HT40, MCS7	-58 dBm	-2	19	-	dB
Adjacent channel (± 20 MHz) rejection - IEEE 802.11ac (10% PER with desired signal level as specified in Condition)	VHT20, MCS0	-79 dBm	16	38	-	dB
	VHT20, MCS7	-61 dBm	-2	21	-	dB
Adjacent channel (± 20 MHz) rejection - IEEE 802.11ax (10% PER with desired signal level as specified in Condition)	HE20, MCS0	-79 dBm	16	33	-	dB
	HE20, MCS9	-54 dBm	-9	2	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit	
Nonadjacent Channel Rejection						
Nonadjacent channel (± 40 MHz) rejection - IEEE 802.11a (10% PER with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	32	41	-	dB
	54 Mbps OFDM	-62 dBm	15	23	-	dB
Nonadjacent channel (± 40 MHz) rejection - IEEE 802.11n (10% PER with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	32	39	-	dB
	HT20, MCS7	-61 dBm	14	19	-	dB
Nonadjacent channel (± 80 MHz) rejection - IEEE 802.11n (10% PER with desired signal level as specified in Condition)	HT40, MCS0	-76 dBm	32	38	-	dB
	HT40, MCS7	-58 dBm	14	20	-	dB
Nonadjacent channel (± 40 MHz) rejection - IEEE 802.11ac (10% PER with desired signal level as specified in Condition)	VHT20, MCS0	-79 dBm	32	38	-	dB
	VHT20, MCS7	-61 dBm	14	21	-	dB
Nonadjacent channel (± 40 MHz) rejection - IEEE 802.11ax (10% PER with desired signal level as specified in Condition)	HE20, MCS0	-79 dBm	32	37	-	dB
	HE20, MCS9	-54 dBm	7	11	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz	-	-	-60	-	dBm
	> 1 GHz	-	-	-55	-	dBm

5.14.1.4 WLAN 5 GHz Transmitter Characteristics

Measured with $T = 25\text{ }^{\circ}\text{C}$, $V_{BAT} = 3.3\text{ V}$ unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	4900	-	5925	MHz

Parameter	Condition	Min.	Typ.	Max.	Unit
TX Power					
TX power - IEEE 802.11a (EVM compliant)	6 Mbps OFDM	-	18	-	dBm
	54 Mbps OFDM	-	16	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	17	-	dBm
	HT20, MCS7	-	15	-	dBm
	HT40, MCS0	-	15	-	dBm
	HT40, MCS7	-	13	-	dBm
TX power - IEEE 802.11ac (EVM compliant)	VHT20, MCS0	-	17	-	dBm
	VHT20, MCS7	-	15	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	17	-	dBm
	HE20, MCS9	-	13	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-55	-	dBm
	> 1 GHz	-	-45	-	dBm

5.14.2 Bluetooth LE RF Characteristics

5.14.2.1 Bluetooth LE Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-98	-	dBm
Maximum input level	30.8% PER	-	10	-	dBm
C/I co-channel	-	-	8	21	dB
C/I 1 MHz adjacent channel	-	-	1	15	dB
C/I -1 MHz adjacent channel	-	-	1	15	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I 2 MHz adjacent channel	Image frequency	-	-29	-9	dB
C/I -2 MHz adjacent channel	-	-	-30	-17	dB
C/I 3 MHz adjacent channel	Image frequency + 1 MHz	-	-30	-15	dB
C/I -3 MHz adjacent channel	-	-	-41	-27	dB
C/I > 3 MHz adjacent channel	-	-	-38	-27	dB
C/I < -3 MHz adjacent channel	-	-	-52	-27	dB
Out-of-band blocking	30–2000 MHz	-30	-	-	dBm
	2003–2399 MHz	-35	-	-	dBm
	2484–2997 MHz	-35	-	-	dBm
	3000 MHz–12.75 GHz	-30	-	-	dBm
Intermodulation	-	-	-32	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-95	-	dBm
Maximum input level	30.8% PER	-	10	-	dBm
C/I co-channel	-	-	8	21	dB
C/I 2 MHz adjacent channel	-	-	1	15	dB
C/I -2 MHz adjacent channel	-	-	-2	15	dB
C/I 4 MHz adjacent channel	Image frequency	-	-28	-9	dB
C/I -4 MHz adjacent channel	-	-	-34	-17	dB
C/I 6 MHz adjacent channel	Image frequency + 2 MHz	-	-33	-15	dB
C/I -6 MHz adjacent channel	-	-	-49	-27	dB
C/I > 6 MHz adjacent channel	-	-	-41	-27	dB
C/I < -6 MHz adjacent channel	-	-	-48	-27	dB
Out-of-band blocking	30–2000 MHz	-30	-	-	dBm
	2003–2399 MHz	-35	-	-	dBm
	2484–2997 MHz	-35	-	-	dBm
	3000 MHz–12.75 GHz	-30	-	-	dBm
Intermodulation	-	-	-31	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	-105	-	dBm
Maximum input level	30.8% PER	-	10	-	dBm
C/I co-channel	-	-	3	12	dB
C/I 1 MHz adjacent channel	-	-	-18	6	dB
C/I -1 MHz adjacent channel	-	-	-16	6	dB
C/I 2 MHz adjacent channel	Image frequency	-	-35	-18	dB
C/I -2 MHz adjacent channel	-	-	-42	-26	dB
C/I 3 MHz adjacent channel	Image frequency + 1 MHz	-	-42	-24	dB
C/I -3 MHz adjacent channel	-	-	-46	-36	dB
C/I > 3 MHz adjacent channel	-	-	-47	-36	dB
C/I < -3 MHz adjacent channel	-	-	-49	-36	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	-101	-	dBm
Maximum input level	30.8% PER	-	10	-	dBm
C/I co-channel	-	-	4	17	dB
C/I 1 MHz adjacent channel	-	-	-2	11	dB
C/I -1 MHz adjacent channel	-	-	-2	11	dB
C/I 2 MHz adjacent channel	Image frequency	-	-31	-13	dB
C/I -2 MHz adjacent channel	-	-	-31	-21	dB
C/I 3 MHz adjacent channel	Image frequency + 1 MHz	-	-33	-19	dB
C/I -3 MHz adjacent channel	-	-	-42	-31	dB
C/I > 3 MHz adjacent channel	-	-	-39	-31	dB
C/I < -3 MHz adjacent channel	-	-	-54	-31	dB

5.14.2.2 Bluetooth LE Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit	
General						
Frequency range	-	2402	-	2480	MHz	
TX power	-	-20	6	25	dBm	
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-50	-	dBm
	±3 MHz offset	-	-	-51	-	dBm
	>±3 MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf1avg	-	225	245	275	kHz
	Δf2max	-	185	230	-	kHz
	Δf2avg/Δf1avg	-	0.8	0.9	-	-
Carrier frequency offset and drift	Max f _n n = 0, 1, 2, 3...k	-	-	3	150	kHz
	Max f ₀ - f _n n = 2, 3, 4...k	-	-	2.5	50	kHz
	f ₁ - f ₀	-	-	2	23	kHz
	Max f _n - f _{n-5} n = 6, 7, 8...k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	-53	-	dBm
	±5 MHz offset	-	-	-53	-	dBm
	>±5 MHz offset	-	-	-53	-	dBm
Modulation characteristics	Δf1avg	-	450	490	550	kHz
	Δf2max	-	370	470	-	kHz
	Δf2avg/Δf1avg	-	0.8	0.9	-	-
Carrier frequency offset and drift	Max f _n n = 0, 1, 2, 3...k	-	-	3	150	kHz
	Max f ₀ - f _n n = 2, 3, 4...k	-	-	2.5	50	kHz
	f ₁ - f ₀	-	-	1.5	23	kHz
	Max f _n - f _{n-5} n = 6, 7, 8...k	-	-	2.5	20	kHz/50 μs

Parameter	Condition	Min.	Typ.	Max.	Unit	
Bluetooth LE 125 kbps						
In-band emissions	± 2 MHz offset	-	-	-49	-	dBm
	± 3 MHz offset	-	-	-51	-	dBm
	$> \pm 3$ MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf_{1avg}	-	225	245	275	kHz
	Δf_{1max}	-	185	250	-	kHz
Carrier frequency offset and drift	$\text{Max } f_n _{n=0, 1, 2, 3\dots k}$	-	-	3	150	kHz
	$\text{Max } f_0 - f_n _{n=1, 2, 3\dots k}$	-	-	2.5	50	kHz
	$ f_0 - f_3 $	-	-	1.5	19.2	kHz
	$ f_n - f_{n-3} _{n=7, 8, 9\dots k}$	-	-	3	19.2	kHz/48 μ s
Bluetooth LE 500 kbps						
In-band emissions	± 2 MHz offset	-	-	-49	-	dBm
	± 3 MHz offset	-	-	-51	-	dBm
	$> \pm 3$ MHz offset	-	-	-52	-	dBm

5.14.3 IEEE 802.15.4 RF Characteristics

5.14.3.1 IEEE 802.15.4 Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2400	-	2483.5	MHz
O-QPSK 250 kbps					
Sensitivity	1 % PER	-	-104	-	dBm
Maximum input level	1 % PER	-	10	-	dBm
Co-channel rejection	1 % PER, desired signal @ -82 dBm	-	0	-	dB
Adjacent channel (+5 MHz) rejection	1 % PER, desired signal @ -82 dBm	0	27	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
Adjacent channel (-5 MHz) rejection	1 % PER, desired signal @ -82 dBm	0	35	-	dB
Alternate channel (+10 MHz) rejection	1 % PER, desired signal @ -82 dBm	30	42	-	dB
Alternate channel (-10 MHz) rejection	1 % PER, desired signal @ -82 dBm	30	40	-	dB
Channel (+15 MHz) rejection	1 % PER, desired signal @ -82 dBm	30	44	-	dB
Channel (-15 MHz) rejection	1 % PER, desired signal @ -82 dBm	30	50	-	dB
Spurious emissions	< 1 GHz	-	-	-60	dBm
	> 1 GHz	-	-	-55	dBm

5.14.3.2 IEEE 802.15.4 Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2400	-	2483.5	MHz
O-QPSK 250 kbps					
Maximum output power	-	-20	10	20	dBm
Error-vector magnitude (EVM)	-	-	6	-	%
Center frequency tolerance	-	-	4	-	ppm
Power spectral density (PSD)	Relative, at greater than 3.5 MHz offset	-	-60	-20	dB
	Absolute, at greater than 3.5 MHz offset	-	-50	-30	dBm
Spurious emissions	< 1 GHz	-	-55	-	dBm
	> 1 GHz	-	-45	-	dBm

5.15 BK7239N Module Throughput

Test Type	Condition	Min.	Typ.	Max.	Unit
2.4 GHz					
TCP RX	-	-	27.2	-	Mbps
TCP TX	-	-	32.7	-	Mbps
UDP TX	-	-	59.2	-	Mbps
UDP RX	-	-	44.2	-	Mbps
5 GHz					
TCP RX	-	-	25.4	-	Mbps
TCP TX	-	-	33.5	-	Mbps
UDP TX	-	-	65.1	-	Mbps
UDP RX	-	-	45.4	-	Mbps

5.16 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Supply voltage	-	2.2	-	3.6	V
Conversion clock	-	1.33	-	40	MHz
Conversion time	-	-	26	-	Cycle
Sampling rate	-	0.05128	-	1.538	MHz
V_{REF}	Internal	-	1.5 or 1.8	-	V
	External	-	VIO/2	-	V
Input voltage range	ADC0	-	VBAT/4	-	V
	Other channels	0	-	$V_{REF} * 2$	V
Input impedance	-	10	-	-	MΩ
Input capacitance	-	-	4	-	pF
DNL	-	-	±0.5	-	LSB
INL	-	-	±1	-	LSB



Parameter	Condition	Min.	Typ.	Max.	Unit
ENOB	-	-	12	-	Bit
SNDR	-	-	74	-	dB
SFDR	-	-	84	-	dB
T _{STARTUP}	-	-	5	-	μs
Current consumption	-	-	1	-	mA

6 Package Information

6.1 QFN48 6 x 6 x 0.75 mm Package

Figure 6-1 QFN48 6 x 6 x 0.75 mm Package Outline

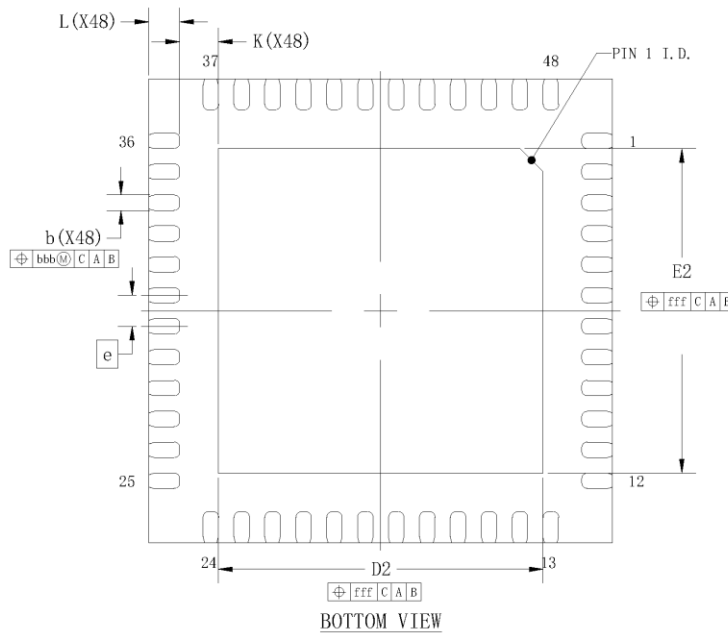
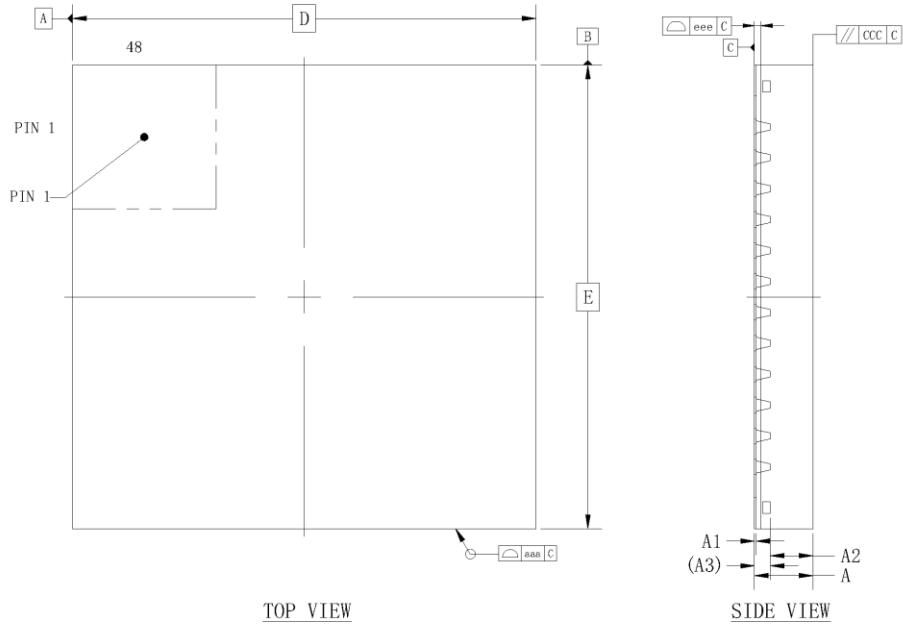




Table 6-1 QFN48 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
D2	4.10	4.20	4.30
E2	4.10	4.20	4.30
L	0.30	0.40	0.50
K	0.50 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
eee	0.08		
fff	0.10		

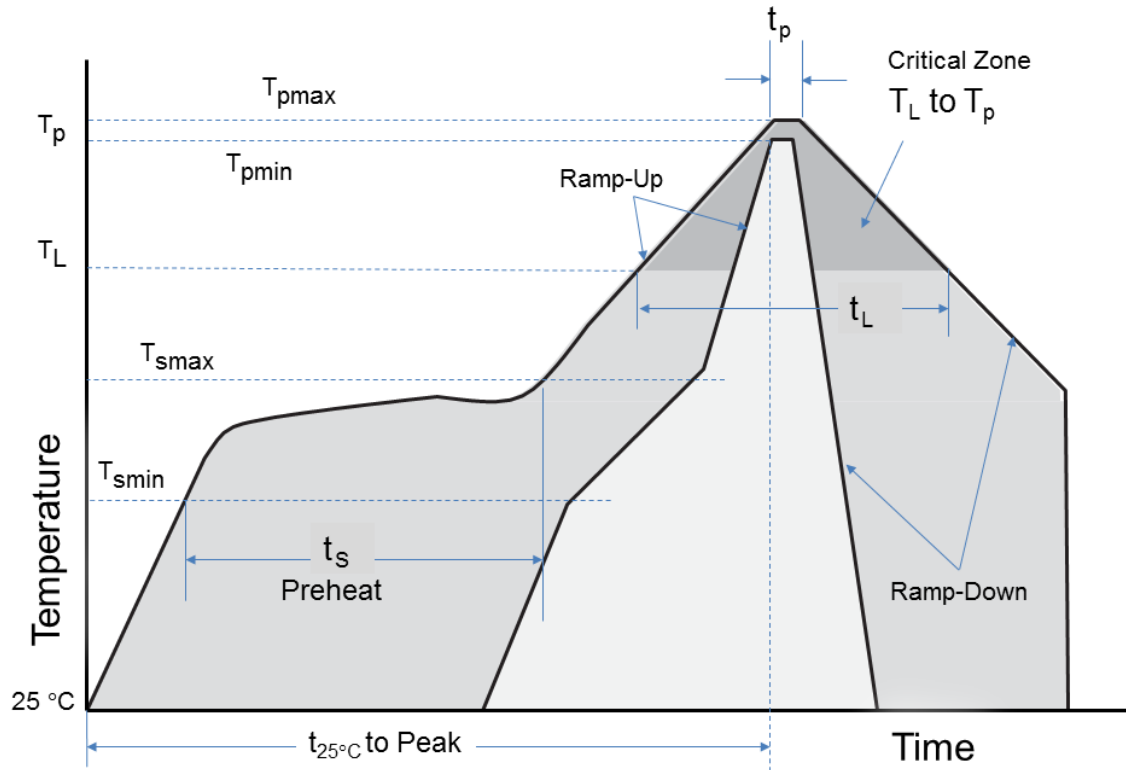


Table 6-2 QFN40 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
L	0.30	0.40	0.50
K	0.40 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

7 Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 °C/s max.
Preheat	Temperature min. (T_{smin})	150 °C
	Temperature max. (T_{smax})	200 °C
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 °C
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 °C
Time within 5 °C of actual peak temperature (t_p)		20 s to 40 s
Ramp-down rate		6 °C/s max.

Profile Feature	Specification
Time 25 °C to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.



Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.



8 Certifications and Compliance

The BK7239N is fully certified and compliant with the following industry standards. These certifications ensure seamless interoperability, robust security, and simplified integration across ecosystems.

Table 8-1 List of Certifications

Standards Organization	Certification Type	Certificate ID/DN
Wi-Fi Alliance	Wi-Fi CERTIFIED 6® (a/b/g/n/ac/ax)	WFA137794
Bluetooth SIG	Core 6.0	Q330059
Thread Group	Thread V1.4.0 (Component)	14A136
Connectivity Standards Alliance	Matter Platform 1.5	CSA26001MCPM0007-24

9 Ordering Information

Figure 9-1 Ordering Code Scheme

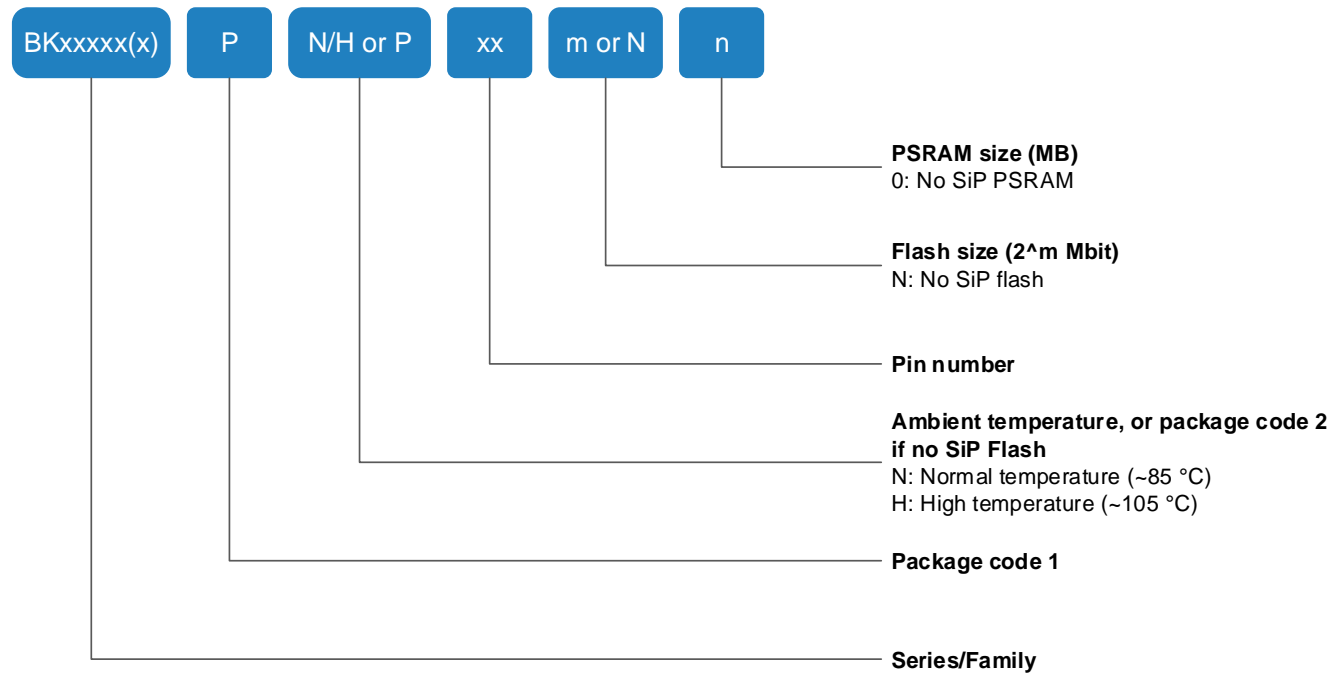


Table 9-1 Ordering Information

Ordering Code	Package	SiP ⁽¹⁾ Flash	SiP PSRAM	Low Power Consumption	Packing	Minimum Ordering Qty (MOQ) ⁽²⁾
BK7239NQN48N8	6 mm x 6 mm x 0.75 mm QFN48	-	8 MB	Yes	Tape and Reel	3000



Ordering Code	Package	SiP ⁽¹⁾ Flash	SiP PSRAM	Low Power Consumption	Packing	Minimum Ordering Qty (MOQ) ⁽²⁾
BK7239NQN4050	5 mm x 5 mm x 0.75 mm QFN40	4 MB	-	-	Tape and Reel	3000
BK7239NQH4050	5 mm x 5 mm x 0.75 mm QFN40	4 MB	-	-	Tape and Reel	3000
BK7239NLQN4050	5 mm x 5 mm x 0.75 mm QFN40	4 MB	-	Yes	Tape and Reel	3000
BK7239NLQN4060	5 mm x 5 mm x 0.75 mm QFN40	8 MB	-	Yes	Tape and Reel	3000
BK7239NLQN4064	5 mm x 5 mm x 0.75 mm QFN40	8 MB	4 MB	Yes	Tape and Reel	3000

(1) A system in a package (SiP) refers to flash/PSRAM enclosed in the package.

(2) The MOQ for customized or exclusive ordering codes is one wafer lot. Please consult your sales representative for the exact quantity.

Revision History

Version	Date	Description
1.0	2024/6/27	Initial release
1.1	2024/8/19	<ul style="list-style-type: none"> Added Wi-Fi 6E support Added IEEE 802.15.4 features and updated current values in Section 1 Features Added QFN48 package Updated the name of pin 5 for the QFN56 package in Section 3 Pin Descriptions Updated the description of Section 4.6 RF Transceivers Updated the description of Section 4.9 Reset Updated VDDA voltage and VDDDIG voltage in Figure 4-6 in Section 4.10.1 Power Scheme Update the description of sleep mode in Section 4.10.3 Power Modes Updated UART baud rate in Section 4.15 UART Interfaces (UART) Updated the maximum voltage of VCCIF, VCCR XFE, VCCPLL_2G, VCCPLL_5G, VCCA, VDDA, and VDDDIG in Section 5.1 Absolute Maximum Ratings Added the typical voltage of VCCIF, VCCR XFE, VCCPLL_2G, VCCPLL_5G, VCCA, VDDA, and VDDDIG in Section 5.3 Recommended Operating Conditions Updated VDDA (LDO output) typical voltage in Section 5.6 Analog LDO Updated VDDDIG typical voltage in Section 5.7 Core LDO Updated VDDA (buck output) typical voltage in Section 5.9 Analog Buck Updated the load capacitance and trim sensitivity of the 40 MHz crystal in Section 5.11 40 MHz Crystal Characteristics Updated and added current values in Section 5.13 Current Consumption Updated and added RF characteristics values in Section 5.14.1 WLAN RF Characteristics
1.2	2025/4/29	<ul style="list-style-type: none"> Removed Wi-Fi 6 GHz band support and Wi-Fi 6E support Added support of 40 MHz channel bandwidth for 2.4 GHz and 5 GHz Updated SRAM size Updated maximum VBAT voltage

Version	Date	Description
		<ul style="list-style-type: none"> • Removed QFN56 package and updated QFN48 package pin assignments • Updated maximum operating temperature • Updated I/O pin multiplexing in Section 3.4 Pin Multiplexing • Changed the heading of Section 4.5 to IEEE 802.15.4 Overview • Updated the description of watchdog reset in Section 4.9 Reset • Updated Section 4.10.1 Power Scheme • Modified the description of wake-up sources for deep sleep and sleep modes in Section 4.10.3 Power Modes • Added Section 4.11 I/O Multiplexer (IOMUX) • Updated the description of Section 4.12 General-purpose I/Os (GPIO) • Added the description of UART0 flash download in Section 4.15 UART Interfaces (UART) • Updated the introduction to PWM module in Section 4.20 PWM Module (PWM) • Section 4.22 Auxiliary ADC (AUX ADC): <ul style="list-style-type: none"> – Updated conversion modes – Updated sampling rate range – Updated external analog input channels and internal channels • Updated Section 5.1 Absolute Maximum Ratings • Updated Section 5.3 Recommended Operating Conditions • Updated the minimum value of V_{OH} in Section 5.4 Digital I/O Characteristics • Added Section 5.5 IO LDO • Updated V_DDA (LDO output) typical voltage in Section 5.6 Analog LDO • Updated V_DDA (buck output) typical voltage in Section 5.9 Analog Buck • Updated Section 5.13 Current Consumption • Updated Section 5.14.1 WLAN RF Characteristics • Updated conversion clock and external V_{REF} voltage for AUX ADC in Section 5.16 AUX ADC Characteristics • Section 9 Ordering Information: <ul style="list-style-type: none"> – Updated the title of Figure 9-1 – Updated ordering code – Added a note about MOQ in Table 9-1
1.3	2025/6/17	<ul style="list-style-type: none"> • Updated Section 5.13 Current Consumption • Updated Section 5.14.1 WLAN RF Characteristics

Version	Date	Description
1.4	2025/6/27	<ul style="list-style-type: none"> • Section 1 Features: <ul style="list-style-type: none"> – Added description for 802.11ax MCS support – Added description for flash XIP support – Updated current values • Added QFN40 package • Updated maximum operating temperature • Corrected WDT clock source in Section 4.24 Watchdog Timer (WDT) • Corrected RTC clock sources in Section 4.25 Real-time Counter (RTC) • Corrected VDDDIG maximum voltage rating to 1.1 V in Section 5.1 Absolute Maximum Ratings • Updated I/O output current values in Section 5.4 Digital I/O Characteristics • Added Section 5.8 EXMEM LDO • Updated Section 5.13 Current Consumption • Added sensitivity values for 802.11ax HE20 MCS8 and MCS9 in Section 5.14.1.1 WLAN 2.4 GHz Receiver Characteristics and Section 5.14.1.3 WLAN 5 GHz Receiver Characteristics • Added TX power value for 802.11ax HE20 MCS9 in Section 5.14.1.4 WLAN 5 GHz Transmitter Characteristics • Updated Bluetooth LE maximum TX power in Section 5.14.2.2 Bluetooth LE Transmitter Characteristics • Added certain 802.15.4 RF characteristics values in Section 5.14.3.1 IEEE 802.15.4 Receiver Characteristics and 5.14.3.2 IEEE 802.15.4 Transmitter Characteristics
1.5	2025/7/24	<ul style="list-style-type: none"> • Changed the maximum MCU frequency in Section 1 Features • Corrected AUX ADC resolution in Section 1 Features and Section 2 Overview • Updated values for T₂, T₃, and T₄ in Table 4-2 Timing Parameters of Power-up Sequence in Section 4.10.1 Power Scheme • Updated the maximum baud rate of the UART interfaces in Section 4.15 UART Interfaces (UART) • Added I2C Fast-mode Plus feature in Section 4.17 I2C Interfaces (I2C) • Added the description of dedicated hardware support for LED dimming/fading for the PWM module in Section 4.20 PWM Module (PWM) • Corrected the resolution, sampling rate range, and description of VBAT channel for the AUX ADC in Section 4.22 Auxiliary ADC (AUX ADC)

Version	Date	Description
		<ul style="list-style-type: none"> Updated values of load capacitance and trim sensitivity for 40 MHz crystal in Section 5.11 40 MHz Crystal Characteristics Added Section 5.12 32.768 kHz Crystal Characteristics Updated AUX ADC Characteristics values in Section 5.16 AUX ADC Characteristics
1.6	2025/8/29	<ul style="list-style-type: none"> Added 802.11ac support Section 5.14 RF Characteristics: <ul style="list-style-type: none"> Added a note regarding RF measurement conditions and the front-end circuit Updated and added some characteristics values
1.7	2025/12/29	<ul style="list-style-type: none"> Added BK7239N QFN40 and BK7239NL QFN40 packages Updated the minimum operating voltage to 2.2 V Updated Section 1 Features Updated Section 2 Overview Updated the clock signal names and clock description Section 3.4 Pin Multiplexing <ul style="list-style-type: none"> Added a note regarding the usage of specific GPIOs Added I/O pin predefined states at reset and after reset Added the description of GPIO WKUP function in Section 3.4.3 Pin Multiplexing of Analog Functions Added Section 4.1 Arm STAR-MC1 Processor to Section 4.4 Bluetooth LE Subsystem Changed the heading of Section 4.5 to IEEE 802.15.4 PHY and MAC Revised the description of reset behavior triggered by wake-up in Section 4.9 Reset Section 4.10.1 Power Scheme <ul style="list-style-type: none"> Revised the description of VBAT and VDDRAM Revised Figure 4-7 BK7239N Power-up Sequence and updated values in Table 4-2 Timing Parameters of Power-up Sequence Revised Figure 4-8 BK7239N Power-down Sequence and updated values in Table 4-3 Timing Parameters of Power-down Sequence Updated the voltages of VDDA, VCCIF, VCCRFXFE, and VCCPLL_5G Added Section 4.10.2 Power Supply Supervisor Revised the description of shutdown, deep sleep, and sleep modes in Section 4.10.3 Power Modes Added support for configurable VIO or VDDRAM supply for GPIOs in Section 4.12 General-purpose I/Os (GPIO)

Version	Date	Description
		<ul style="list-style-type: none"> • Added GMDA features in Section 4.18 GDMA Controller (GDMA) • Corrected the description of internal dedicated channels for AUX ADC in Section 4.22 Auxiliary ADC (AUX ADC) • Removed note “Values currently listed in this section are objective data and are subject to change.” from Section 5 Electrical Characteristics • Added Section 5.2 ESD Ratings • Added Schmitt-trigger input voltages to Section 5.4 Digital I/O Characteristics • Revised test conditions of trim sensitivity for 40 MHz crystal in Section 5.11 40 MHz Crystal Characteristics • Added and updated current values to Section 5.13 Current Consumption • Updated and added some characteristics values in Section 5.14 RF Characteristics • Added Section 5.15 BK7239N Module Throughput • Added parameters and updated values for AUX ADC in Section 5.16 AUX ADC Characteristics
1.8	2026/1/28	<ul style="list-style-type: none"> • Specified part-specific availability for the buck converter • Added Table 2-1 Device Options and Features to Section 2 Overview • Updated BK7239N QFN40 pinout (pins 33 and 34 changed) • Updated Figure 4-6 Internal Power Distribution in Section 4.10.1 Power Scheme • Updated RF characteristics in Section 5.14 RF Characteristics • Added Section 8 Certifications and Compliance

Copyright

© 2026 Beken Corporation. The term “Beken” refers to Beken Corporation and/or its affiliates. This document contains information that is proprietary to Beken. Any unauthorized use, reproduction, or disclosure of this document in whole or in part is prohibited.

Disclaimer

The documentation is provided on an "as-is" basis only. Beken reserves the right to make any updates, corrections and any other modifications to its documentation without further notice and limitation to product information, descriptions, and specifications herein. Beken does not give warranties as to the accuracy or completeness of the included information. Beken shall have no liability for any use of the information in this documentation. You should obtain the latest relevant information before placing orders and should verify that such information is current and complete. Information published by Beken regarding any third-party products does not constitute a license to use such products or a warranty or endorsement thereof. Use of such information may require a license from a third party under the intellectual property rights of such third party, or a license from Beken under the intellectual property rights of Beken.

Trademarks

Beken, the BEKEN logo, and combinations thereof are trademarks or registered trademarks of Beken. All other product or brand names mentioned herein are trademarks or registered trademarks of their respective holders.



Beken Corporation

Building 41, 1387 Zhangdong Rd
Shanghai 201203
China

<http://www.bekencorp.com>