

General Description:

The LWP2015AD2 uses trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is DFN2*2-6L, which accords with the ROHS standard and Halogen Free standard.

Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Applications:

- Battery switching application
- Hard switched and high frequency circuits
- Power Management

100% DVDS Tested

100% Avalanche Tested



Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
P2015AD2/D.C.	LWP2015AD2	DFN2*2-6L	Reel	3000 Pcs

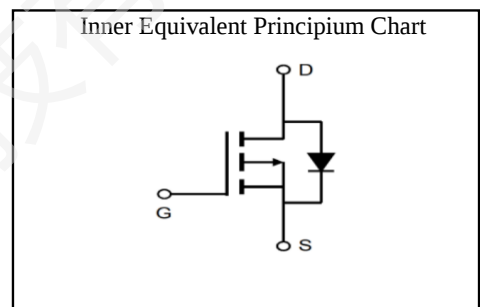
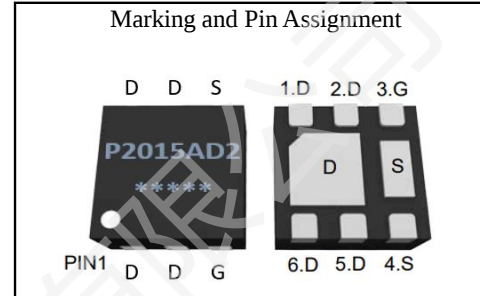
Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-20	V
I_D	Continuous Drain Current	$T_C=25^{\circ}C$	-25	A
	Continuous Drain Current	$T_C=100^{\circ}C$	-16	A
I_{DM}^{a1}	Pulsed Drain Current		-100	A
E_{AS}^{a2}	Single pulse avalanche energy		144	mJ
V_{GS}	Gate-to-Source Voltage		± 10	V
P_D	Power Dissipation		18	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	$^{\circ}C$
T_L	Maximum Temperature for Soldering		260	$^{\circ}C$

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6.9	$^{\circ}C/W$
$R_{\theta JA}^{a3}$	Thermal Resistance, Junction-to-Ambient	50	$^{\circ}C/W$

V_{DSS}	-20	V
I_D	-25	A
P_D	18	W
$R_{DS(ON) \text{ TYPE}}$	9.5	$m\Omega$



Electrical Characteristic ($T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified):

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=-20V, V_{GS}=0V$	--	--	-1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=-10V, V_{DS}=0V$	--	--	-100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=+10V, V_{DS}=0V$	--	--	100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.6	-1.0	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	$V_{GS}=-4.5V, I_D=-10A$	--	9.5	13	$m\Omega$
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	$V_{GS}=-2.5V, I_D=-8.0A$	--	12.5	17	$m\Omega$

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V$	--	1962	--	pF
C_{oss}	Output Capacitance	$V_{DS}=-10V$	--	298	--	
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	--	294	--	
R_G	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	--	10	--	Ω

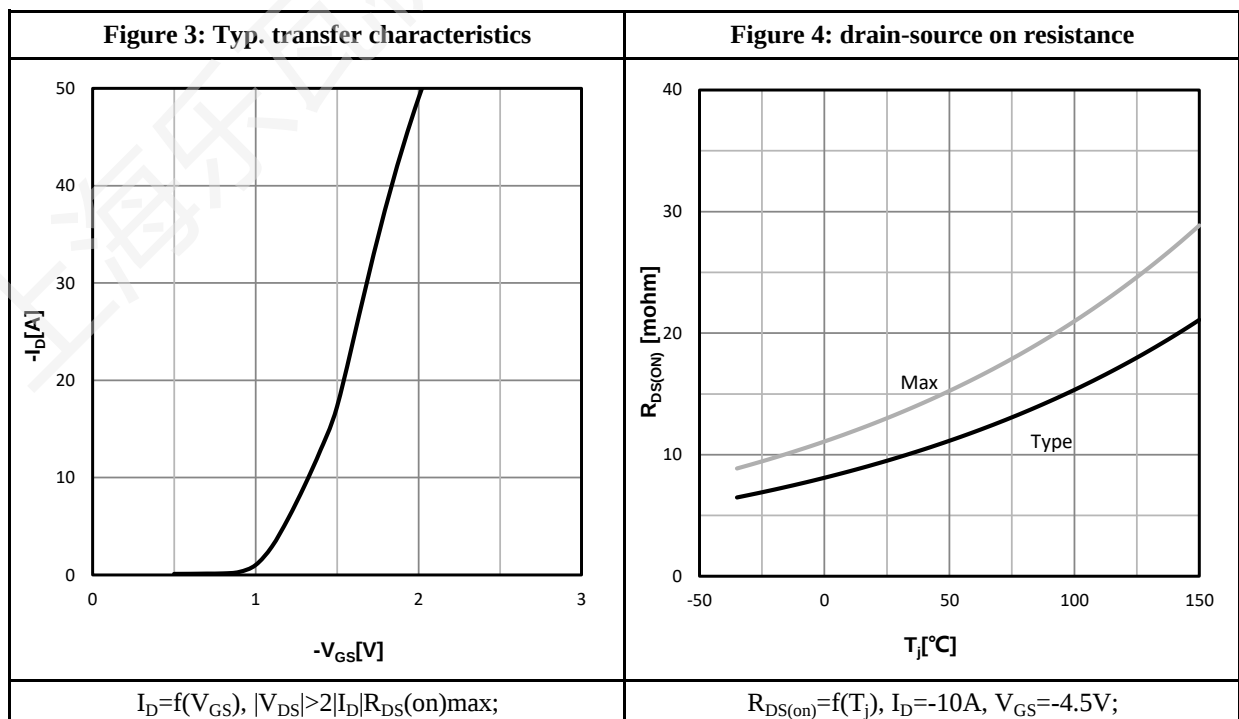
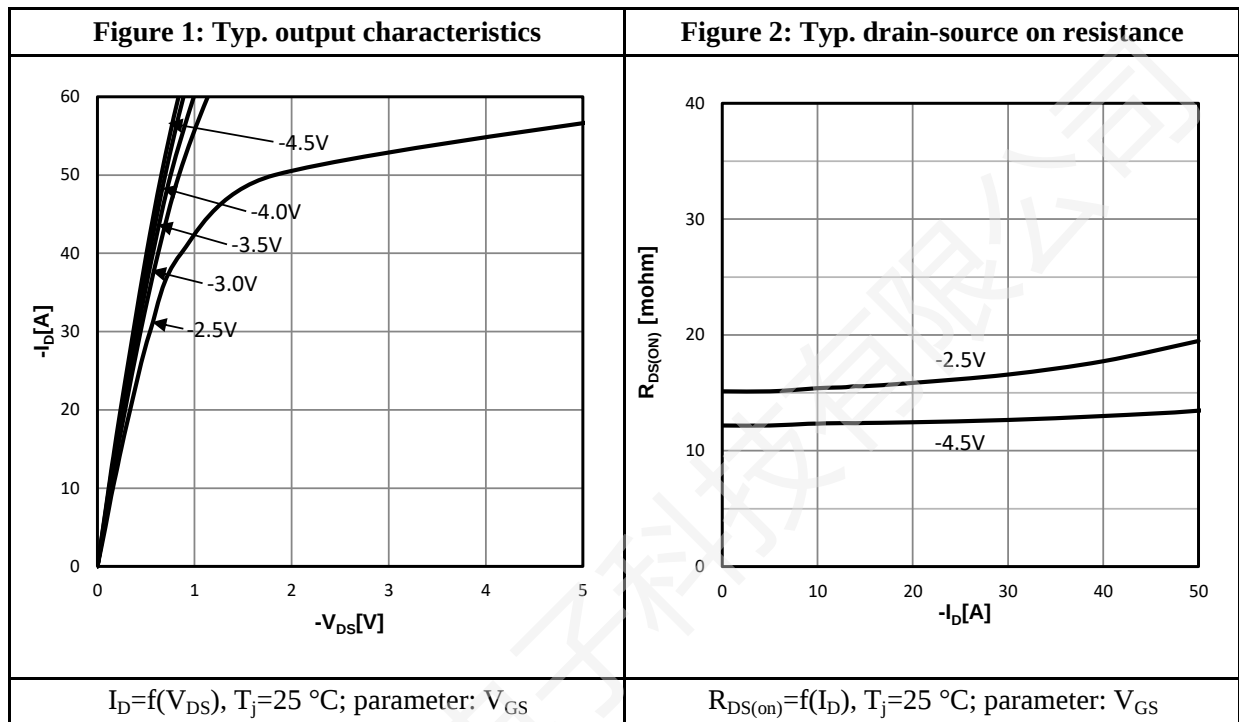
Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=-10A$	--	10	--	ns
t_r	Rise Time	$V_{DS}=-10V$	--	35	--	
$t_{d(OFF)}$	Turn-Off Delay Time	$V_{GS}=-4.5V$	--	27	--	
t_f	Fall Time	$R_G=1.0\Omega$	--	11	--	
Q_g	Total Gate Charge	$V_{GS}=-4.5V$	--	27	--	nC
Q_{gs}	Gate to Source Charge	$V_{DS}=-10V$	--	3.4	--	
Q_{gd}	Gate to Drain Charge	$I_D=-10A$	--	6.4	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	$T_C=25\text{ }^{\circ}\text{C}$	--	--	-25	A
V_{SD}	Diode Forward Voltage	$I_S=-10A, V_{GS}=0V$	--	--	-1.2	V

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $V_{DD}=-15V, L=0.5mH, R_G=25\Omega$, Starting $T_j=25^{\circ}\text{C}$

a3: Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection.

Characteristics Curve:


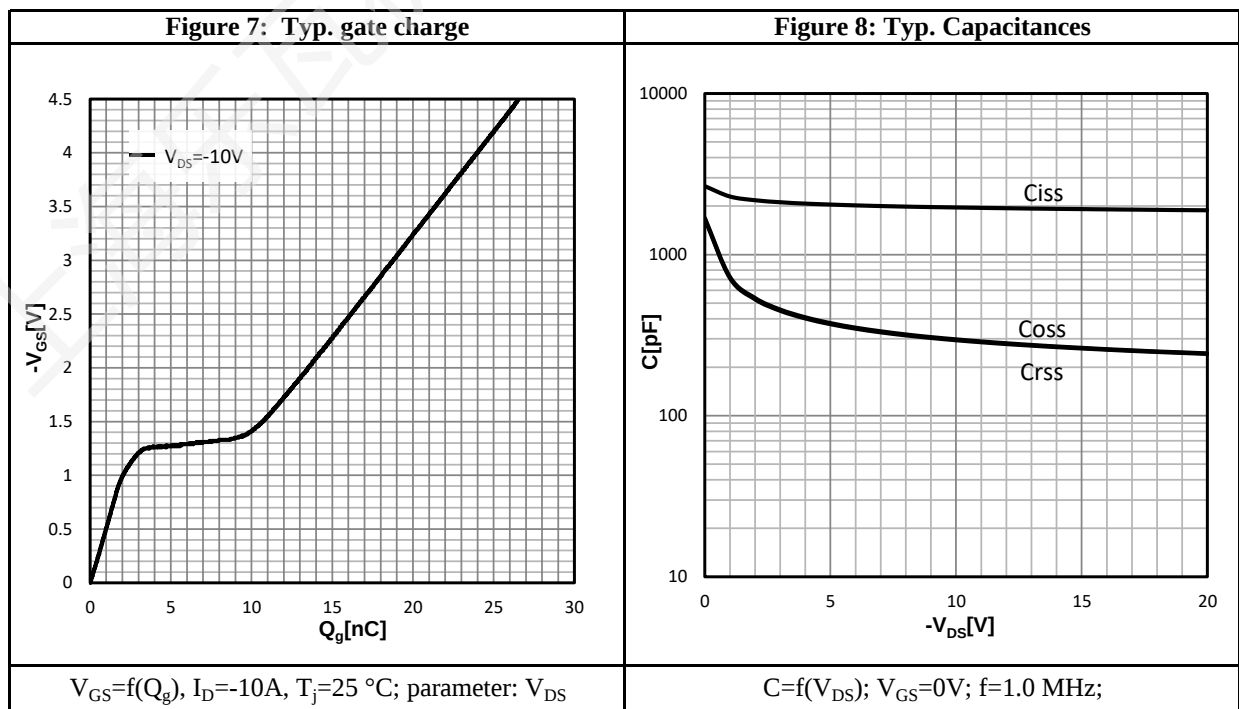
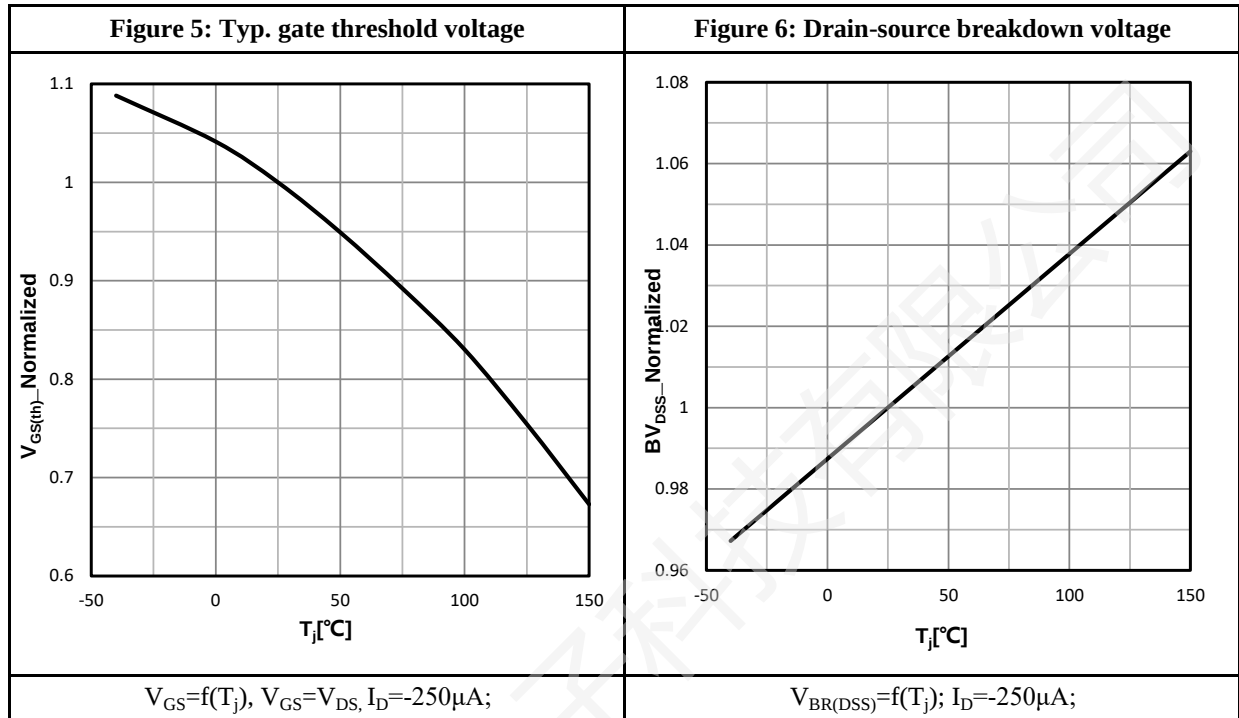
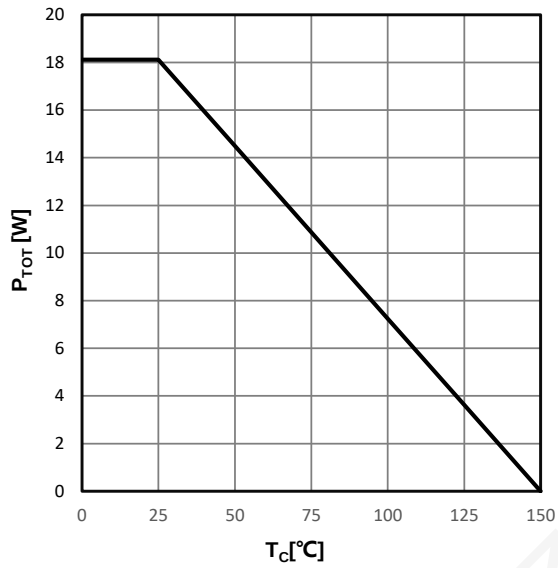
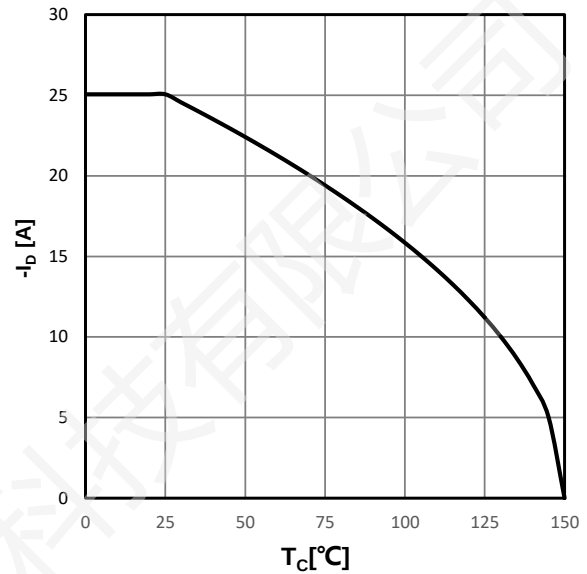
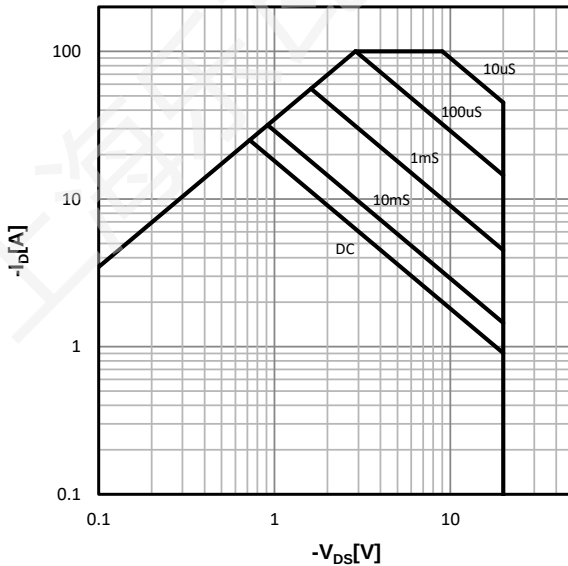


Figure 9: Power dissipation


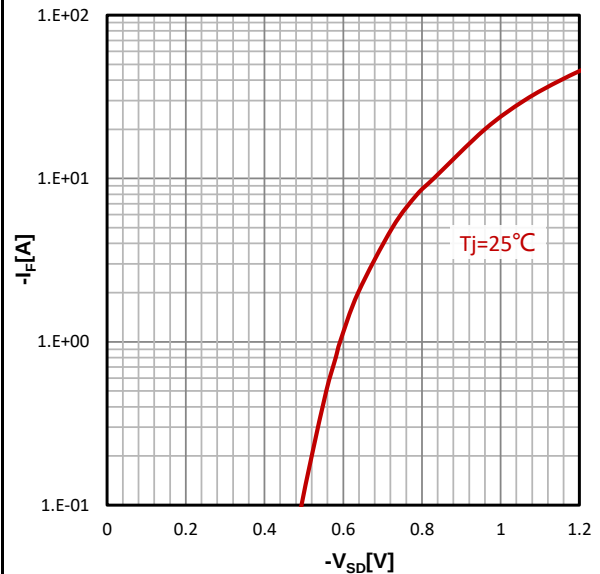
$$P_{tot}=f(T_C);$$

Figure 10: Drain current


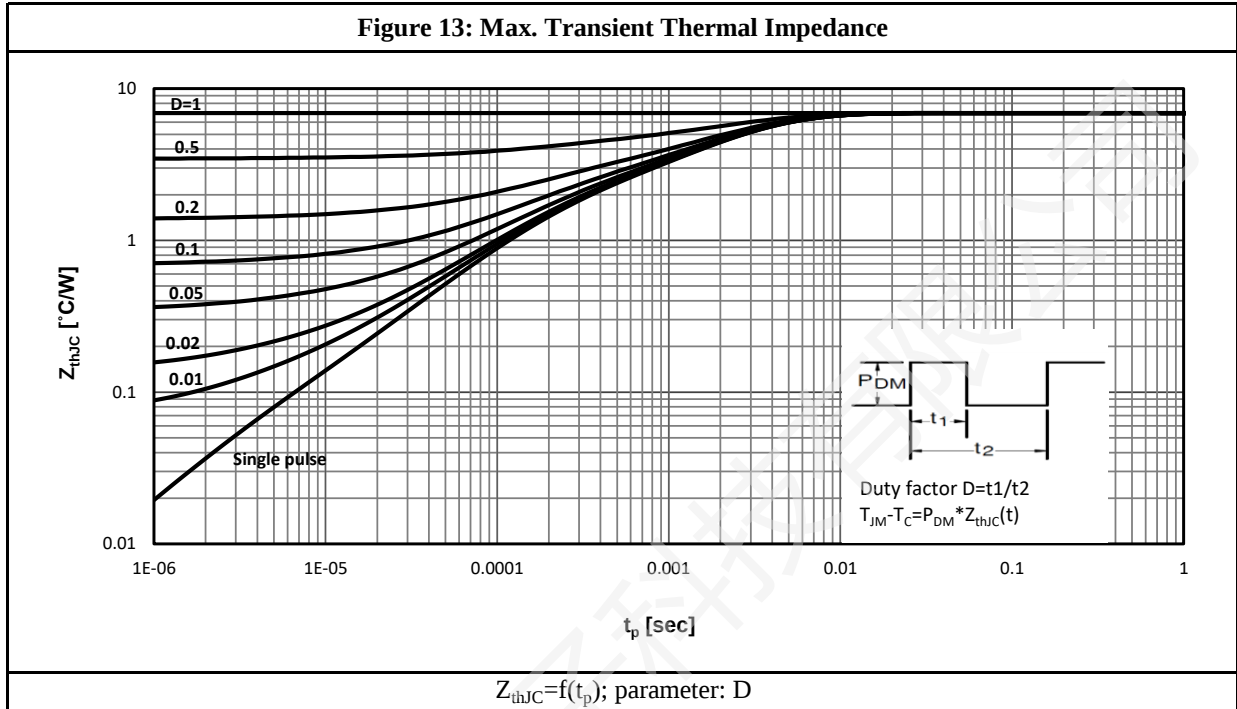
$$I_D=f(T_C);$$

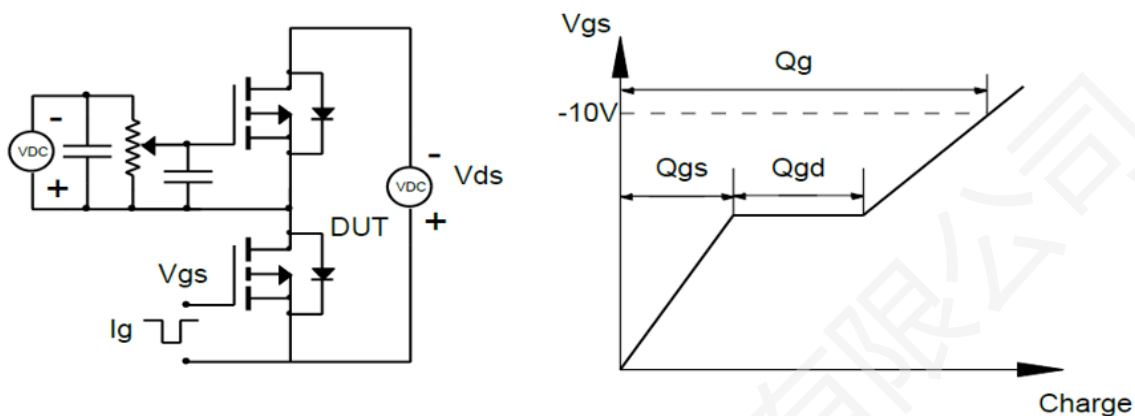
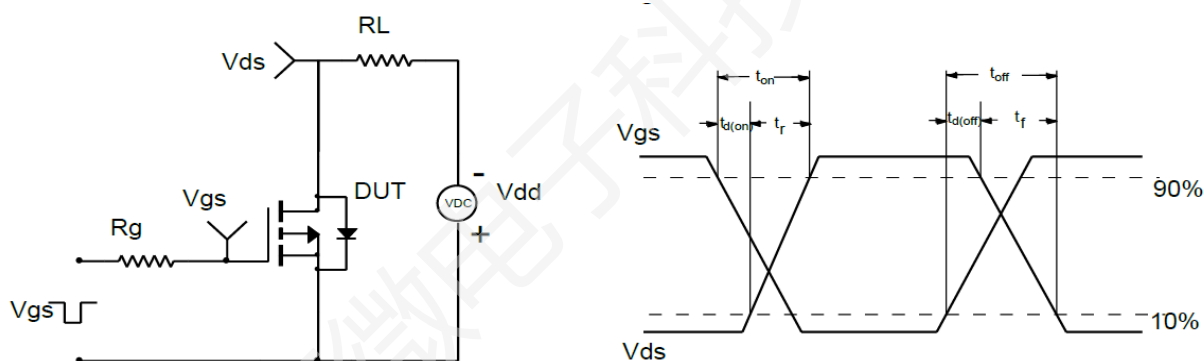
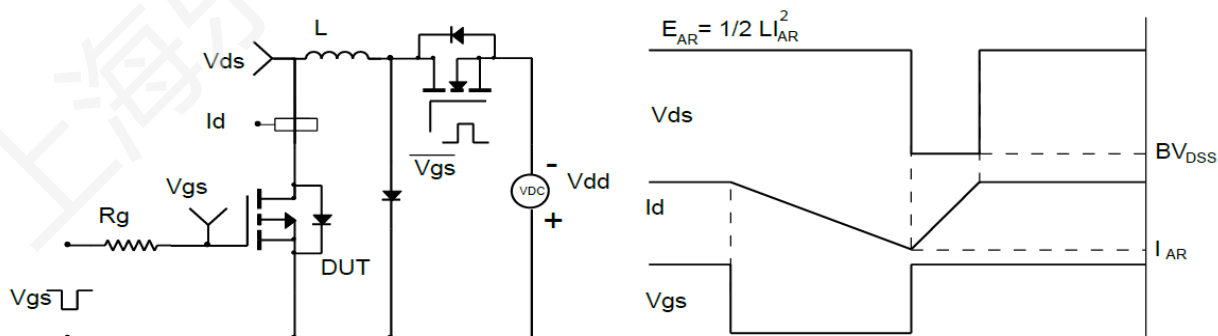
Figure 11: Safe operating area


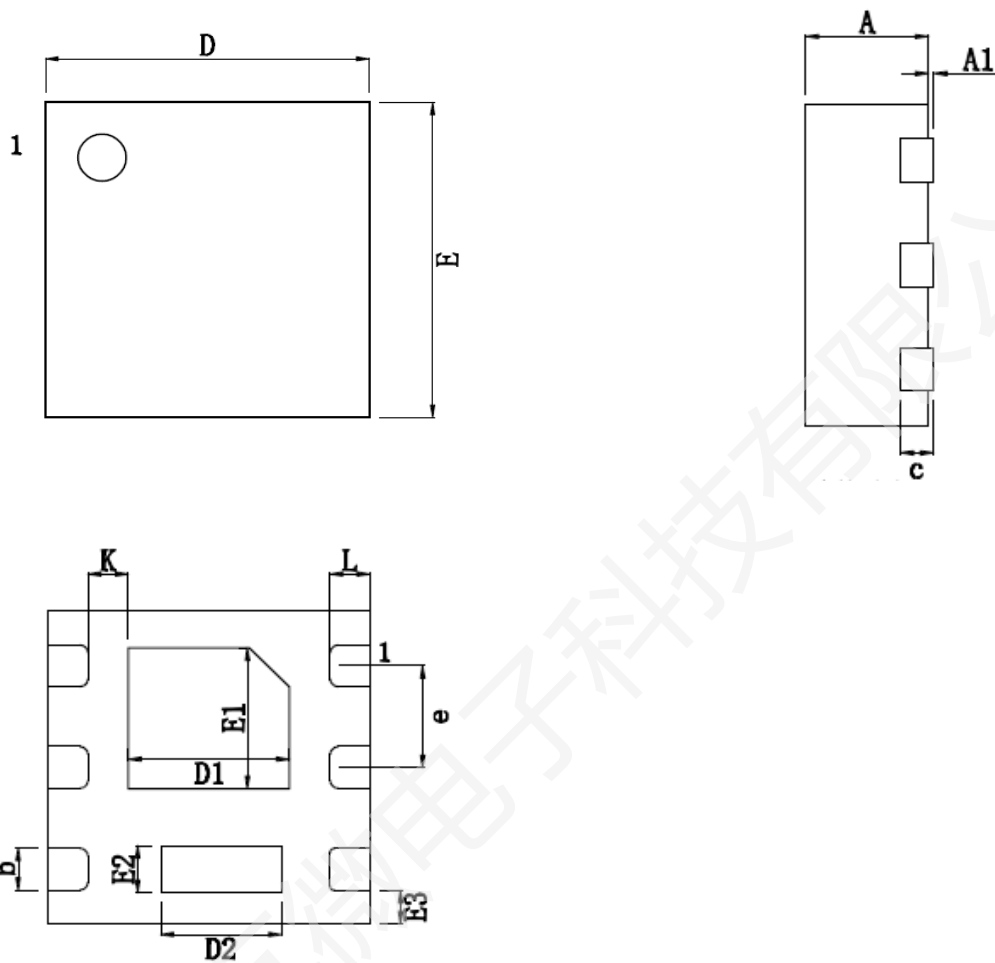
$$I_D=f(V_{DS}); T_C=25\text{ }^{\circ}\text{C}; D=0; \text{parameter: tp}$$

Figure 12: Typ. forward characteristics


$$I_F=f(V_{SD});$$

Figure 13: Max. Transient Thermal Impedance


Test Circuit & Waveform:

Figure 14: Gate Charge Test Circuit & Waveform

Figure 15: Resistive Switching Test Circuit & Waveforms

Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:


SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.22	0.29	0.35
c	0.203 TYP		
D	1.95	2.00	2.05
D1	0.90	1.00	1.10
D2	0.55	0.70	0.85
E	1.95	2.00	2.05
E1	0.80	0.90	1.00
E2	0.25	0.30	0.35
E3	0.215 REF		
e	0.65 BSC		
K	0.25 REF		
L	0.20	0.25	0.30

Revision History:

Revison	Date	Descriptions
Rev 1.0	July.2025	Initial Version

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