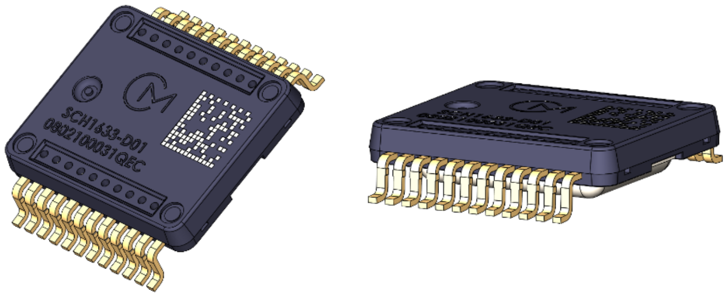
SCH1633 Data Sheet



SCH1600 Series: 6-DOF XYZ-Axis Gyroscope and xyz-Axis Accelerometer with digital SPI interface

Features

- ±300°/s calibrated angular rate measurement range.
  - Selectable measurement range options from ±300°/s down to ±62.5°/s
- ±80m/s² calibrated acceleration measurement range
  - Selectable measurement range options from ±80m/s² down to ±15m/s²
- Redundant digital accelerometer channel with up to ±260m/s² dynamic range
- Options for output interpolation and decimation
- Option for several rate and acceleration filters
- Data Ready output, timestamp index and SYNC input functions for clock domain synchronization.
- -40...110°C operating temperature range
- 3.0...3.6V supply voltage, 1.7…3.6V I/O supply
- SafeSPI v2.0 interface
- 20bit and 16bit output data, selectable via SPI frame
- Extensive self-diagnostic features
- 12mm x 14mm x 3mm (l x w x h) SOIC-24 inverted housing with <170mm² footprint on PCB.
- Qualified according to AEC-Q100 standard
- ISO26262 compliant, ASIL-D for common cause failures

Applications

SCH1600 series is targeted at applications demanding high performance and functional safety with tough environmental requirements. Typical applications include:

- Advanced Driver Assistance Systems
- Automated Driving (AD)
- Inertial Navigation
- Advanced Vehicle Stability Control Systems
- Dynamic Leveling

Restriction

- https://www.murata.com/en-global/support/militaryrestriction

Overview

The SCH1600 is a combined high-performance 3-axis angular rate and 3-axis accelerometer. The angular rate and accelerometer sensor elements are based on Murata's proven capacitive 3D-MEMS technology. Signal processing is done by a single mixed-signal ASIC that provides angular rate via a flexible SafeSPI v2.0 compliant digital interface. Sensor elements and ASIC are packaged to pre-molded SOIC 24-pin plastic housing that guarantees reliable operation over the product's lifetime.

The SCH1600 is designed, manufactured, and tested for high stability, reliability, and quality requirements. The component has extremely stable output over temperature, humidity, and vibration. It is qualified according to the AEC-Q100 standard and has several advanced self-diagnostic features. The component is suitable for SMD mounting and is compatible with RoHS and ELV directives

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TABLE OF CONTENTS

1 Introduction

This document contains essential technical information about the SCH1600 sensor including specifications, SPI interface descriptions, user-accessible register details, electrical properties, and application information. This document should be used as a reference when designing in SCH1600 component.

2 Product Types and order code with packing quantity

Table 1 Product Types and Order codes

Product Type	Description	Packing	Quantity
SCH1633-B01-004	Gyro ±300dps, Accelerometer ±80m/s2	Sample package, Bulk	4pcs
SCH1633-B01-1	Gyro ±300dps, Accelerometer ±80m/s2	Tape & Reel	100pcs
SCH1633-B01-10	Gyro ±300dps, Accelerometer ±80m/s2	Tape & Reel	1000pcs

3 Specifications

3.1 Definition of Critical Characteristics

Product or process characteristics which affect regulatory compliance or safe product function. Even a small exceeding of the tolerances is safety critical. Process capabilities must be continuously monitored. If the process is not capable enough (CPK < 2.0), 100% measurement or inspection must be applied (excluding lifetime effects).

3.2 Definition of Significant Characteristics

Product or process characteristics where reduction in variation within the specification tolerance is in manufacturers own interest or affects significantly customer satisfaction. The product or process characteristics are not, however, safety critical, unless the tolerances are exceeded significantly. Process capabilities must be continuously monitored. If the process is not capable enough (CPK <1.67), 100% measurement or inspection must be applied (excluding lifetime effects).

3.3 Abbreviations

ACC	Accelerometer
ARS	Angular Rate Sensor
ASIC	Application Specific Integrated Circuit
CC	Critical Characteristic
CS	Chip Select
CPK	Process Capability Index
DPS	Degrees Per Second
DRY	Data Ready
F_PRIM	Gyro Primary Frequency
FHTI	Fault Handling Time Interval
FREQ	Frequency
LPM	Low Power Mode
LPF	Low-Pass Filter
MCU	Microcontroller
MEMS	Micro-Electro Mechanical System
MISO	Master In Slave Out
MOSI	Master Out Slave In
RT	Room Temperature
SC	Significant Characteristic
SCK	Serial Clock
SPFM	Single Point Fault Metrics
SPI	Serial Peripheral Interface
SYNC	Synchronization

3.4 General specifications

General specifications for SCH1600 series component are presented in table below.

Table 2 General specifications for SCH1600 series

Title	Classification	Min	Nom	Max	Unit
Operating Temperature		-40		110	°C
Supply Voltage		3.0	3.3	3.6	V
Digital I/O supply		1.7		3.6	V
Total Supply Current	CC	36	41	47	mA
Low Power Mode current consumption				10	mA
Gyro Primary Frequency, F_PRIM		22.1	23.6	25.1	kHz
Output update rate - Interpolated outputs (F_PRIM x 16)		353.6	377.6	401.6	kHz
Output update rate - Decimated outputs			F_PRIM/X(1		kHz
Turn-on-time(2				250	ms

1) Decimation ratio X is selectable from the following options: 2, 4, 8, 16 and 32
2) After voltage supplies are within specification

3.5 Absolute Maximum ratings

Within the maximum ratings, no damage to the component shall occur. Parametric values may deviate from specification, yet no functional deviation shall occur. All voltages are related to the potential at GND.

Table 3 Absolute Maximum ratings

Title	Foot Note	Min	Nom	Max	Unit
Supply voltage	Supply voltage (pins 3P3, VDDIO)	-0.3		3.63	V
Voltage at Analog input/output pins		-0.3		3.63	V
Voltage at Digital input/output pins		-0.3		3.63	V
Storage Temperature	Within these maximum ratings no damage to the component shall occur in an instant or up to max 24hours	-50		150	°C
ESD_HBM	ESD according to Human Body Model (HBM), Q100-002	2000			V
ESD_CDM center pins	Center pins ESD according to Charged Device Model (CDM), Q100-011	500			V
ESD_CDM corner pins	corner pins ESD according to Charged Device Model (CDM), Q100-011	750			V
Ultrasonic agitation	Cleaning, welding, etc.		Prohibited		

3.6 Performance Specifications for Gyroscope (ARS)

Table 4 Performance Specifications for Gyroscope are valid for measurement range and over specified supply voltage at room temperature unless otherwise specified

Title	Condition	SC CC	Min	Nom	Max	Unit
Measurement range[A)]	Measurement axes XYZ, default sensitivity setting				±300	°/s
	Measurement axes XYZ, highest selectable sensitivity setting		±62.5			°/s
Mechanical range			2000			°/s
Total Offset Error[B)]	XY axis, -40 °C ... +110 °C	CC	-2		2	°/s
	Z axis, -40 °C ... +110 °C	CC	-1		1	°/s
Offset Drift Over Temperature[C)]	XY axis, -40 °C ... +110 °C		0		0.5	°/s
	Z axis, -40 °C ... +110 °C		0		0.25	°/s
Offset Drift Velocity[D)]	-40 °C ... +110 °C, 0.5K/min 2.5K/min		-0.1	±0.02	0.1	(°/s)/min
Repeatability Over Time[E)]	-40 °C ... +110 °C		-0.1		0.1	°/s
Default Sensitivity - 16bit mode[F)]	16 bits in 2's complement format			100		LSB/°/s
Default Sensitivity - 20bit mode[F)]	20 bits in 2's complement format			1600		LSB/°/s
Total Sensitivity Error[G)]	XY axis, -40 °C ... +110 °C	CC	-1.5		1.5	%
	Z axis, -40 °C ... +110 °C	CC	-1.5		1.5	%
Linearity Error[H)]	XYZ axis, ±300°/s, -40 °C ... +110 °C		-0.5		0.5	°/s
	XYZ axis, ±20°/s, -40 °C ... +110 °C		-0.05		0.05	°/s
Micro Linearity[I)]	Step width ≥2.5°/s		-5		5	%
Output RMS Noise LPF2[J)]	-40 °C ... +110 °C	CC		0.003	0.01	°/s
Output RMS Noise LPF1[J)]	-40 °C ... +110 °C	CC		0.005	0.015	°/s
Output RMS Noise LPF0[J)]	-40 °C ... +110 °C	CC		0.006	0.02	°/s
Noise density[K)]	-40 °C ... +110 °C			0.7		mdps/√Hz
Angle Random Walk[L)]				0.025		°/√h
Bias Instability[M)]	Allan Variance minimum divided by 0.664			1		°/h
Orthogonality Error (between rate axis')[N)]	-40 °C ... +110 °C		-0.2		0.2	deg
Orthogonality Error (between rate/acc axis')[O)]	-40 °C ... +110 °C		-0.5		0.5	deg
Cross-Axis Sensitivity[P)]	Absolute cross axis error, -40 °C ... +110 °C	SC	-1.7		1.7	%
G-sensitivity[Q)]	For DC gravity input		-0.01		0.01	°/s/(m/s²)

- Specification is valid after 24hours from reflow.
- Each system design including SCH1600 Series components must be evaluated by the customer in advance to guarantee proper functionality during operation.

Table 5 Foot notes for Gyroscope performance specification

Symbol	Foot Note
A)	Measurement range is tied to Electrical headroom and is selectable from predefined options presented in table 61. Changing electrical headroom affects only signal path sensitivity (LSB/°/s) (up to 4x). Increasing sensitivity decreases electrical headroom respectively (up to 1/4x). Max value is indicating measurement range for given product variant where specification is at least valid to. Min value is indicating lowest measurement range the signal can be scaled to by sensitivity setting and in which specification is valid.
B)	Sensor's absolute offset shall remain in specified limits in static measurement environment despite of changes resulting from temperature, supply voltage and lifetime effects.
C)	Offset drift over temperature is determined by [(maximum offset value over temperature) - (minimum offset value over temperature)] / 2
D)	The Offset Drift Velocity is the change rate of the zero rate offset for pre-defined temperature gradients, at specified temperature range. Offset Drift Velocity applies for temperature ramps 2.5K/min and 0.5K/min
E)	Drift of the output value over one hour under exactly same conditions (angular rate, temperature and other environmental conditions)

F)	Default sensitivity used in factory calibration. With this default sensitivity, signal has a typical electrical headroom of ±655°/s.
G)	The Total Sensitivity error is the deviation of the sensitivity over full temperature range, supply voltage range, calibration and lifetime. EMC and vibration are not included
H)	Linearity error is the residual error remaining after a least-squares linear fit over ±300°/s range.
I)	(Measured gradient - nominal gradient) at given step width (Δy). Step width = 2.5°/s, Range ±300°/s
J)	RMS (root-mean-squared) noise is the standard deviation of the samples collected with ≥1kHz sample rate for ≥5s period.
K)	White noise term estimated from Allan Variance
L)	White noise term estimated from Allan Deviation at tau = 1s. Angle random walk is the rate at which the standard deviation of integrated angle errors increases over time.
M)	RT, Allan Variance minimum divided by 0.664. Optimization for SPI duty cycle or sample rate is required to achieve typical Allan variance in table. Device powered four hours before data collection starts to permit fully settling from power up.
N)	ARS axis' are orthogonal if their angle is exactly 90°. Orthogonality Error is the deviation from 90°.
O)	ARS and ACC axis' are orthogonal if their angle is exactly 90°. Orthogonality Error is the deviation from 90°.
P)	ARS cross-axis sensitivity is the sensitivity on other axis than the intended axis of rotation. This means that, if device is rotated around Z axis at 100°/s, X and Y can have an output of ±1.7°/s if specified cross-axis sensitivity is 1.7%.
Q)	Angular rate offset sensitivity in respect to orientation in the earth gravitation. Spec cannot be extrapolated beyond gravitation (±1g).

3.7 Performance Specifications for Accelerometer (ACC)

Table 6 Performance Specifications for Accelerometer are valid for up to ±80 measurement range and over specified supply voltage at room temperature unless otherwise specified

Title	Condition	SC CC	Min	Nom	Max	Unit
Measurement Range[A)]	Measurement axes XYZ, default sensitivity setting				±80	m/s^2
	Measurement axes XYZ, highest selectable sensitivity setting		±15			m/s^2
Total Offset Error[B)]	-40 °C ... +110 °C	SC	-0.4		0.4	m/s^2
Offset Drift Over Temperature[C)]	-40 °C ... +110 °C			0.05	0.1	m/s^2
Offset Drift Velocity[D)]	-40 °C ... +110 °C, 0.5K/min		-0.03		0.03	m/s^2/min
	-40 °C ... +110 °C, 2.5K/min		-0.05		0.05	m/s^2/min
Default Sensitivity - 16bit Mode[E)]	16 bits in 2's complement format			200		LSB/m/s^2
Default Sensitivity - 20bit Mode[E)]	20 bits in 2's complement format			3200		LSB/m/s^2
Total Sensitivity Error[F)]	-40 °C ... +110 °C	CC	-0.5		0.5	%
Linearity Error[G)]	XYZ axis, -80…80m/s^2, -40 °C ... +110 °C				0.4	m/s^2
	XYZ axis, -10m/s^2…10m/s^2, -40 °C ... +110 °C		-0.1	±0.01	0.1	m/s^2
Micro Linearity[H)]	Step width 1m/s^2, -40 °C ... +110 °C		-5		5	%
Output RMS Noise LPF2[I)]	-40 °C ... +110 °C	CC		0.004	0.01	m/s^2
Output RMS Noise LPF1[I)]	-40 °C ... +110 °C	CC		0.006	0.014	m/s^2
Output RMS Noise LPF0[I)]	-40 °C ... +110 °C	CC		0.009	0.02	m/s^2
Noise Density[J)]	-40 °C ... +110 °C			0.75		$mm/s^2/\sqrt{Hz}$
Velocity Random Walk[K)]				38		$mm/s/\sqrt{h}$
Bias Instability[L)]	At RT, Allan Variance minimum divided by 0.664, 3σ, N = 12			0.2		mm/s^2
Orthogonality Error (between ACC axis')[M)]	-40 °C ... +110 °C		-0.2		0.2	deg
Cross-Axis Sensitivity[N)]	Absolute cross axis error, -40 °C ... +110 °C	SC	-1.7		1.7	%

- Specification is valid after 24hours from reflow.
- Each system design including SCH1600 Series components must be evaluated by the customer in advance to guarantee proper functionality during operation.

Table 7 Foot notes for Accelerometer performance specification

Symbol	Foot Note
A)	Measurement range is tied to Electrical headroom and is selectable from predefined options. Changing electrical headroom affects only signal path sensitivity (LSB/°/s) (up to 8x). Increasing sensitivity decreases electrical headroom respectively (up to 1/8x). Max value is indicating measurement range for given product variant where specification is at least valid to. Min value is indicating lowest measurement range the signal can be scaled to by sensitivity setting and in which specification is valid.
B)	Sensor's absolute offset shall remain in specified limits in static measurement environment despite of changes resulting from temperature, supply voltage and lifetime effects.
C)	Offset drift over temperature is determined by [(maximum offset value over temperature) - (minimum offset value over temperature)] / 2
D)	The ACC Offset Drift Velocity is the change rate of the zero acceleration offset for pre-defined temperature gradients, at specified temperature range. @2.5K/min @0.5K/min
E)	Default sensitivity used in factory calibration. With this default sensitivity, signal has a typical electrical headroom of ±163.4 m/s^2.
F)	The Total Sensitivity error is the deviation of the sensitivity over full temperature range, supply voltage range, calibration and lifetime. EMC and vibration are not included
G)	Linearity error is the residual error remaining after a least-squares linear fit over specified measurement range.
H)	(Measured gradient - nominal gradient) at given step width (Δy).
I)	RMS (root-mean-squared) noise is the standard deviation of the samples collected with ≥1kHz sample rate for ≥5s period.
J)	White noise term estimated from Allan Variance
K)	White noise term estimated from Allan Deviation at tau = 1s. Angle random walk essentially is the rate at which the standard deviation of integrated angle errors increases over time.
L)	RT, Allan Variance minimum divided by 0.664. Optimization for SPI duty cycle or sample rate is required to achieve typical Allan variance in table. Device powered four hours before data collection starts to permit fully settling from power up.
M)	ACC axis' are orthogonal if their angle is exactly 90°. Orthogonality Error is the deviation from 90°.
N)	ACC cross-axis sensitivity is the sensitivity on other axis than the intended axis of acceleration. This means that, if device has 10m/s^2 acceleration in Z axis, X and Y can have an output of ±0.17 m/s^2 if specified cross-axis sensitivity is 1.7%.

3.8 Temperature sensor

Table 8 Temperature sensor performance specification

Title	Min	Nom	Max	Unit
Measurement range	-50		135	°C
Temperature Signal sensitivity		100		LSB/°C
Total signal accuracy (Offset, linearity, sensitivity)	-15		15	°C
Linearity	-1		1	°C

Temperature is converted to °C with following equation:

Temperature [°C] = TEMP / 100,

where TEMP is temperature sensor output register content in 2's complement format.

3.9 Gyro and ACC Frequency response

3.9.1 Filter characteristics

SCH1600 Filter characteristics are presented in table 9. Note that these do not represent the total frequency response and group delay.

Table 9 SCH1600 Filter characteristics.

Filter	Title	Type	Order	Min	Nom	Max	Unit
LPF0	Cut-off frequency (-3dB)	Butter	4	63.5	68	72.5	Hz
	Group Delay					10	ms
	Settling time				10	20	ms
LPF1	Cut-off Frequency (-3dB)	Butter	4	28	30	32	Hz
	Group Delay					16	ms
	Settling time				25	40	ms
LPF2	Cut-off Frequency (-3dB)	Butter	3	12.2	13	13.8	Hz
	Group Delay					35	ms
	Settling time				65	200	ms
LPF3	Cut-off Frequency (-3dB)	Bessel	4	262	280	300	Hz
	Group Delay					1.15	ms
	Settling time					5	ms
LPF4	Cut-off Frequency (-3dB)	Bessel	3	346	370	394	Hz
	Group Delay					0.78	ms
	Settling time					TBD	Ms
LPF5	Cut-off Frequency (-3dB)	Bessel	3	220	235	250	Hz
	Group Delay					1.24	ms
	Settling time					TBD	ms

3.10 Functional safety Specification

Development process has been done according to ISO26262, release 2018 fulfilling ASIL-D design process requirements.

ASIL specification is depending on the function according to the Table 10

Table 10 Functional Safety Requirements

Function	ASIL	SPFM	FHTI
Total offset error of angular rate signal shall not exceed ±2 dps (XY) or ±1 dps (Z)	B	≥ 90%	≤ 20ms
Total sensitivity error of any angular rate signal shall not exceed ±1.5 %	B	≥ 90%	≤ 20ms
Cross-axis sensitivity error of any angular rate signal shall not exceed ±1.7 %	B	≥ 90%	≤ 20ms
Any offset drift of any angular rate signal shall not exceed ±1.4 °/s/s	B	≥ 90%	≤ 20ms
Total offset error of any low-g acceleration signal shall not exceed ±0.5 m/s^2	B	≥ 90%	≤ 20ms
Total sensitivity error of any low-g acceleration signal shall not exceed ±1 %	B	≥ 90%	≤ 20ms
Cross-axis sensitivity error of any low-g acceleration signal shall not exceed ±1.7 %	B	≥ 90%	≤ 20ms
Any offset drift of the low-g acceleration signal shall not exceed ± 0.1 (m/s^2)/min	B	≥ 90%	≤ 20ms
Temperature sensor signal error shall not exceed +/-15degC	B	≥ 90%	≤ 20ms
Any low-g acceleration or Gyro signal shall not freeze	B	≥ 90%	≤ 20ms
Any error of any low-g acceleration or gyro signal shall not change the sign of the corresponding signal	B	≥ 90%	≤ 20ms
Common Cause (Violation of both ACC and Gyro signal)	D	≥ 99%	≤ 20ms
Common Cause (SPI)	D	≥ 99%	≤ 20ms

3.11 Pin Description

The pinout for SCH1600 is presented in Figure 1, while the pin descriptions can be found in Table 11

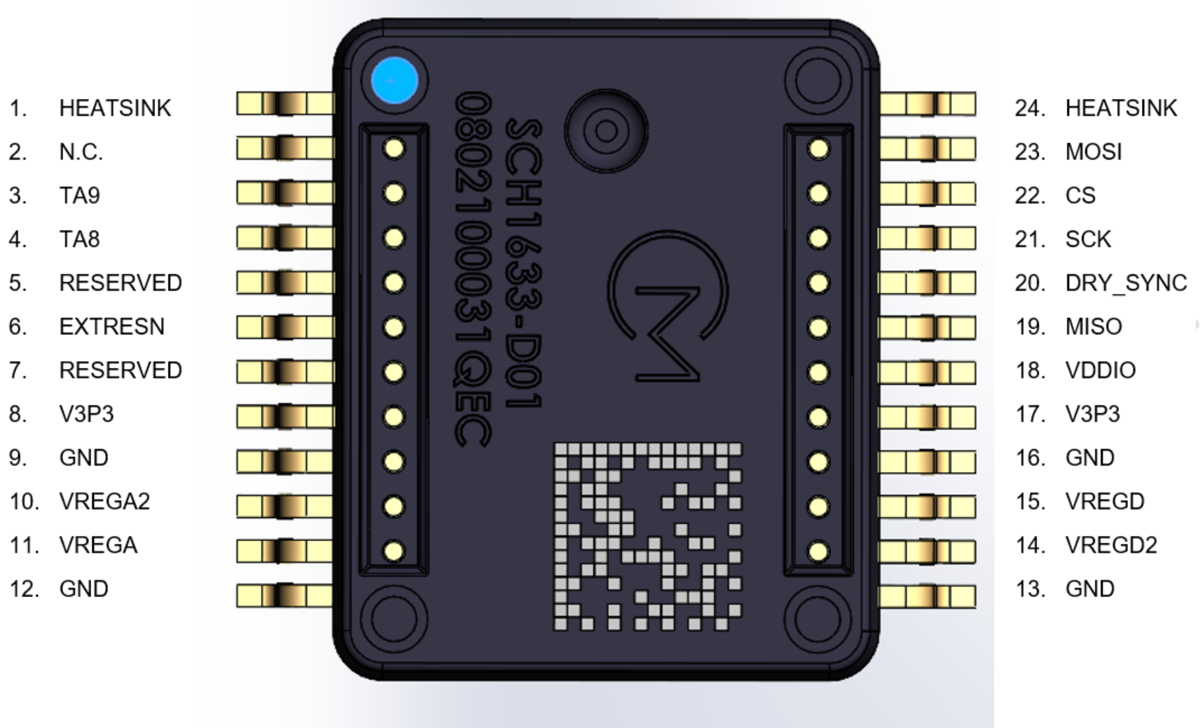

Figure 1 SCH1600 Series Pin Description

Table 11 SCH1600 Pin Description

Pin #	Name	Description	Type	Voltage Level	Default state/structure
1	HEATSINK	Heatsink connection	GND	0 V	
2	Reserved	Floating	N/A		
3	TA9	SPI device selection Address 1 (static). Slave addressing in SafeSPI2. Max four slaves can be addresses by TA9:8. TA on the slave is defined DVIO logic level at pins TA9 TA8.	DIN	0V	0/PDR[1)]
4	TA8	SPI device selection Address 0 (static). Slave addressing in SafeSPI2. Max four slaves can be addresses by TA9:8. TA on the slave is defined DVIO logic level at pins TA9 TA8.	DIN	0V	0/PDR[1)]
5	Reserved	Reserved	N/A		
6	EXTRESN	External reset input (low active) during normal operation.	DIN/AIN	VDDIO V	1/PUR[1)]
7	Reserved	Reserved	N/A		

8	V3P3	External unregulated inputs for the core supply regulators	SUPPLY	3.3 V	
9	GNDA	Analog ground voltage	GND	0V	
10	VREGA2	Regulated core voltages for the analog circuitry. External cap connection for positive reference/supply voltage. Connected in PCB.	AIN	2.5 V	
11	VREGA	Regulated core voltages for the analog circuitry. External cap connection for positive reference/supply voltage. Connected in PCB.	AOUT	2.5 V	
12	GNDA	Analog ground	GND	0 V	
13	GNDD	Digital ground	GND	0 V	
14	VREGD2	Regulated core voltages for the digital circuitry. External cap connection for positive reference/supply voltage. Connected in PCB.	AIN	1.5 V	
15	VREGD	Regulated core voltages for the digital circuitry. External cap connection for positive reference/supply voltage. Connected in PCB.	AOUT	1.5 V	
16	GNDD	Digital ground	GND	0 V	
17	V3P3	External unregulated inputs for the core supply regulators	SUPPLY	3.3 V	
18	VDDIO	Digital supply IO	SUPPLY	3.3 V (option: 1.8V or 2.5V)	
19	MISO	Master In Slave Out (SPI)	DOUT	VDDIO V	TRI
20	DRY_SYNC	Sync input (active high) DATARDY outputs an interrupt signal for the external MCU when the internal output registers (Gyro+accel) have been updated.	DIN/DOUT	VDDIO V	0/PDR
21	SCK	Serial clock (SPI)	DIN	VDDIO V	0/PDR
22	CS	Chip select (SPI)	DIN	VDDIO V	1/PUR
23	MOSI	Master Out Slave In (SPI)	DIN	VDDIO V	0/PDR
24	HEATSINK		GND		

1) Strong PD/PU resistance during device reset state, otherwise weak PD/PU.

3.12 Digital I/O Specification

Table 12 describes the DC characteristics of SCH1600 sensor SPI I/O pins. Current flowing into the circuit has a positive value.

Table 12 SPI DC characteristics

Title	Symbol	Min	Max	Unit
SPI Voltage Level	VIO	1.7	3.6	V
Input High Voltage	VIH	0.7*VIO	VIO	V
Input Low Voltage	VIL	0	0.3*VIO	V
Input Voltage Hysteresis	VHYST	0.1*VIO		V
Input/Output Capacitance	CIO		10	pF
Total MISO load capacitance, <Wide> range	CLWIDE	10	100	pF
Input pull-down resistance, strong (default)	RPD	60	140	kOhm
Input pull-up resistance, strong (default)	RPU	60	140	kOhm
Input pull-down/pull-up resistance, weak (option)	RPD/RPU	200	400	kOhm
Output leakage current in case MISO is in high impedance (tri -state) condition	ILEAK	-10	10	µA

3.13 SPI AC Characteristics

The AC characteristics of SCH1600 Series are defined in Figure 2 and Table 13

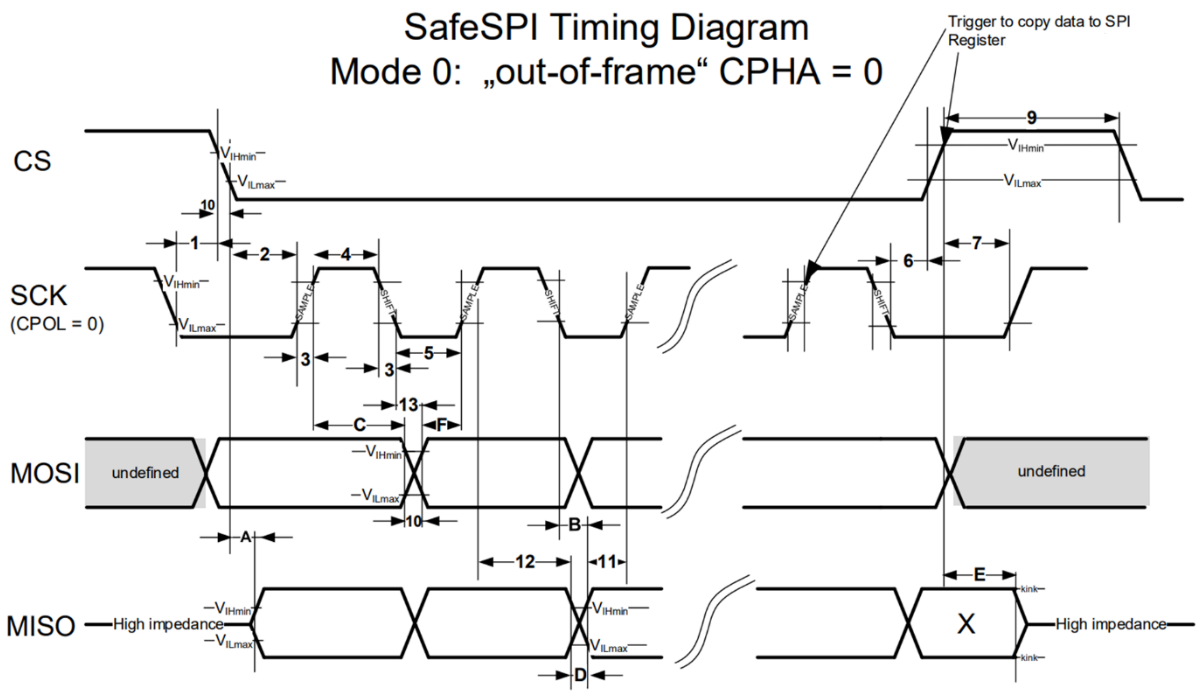

Figure 2 Timing diagram of SPI communication. (SPI mode 0)

Table 13 SPI AC electrical characteristics

Title	Foot Note	Symbol	Min	Max	Unit
SCK Operating Frequency			0.095	10.5	MHz
MISO data valid time (CS)		A		40	ns
MISO data valid time (SCK)		B		32	ns
MOSI data hold time		C	20		ns
MISO rise/fall time	MISO rise/fall time is not defined during transition between high impedance and active mode	D	2	9	ns
MISO data disable lag time		E		50	ns
MOSI data setup time		F	10		ns
SCK disable lead time		1	10		ns
SCK enable lead time	SCK enable lead time	2	40		ns
SCK rise and fall time		3	2	9	
SCK high time	SCK high time	4	37		ns
SCK low time	SCK low time	5	37		ns
SCK enable lag time		6	20		ns
SCK disable lag time		7	10		ns
Sequential transfer delay	In case of MOSI Write commands (RW=1)	9	750		ns
Sequential transfer delay	In case of MOSI Read commands (RW=0)	9	450		ns
MOSI rise and fall time		10	2	9	ns
MOSI data setup time	Setup time of MOSI before the rising edge of SCK	11	5		ns
MISO data hold time		12	X		ns
MOSI valid time		13		10	ns
CS rise and fall time		10	2	9	ns

3.14 Measurement Axis and directions

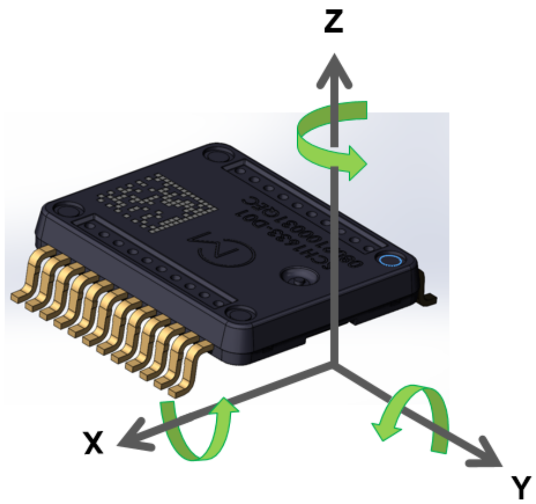

Figure 3 SCH1600 measurement directions

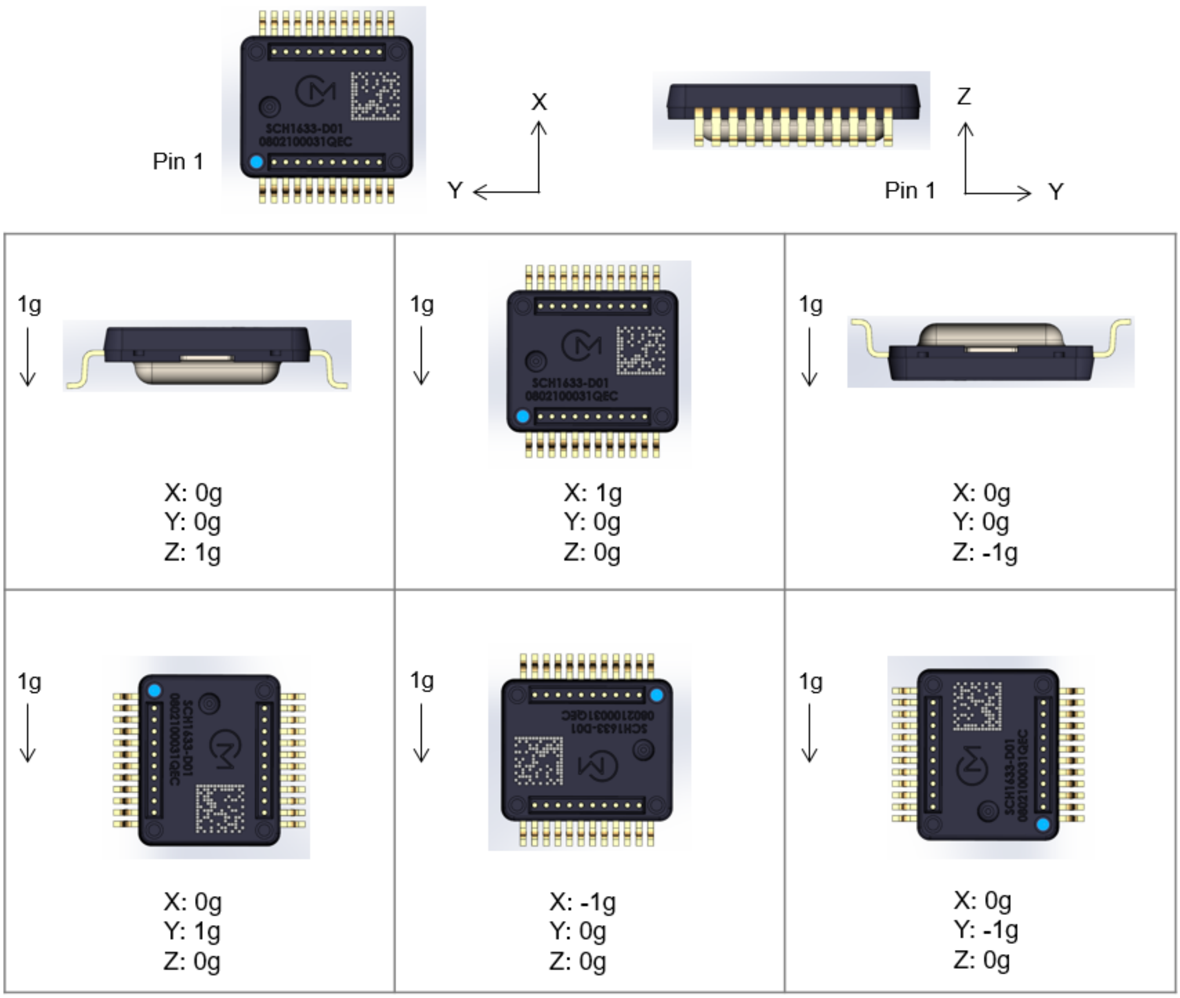

Figure 4 SCH1600 accelerometer measurement directions and outputs. 1g indicates direction of gravity. Note: Pin 1 is marked in blue only in this data sheet to emphasize location.

3.15 Package outline drawing

The SCH1600 package outline and dimensions are presented in figure 5 and table 14. All dimensions are in millimeters

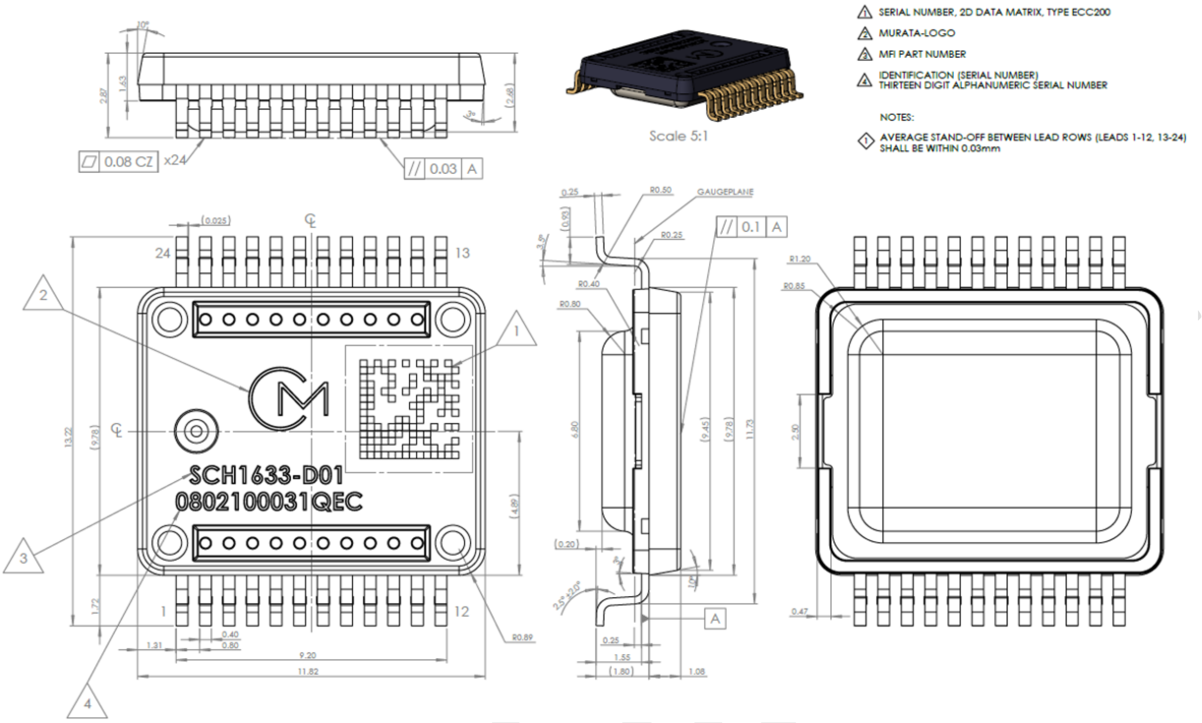

Figure 5 The outline of SCH1600 package in mm

Table 14 Tolerances

Type	Tolerance
Linear	±0.05
Radius	±0.05
Angular	±1.0°

3.16 PCB footprint

SCH1600 foot print dimensions are presented in Figure 6

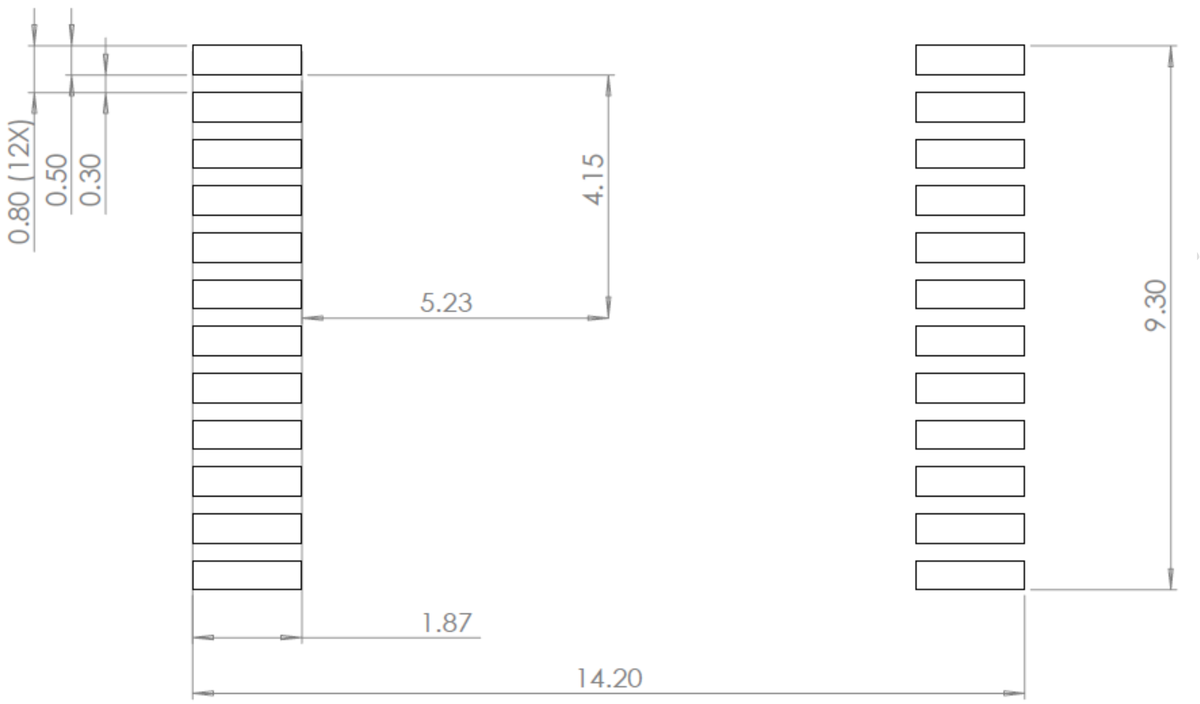

Figure 6 Recommended PCB pad layout for SCH1600

4 General Product Description

4.1 Component Block Diagram

The SCH1600 sensor consists of independent acceleration and angular rate sensing elements, and an Application-Specific Integrated Circuit (ASIC) used to sense and control those elements. The angular rate and acceleration sensing elements are manufactured using Murata's proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables the making of robust, extremely stable, and low noise capacitive sensors.

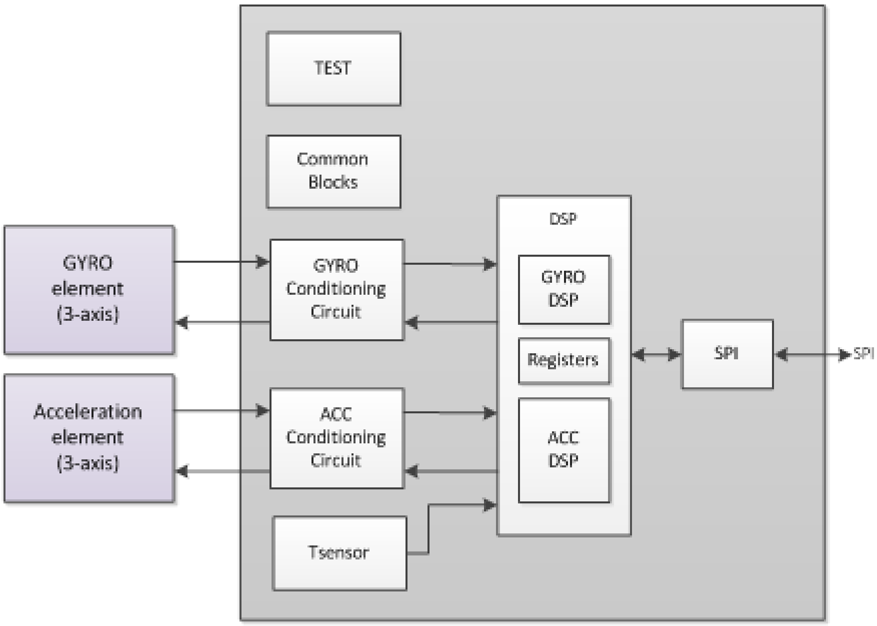

Figure 7 SCH1600 Component block diagram

4.2 Acceleration sensing element

The acceleration sensing element consists of three acceleration-sensitive masses. Acceleration causes capacitance change that is converted into a voltage change in the signal conditioning ASIC.

4.3 Angular rate sensing element

The angular rate sensing element consists of moving masses that are intentionally exited to in-plane drive motion. Rotation in a sensitive direction causes in-plane (Z) or out-of-plane (XY) movement that can be measured as capacitance change with the signal conditioning ASIC.

4.4 Factory calibration

Sensors are factory calibrated. No separate calibration is required in the application. Parameters that are trimmed during production include offset, sensitivity and Cross-Axis sensitivity for gyroscope and accelerometer. Fail-safe monitoring signals are also calibrated. Offset and sensitivity are calibrated with 2nd order polynomial. Linear calibration is used for Cross-Axis. Calibration is done at -40°C, +25°C, and +110°C. Calibration parameters are stored in non-volatile memory during manufacturing. The parameters are read automatically from the internal non-volatile memory during the start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If the best possible offset/bias accuracy is required, system-level offset/bias calibration (zeroing) after assembly is recommended.

5 Component Operation, Reset and Power Up

5.1 Component operation

The SCH1600 component has an internal power-on reset circuit. After release of EXTRESN and once the power supplies are within the specified range, the component releases an internal reset signal and reads configuration and calibration data from the non-volatile memory to volatile registers. After the memory is read, the sensor goes to Low power mode and an external SPI command, EN_SENSOR, is needed to continue to the initialization phase and to start the measurement.

Start-up time is dependent on the low pass filter setting. After the power-on or reset, release of EXTRESN and EN_SENSOR command, the sensor shall be able to provide valid acceleration and angular rate data after the specified power-on start-up time.

SCH1600 sensor uses the LPF0 setting by default. In case some other low pass filter is desired the filter can be selected by SPI command. SCH1600 component has extensive internal fail-safe diagnostics to detect over range and possible internal failures. The diagnostic status can be monitored via Status bits included in SPI frame and status register bits.

5.2 Internal Failsafe Diagnostics

During the startup sequence, the sensor performs a series of internal tests that will set various error flags in the sensor status registers. To clear them it is necessary to read the status registers after the startup sequence is complete. When reading the status registers, the user must take into account that the state of status flags is not defined during LPM (Low Power Mode) and the 215ms Wait state after EN_SENSOR.

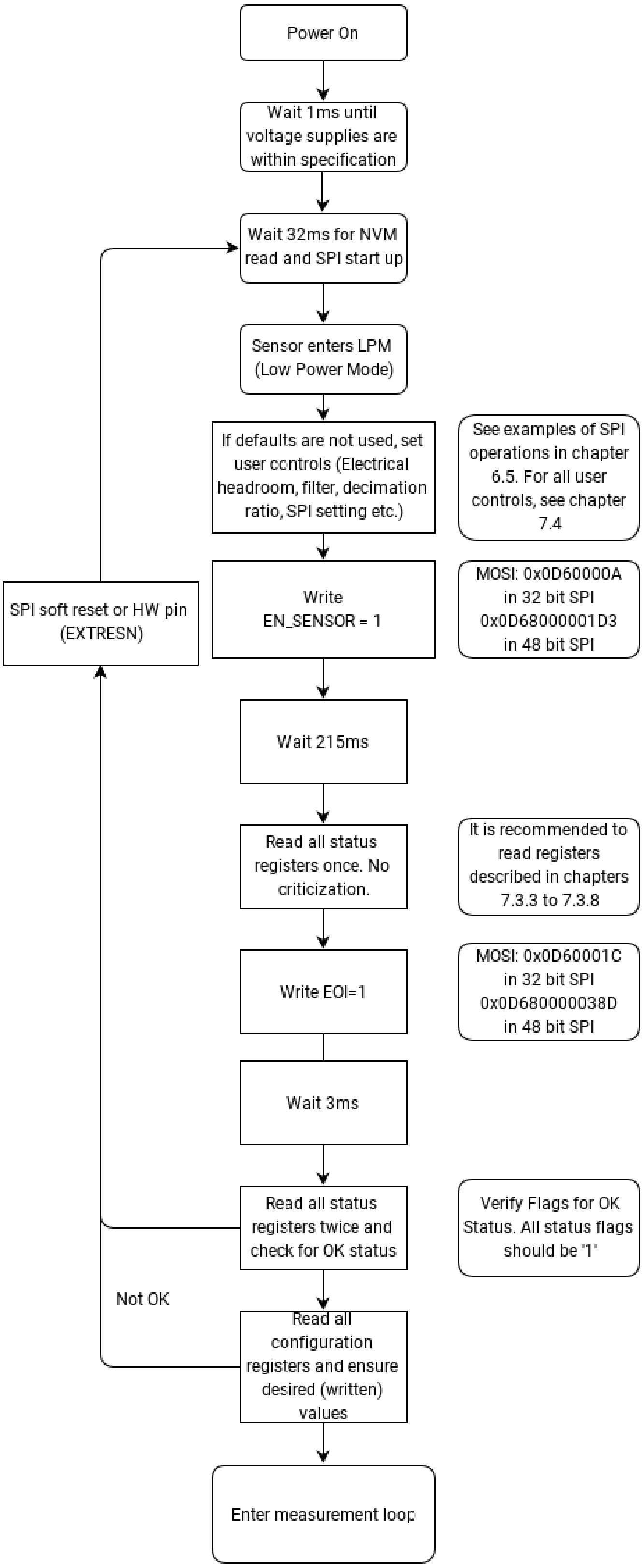

Figure 8 Example of SCH1600 Start-up sequence

5.3 Component output channels

The SCH1600 series component has several output channels for the user to choose from. The component has two channels for reading gyroscope data and a total of 3 channels for reading acceleration data. Each channel consists of separate X, Y and Z output data registers and each channel and axis has separate status flags. The first gyroscope data channel RATE_XYZ1 has interpolated output and second channel RATE_XYZ2 is for decimated output. The first acceleration channel ACC_XYZ1 has interpolated output, second channel ACC_XYZ2 is for decimated output and the third channel is a redundant interpolated channel, ACC_XYZ3. Interpolation and decimation are explained in more detail in chapter 5.4.

The user may choose to utilize multiple channels simultaneously and adjust channel settings separately according to the users' needs. Dynamic range can be individually set for each channel, but filter settings are shared between Interpolated and Decimated outputs. Different filters within one channel can be applied between X, Y and Z axis, if desired. For example, the user can read ACC_XYZ1 with nominal ±163.4m/s^2 dynamic range and 68Hz filter and ACC_XYZ3 with nominal ±20.48m/s^2 dynamic range and 13Hz filter. The output options are presented in the table below.

Table 15 SCH1600 output channel options

Channel	Description	Filter setting	Dynamic range setting
RATE_XYZ1	Interpolated Gyroscope output	Common for both gyro channels, selectable separately for each axis	RATE_XYZ1 specific
RATE_XYZ2	Decimated Gyroscope output		RATE_XYZ2 specific
ACC_XYZ1	Interpolated Accelerometer output	Common for ACC_XYZ1 and ACC_XYZ2 channels, selectable separately for each axis	ACC_XYZ1 specific
ACC_XYZ2	Decimated Accelerometer output		ACC_XYZ2 specific
ACC_XYZ3	Redundant Interpolated Accelerometer output	ACC_XYZ3 specific, selectable separately for each axis	ACC_XYZ3 specific

5.4 Solutions for asynchronous clock domains

Multiple features are implemented to improve synchronization between the product's internal clock and application system clock. While most systems can most likely cope with conventional continuous polling of SPI peripheral, accurate time-domain synchronization can be essential in certain high-performance applications. The table below summarizes the synchronization features.

Table 16 Solutions for asynchronous clock domains

Feature	Use case	Value
Interpolation	This should be used by default. Interpolation is applied in outputs RATE_XYZ1, ACC_XYZ1, and ACC_XYZ3.	- Minimized sampling jitter - Minimized timing difference between channels - No missing samples
SYNC Input	Special case. Recommended if there is a need to sync between multiple SCH1600 family sensors or if sample time consistency is valued over jitter	- Synchronization between multiple sensors. - Data can be received with consistent rate even if host system sampling is affected by changing load
Data Ready (Interrupt)	Special case. Recommended only, if decimated, low update rate outputs RATE_XYZ2 and ACC_XYZ2 are used. Decimated outputs are typically used if MCU bandwidth is limited.	- Minimized sampling jitter. With decimated outputs, the maximum data jitter depends on the decimation ratio and interrupt use removes this jitter totally. - No missing samples.

Data counter	Special case. Recommended only if Data Ready is not preferred in application.	- Data counter is index for the component data output values. The application can monitor that: - Data is updating - Every wanted sample has been acquired - The same sample has not been read twice
Data counter with frequency counter	Special case. Recommended if integration operation is performed to sensor data and timing uncertainty or data jitter of the interpolated data do not fulfill the system accuracy requirements.	- Data counter together with frequency counter can be used for more accurate integration.

SYNC and Data Ready are implemented on a single hardware pin. Therefore, simultaneous use of these pins is not possible. Controlling the behavior of SYNC and Data ready is explained in chapter 7.4

5.4.1 Interpolation

The purpose of interpolation is to minimize time uncertainty (sampling jitter) by increasing artificially the internal sample rate. The natural output data rate of all data outputs is F_PRIM/2, which is 11.8kHz with nominal primary frequency. This means that a time-uncertainty between sensor register update and system sampling time could be theoretically anything between 0...85µs.
To minimize this jitter, a fixed interpolation factor of 32 is applied to outputs RATE_XYZ1, ACC_XYZ1, and ACC_XYZ3. With nominal primary frequency it corresponds to a 377.6kHz refresh rate of register content.
The sample rate is increased by adding a 1 cycle latency delay to the initial sample. The delay corresponds the maximum time uncertainty which is with nominal primary frequency 85µs. A linear interpolation is then applied between the initial sample and the new sample and this interpolation is divided into time segments by the artificially increased update rate 32 x F_PRIM/2. Time uncertainty is now reduced to the length of this segment, which is max (85 µs)/32 = 2.6 µs with nominal primary frequency.

Please refer to the illustration below.

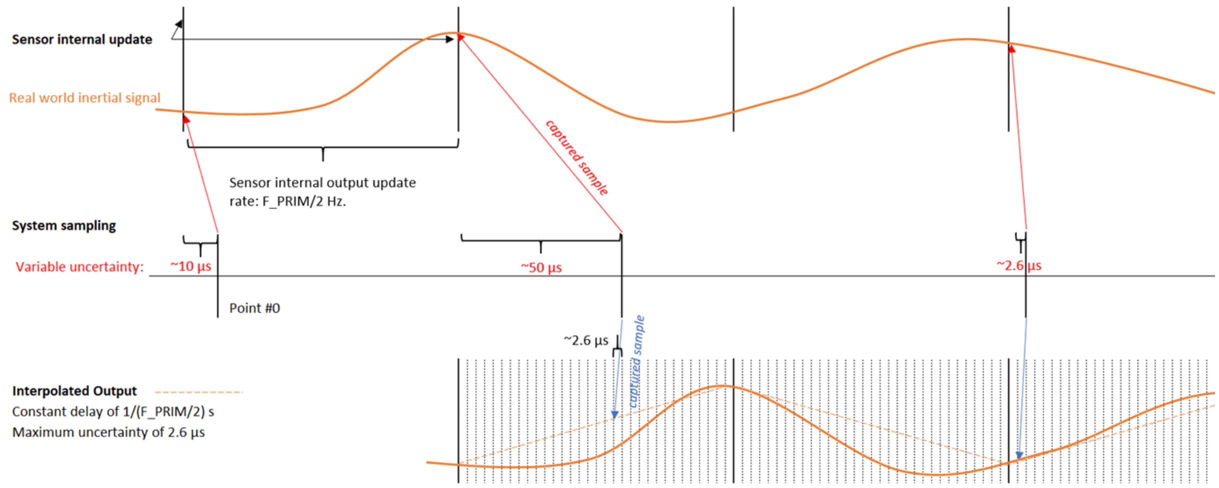

Figure 9 Interpolation. 8kHz system sampling rate is assumed in this illustration.

5.4.2 Decimation

Certain systems want to utilize every available sample and for example acquire samples from all axis from the same time instant. As the natural output data rate with nominal primary frequency is 11.8kHz, this can create more load to the MCU than it can handle. The purpose of decimation is to decrease the internal update rate to give the host system enough time to read every sample.
During start-up, the user can select a suitable decimation ratio from the options presented in table 17. The decimation ratio is then applied to outputs RATE_XYZ2 and ACC_XYZ2.

Table 17 Selectable decimation ratios and corresponding ODR

Decimation factor	Output data rate	Output data rate with nominal F_PRIM (kHz)
1	F_PRIM/2	11.8
2	F_PRIM/4	5.9
4	F_PRIM/8	2.95
8	F_PRIM/16	1.475
16	F_PRIM/32	0.7375

The drawback of decimation is that sampling jitter is increased with the same ratio as the decimation factor. With nominal primary frequency and decimation ratio of 16, the sampling jitter will be up to 85µs x 16 = 1.36ms. This means that sample age can be anything between 0 and 1.36ms. To address this issue, the user can combine decimation with the data ready function. Data ready is explained in chapter 5.4.4.

5.4.3 SYNC input pin

Certain systems with high-performance requirements and/or high safety requirements may benefit from the use of multiple SCH1600-series components. Depending on application SPI master clock conditions, the reading operation of multiple parallel sensors can take longer than the sensor internal register update period if individual MISO line is not used for each component. As a result of this, samples are being acquired from different time instants for each parallel sensor. In certain real-world inputs, this can lead to a significant apparent disagreement of sensors, as different time-instants are being sampled.
To mitigate this issue, SYNC input pin has been implemented. When the master issues SYNC signal to all sensors in the system, the sensors' internal updates for RATE_XYZ1/2 and ACC_XYZ1/2/3 are being frozen until SYNC pin is set LOW or after time out period set by CTRL_SYNC_TOC_TH time-out counter. This allows enough time for the master to read all sensor data from a single time instant. CTRL_SYNC_TOC_TH is user-selectable with typical values of 1.2ms to 11.6ms. Please refer to chapter 7.4.4 for user controls.

SYNC is only feasible on interpolated outputs RATE_XYZ1 and ACC_XYZ1/3. With decimated outputs and a decimation factor of 2 or above, most masters will have enough time to read the output registers before they are updated again.

SYNC can be beneficial also to ensure that all 6-axis data is captured at the same time instant. With very low SPI master clocks, it can occur that even a single sensor will update its internal registers during the slow read operation. In this case, different axis data could represent different time instant. SYNC can also help in situations where system load is high, and sample read cannot be performed with a consistent frequency.

Please refer to the illustration below.

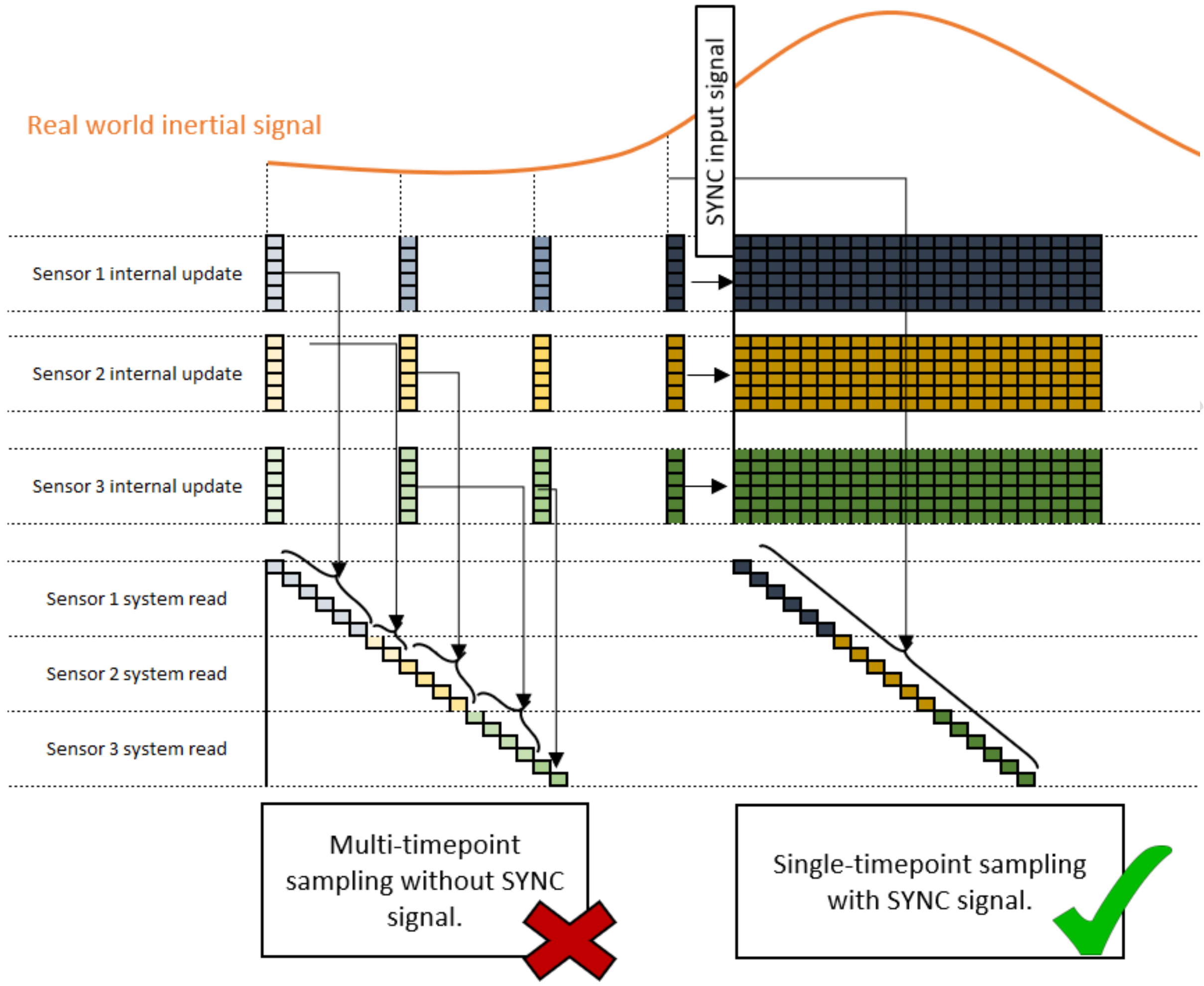

Figure 10 Illustration of SYNC usage when 3 slave sensors are read by single master.

5.4.4 Data Ready, DRY

In some system implementations, it may be that the rate, at which the host processor can read the peripherals is limited. In these cases, in order to ensure that the host has enough time to read without signal aliasing, it is beneficial to use decimated outputs with suitable decimation factor. When the sensor update rate is lowered, sampling jitter becomes more of an issue. As explained in chapter 5.4.1, worst case sampling jitter can be up to 85µs with decimation factor of 1. When decimation factor is increased, the worst-case sampling jitter is increased accordingly.

In case jitter minimization is critical in application, user should use the data ready output pin. When all sensor output channels have been updated, the data ready triggers a rising edge to indicate that the samples were generated. This rising edge can be used as direct interrupt to start sensor read operation or the host can take note of the data ready signal and ensure that the data is read in burst before the next expected sensor internal update. This way, the system can ensure that no samples are missed, and no samples are being read twice.

Please refer to the illustration below.

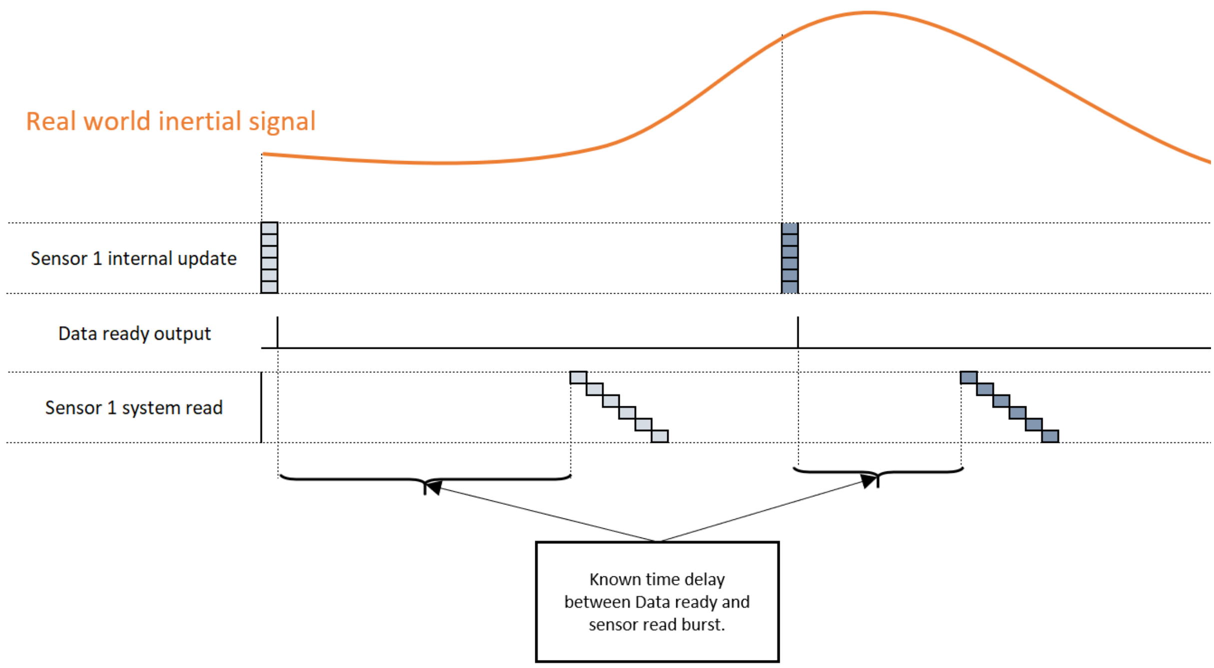

Figure 11 Illustration of Data ready output signal. In this example, data is read in a burst between the internal sensor updates.

5.4.5 Data Counter

Data counter is supported for decimated outputs, RATE_XYZ2 and ACC_XYZ2. The value of data counter is increased by one when a new sample is available from corresponding RATE/ACC channel. It can be understood as the index for the component data output values. Using data counter, the user can monitor that every wanted sample has been acquired and that same sample has not been read twice. When using 48-bit SPI protocol, data counter 4-bit value is included in MISO response frame. Data counter can be also used in 32-bit mode by reading DCNT_RATE and DCNT_ACC register values via SPI command. Register location is described in chapter 7.3.

5.4.6 Frequency Counter

Using frequency counter, user can acquire accurate clock information from component internal MCLK via SPI. The value of Frequency counter register is increased by one with every 16th rising edge of Master Clock.

5.4.7 Calculating Exact Time Stamp

The data counter value can be combined with the frequency counter data to calculate exact time stamp of sample, when the MCU clock of the host system is used as reference. This combination is recommended if integration operations are performed to sensor data and timing uncertainty or data jitter of the interpolated data do not fulfill the system accuracy requirements.

6 Component Interfacing

6.1 Safe SPI

Product supports Safe SPI v2.0 protocol to transfer data between SPI master and registers of SCH1600 ASIC. The product always operates as a slave device in master-slave operation mode. 3-wire SPI connection cannot be used.
Communication between Master and Slave is done with pins described below in table 17

Table 18 SPI interface pins

SPI interface pin	Description	Communication direction
CS	Chip Select (active low)	MCU to ASIC
SCK	Serial Clock	MCU to ASIC
MOSI	Master Out Slave In	MCU to ASIC
MISO	Master In Slave Out	ASIC to MCU

SPI communication uses out-of-frame protocol so each transfer has two phases. The first phase contains the SPI command (Request) and the data (Response) of the previous command. The second phase contains the next Request and the Response to the Request of the first phase, see Figure 12. The first response after reset is undefined and shall be discarded.

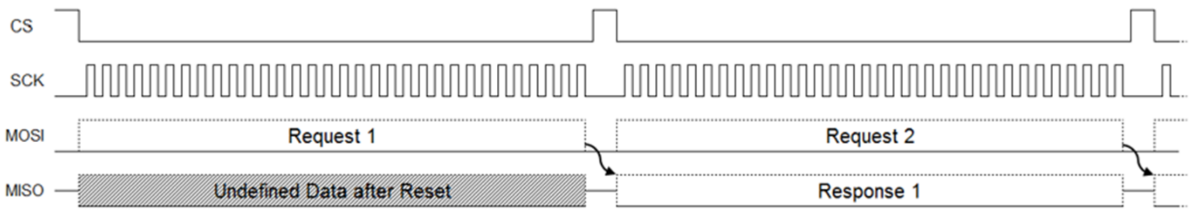

Figure 12 SPI protocol example

Product SPI block implements two different SPI protocol types. Both protocol types can be used during operation by defining bit length in SPI frame.
• SafeSPI2 32-bit frame, SPI32BF.
• SafeSPI2 48-bit frame, SPI48BF.
SPI block does not implement the complete SafeSPI v2.0 specification. Summary of supported features is seen in table below. For Safe SPI standard, please refer to www.SafeSPI.org

Table 19 SCH1600 supported features of SafeSPI v2.0

Supported feature	Description
<48/32oof>	Block receives and transmits 32-bit and 48-bit Out-of-frame SPI frames. In-frame protocols are not supported.
<FrTyp>	MOSI frame width is defined by received frame length. Frame is effective only if width is 32-bits or 48-bits and the CRC is valid.
<SelBitWidthByAdr >	Next MISO frame width is decided by <FrTyp>
<Sel4SlaveByAdrPin>	Two MSB address bits can be used to select one of four slaves when one CS signal pin is in use. Slave compares the two MSBs to a reference value defined by two input pins.
<Sel4SlaveByAdrNVM>	Two MSB address bits can be used to select one of four slaves when one CS signal pin is in use. Slave compares the two MSBs to a reference value defined by a NVM programmed value. Factory use only.
<FixedSensorFrame>	Frame content is well defined and fixed.
<CLWide>	Wide range for “total signal load capacitance”
<DCnt>	Block updates a wrapping 4-bit sample counter each time new sensor data is generated.
<IDS>	Internal Data Status field includes additional status information for sensor data.
<CAP>	Not implemented and replaced with fixed value.

The SPI transmission is always started with the CS falling edge and terminated with the CS rising edge. The data is captured on the SCK's rising edge (MOSI line) and it is propagated on the SCK’s falling edge (MISO line). This equals to SPI Mode 0 (CPOL = 0 and CPHA = 0), an example with 32bit frame can be seen in Figure 13.

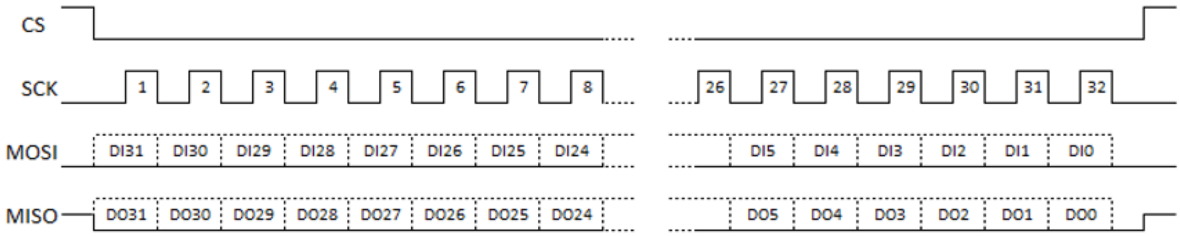

Figure 13 SPI frame format example (32bit)

6.2 SPI Frame structure

SPI Frame format is explained in figure 14 and table 19

SPI48BF

<table>
<tr><td>Bit</td><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MOSI</td><td colspan="10">TA 9:0</td><td>RW</td><td>0</td><td>FT</td><td colspan="7">AE</td><td colspan="20">DATAI 19:0</td><td colspan="8">CRC8</td></tr>
<tr><td>MISO (sensor data)</td><td>D</td><td colspan="10">SA 9:0</td><td>IDS</td><td>CE</td><td colspan="2">S1:0</td><td colspan="4">DCNT</td><td>*</td><td colspan="20">SENSOR 19:0</td><td colspan="8">CRC8</td></tr>
<tr><td>MISO (other data)</td><td>D</td><td colspan="10">SA 9:0</td><td>IDS</td><td>CE</td><td colspan="2">S1:0</td><td colspan="5">*</td><td colspan="20">INFO 19:0</td><td colspan="8">CRC8</td></tr>
</table>

SPI32BF

<table>
<tr><td>Bit</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MOSI</td><td colspan="10">TA 9:0</td><td>RW</td><td>0</td><td>FT</td><td colspan="16">DATAI 15:0</td><td colspan="3">CRC3</td></tr>
<tr><td>MISO (sensor data)</td><td>D</td><td colspan="10">SA 9:0</td><td>S1</td><td colspan="16">SENSOR 15:0</td><td>S0</td><td colspan="3">CRC3</td></tr>
<tr><td>MISO (other data)</td><td>D</td><td colspan="10">SA 9:0</td><td>S1</td><td colspan="16">INFO 15:0</td><td>S0</td><td colspan="3">CRC3</td></tr>
</table>

Figure 14 SPI frame format for 48bit and 32bit frames

Table 20 SPI bit definitions

SYMBOL	DESCRIPTION
D	D=1 condition: Gyro data register read ACC data register read Temperature data register read D=0 condition: Any other register than listed above is read
TA	Defines the Target Address in SCH1600. TA[9:8] bits are used as Chip Select information, and thus they are not part of the effective address. TA[7:0] are used as effective address within the chip.
SA	Contains the Source Address. It has the same content as TA.
RW	Read and write access selector. Read is selected with 0 and write with 1.

FT (FrTyp)	Frame Type for next MISO frame: 0 for SPI32BF, 1 for SPI48BF. MOSI frame width is defined by the MOSI frame itself, hence this field should match the next incoming MOSI frame, since out-of-frame responses are in use.
AE	Reserved. Bits shall be ignored.
DATAI	MOSI line input data from SPI host. This field is 20-bits wide for SPI48BF and 16-bits for SPI32BF.
SENSOR	MISO line sensor type output data towards SPI host.
INFO	MISO line non-sensor type output data towards SPI host. This field is 20-bits wide for SPI48BF and 16-bits for SPI32BF. 20-bit data is clipped from LSB end to 16-bit with SPI32BF, i.e. data is MSB aligned.
*	Unused field that is ignored for receive and set to all-zeros for transmit.
S1:0, S1, S0	Sensor status indication.
CE	Command Error indication. SCH1600 reports only semantically invalid frame content using these bits. SPI protocol level errors are indicated with High-Z on MISO pin.
IDS	Internal Data Status indication. SCH1600 uses this field to indicate common cause error. This is redundant, more accurate info for sensor status (S1:S0).
DCNT	A wrapping 4-bit sensor data counter.
CRC8 (C7:0)	8-bit CRC reference for SPI48BF. Calculated over bits 47 to 8.
CRC3 (C2:0)	3-bit CRC reference for SPI32BF. Calculated over bits 31 to 3.

6.3 Multi-slave operation

SCH1600 SPI supports several slave devices on one bus by using either multiple chip select lines, one for each slave, or with only one common CS and using TA9 and TA8 pins to enable logical addressing.

Pin 3 (TA9) and pin 4 (TA8) correspond to the bits TA9:9 and TA8:8 included in the SPI MOSI frame. Issuing a pull-up signal to either pin means that the components TA bit has been flipped as ‘1’ in component logic level. All options for addressing four slaves are shown in figure below.
Example: Compose MOSI frame targeted to component 3
1. Keep pin 3 (TA9) low and pull up pin 4 (TA8)
2. Send MOSI frame in which TA9:8 is written as ‘01’

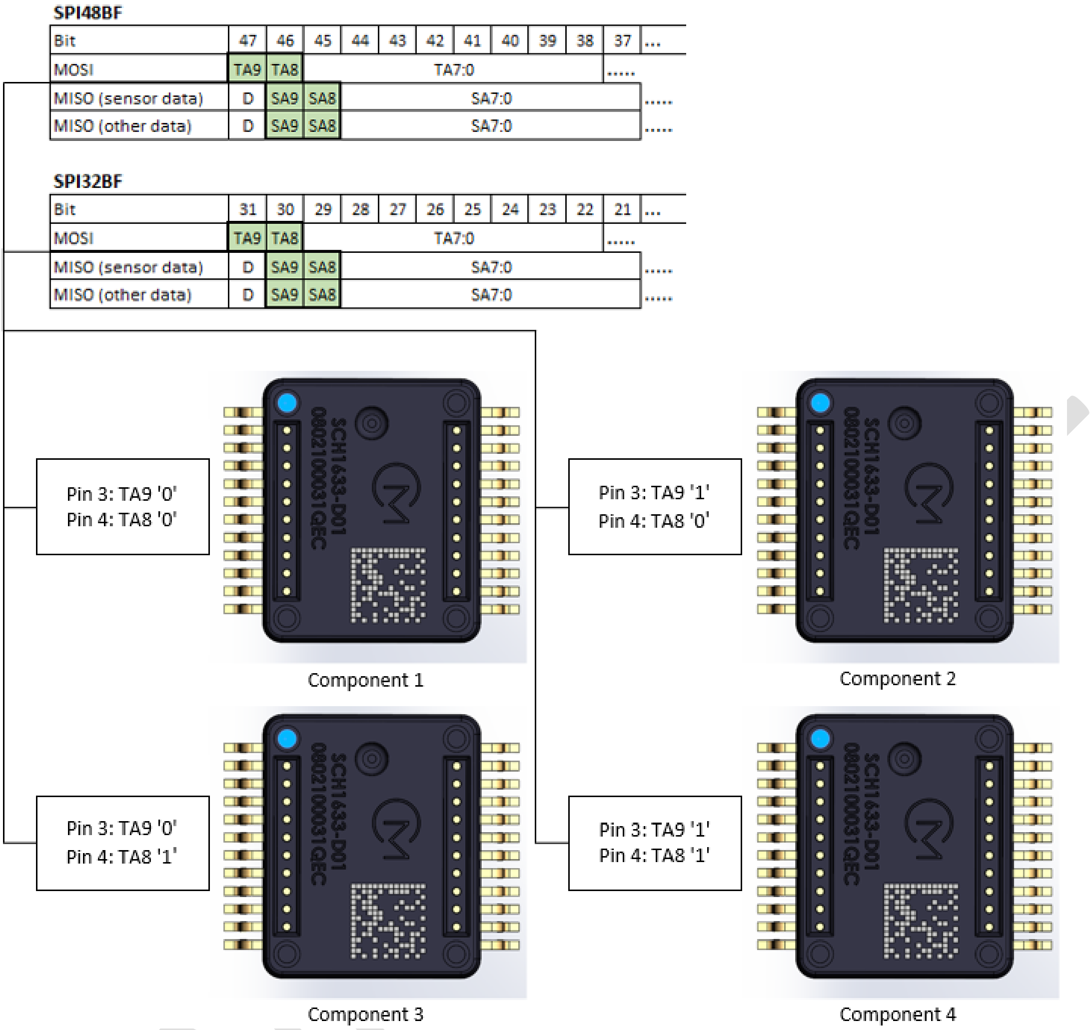

Figure 15 Multi-slave addressing by TA-bits

6.4 SPI Frame Status Bits

Status bits indicate the functional status of the sensor. See table below for definitions of bits S[1:0]

Table 21 Status bit description

Status bits S[1:0]	Description
00	Normal Operation
01	Error Status
10	Saturation Error
11	Initialization Running

S[1:0] priority order is 11 (Initialization) --> 01 (Error) -->10 (Saturation) --> 00 (Normal operation)

IDS, or Internal Data Status bits are redundant error status bits for S[1:0] in case of common status error.
0 - Normal Operation
1 - Common Error

CE status bits report command errors. Description of what is reported can be seen below:
0 - Normal Operation
1 - Command Error

The following access errors are detected and reported:

- Write request when EOI is active, excluding write to reset activation register.
- Read or write to SPI_TMODE addresses when SPI_TMODE is inactive. (Factory only)
- Read or write request to unused/undefined address.
- Write request to read-only register.

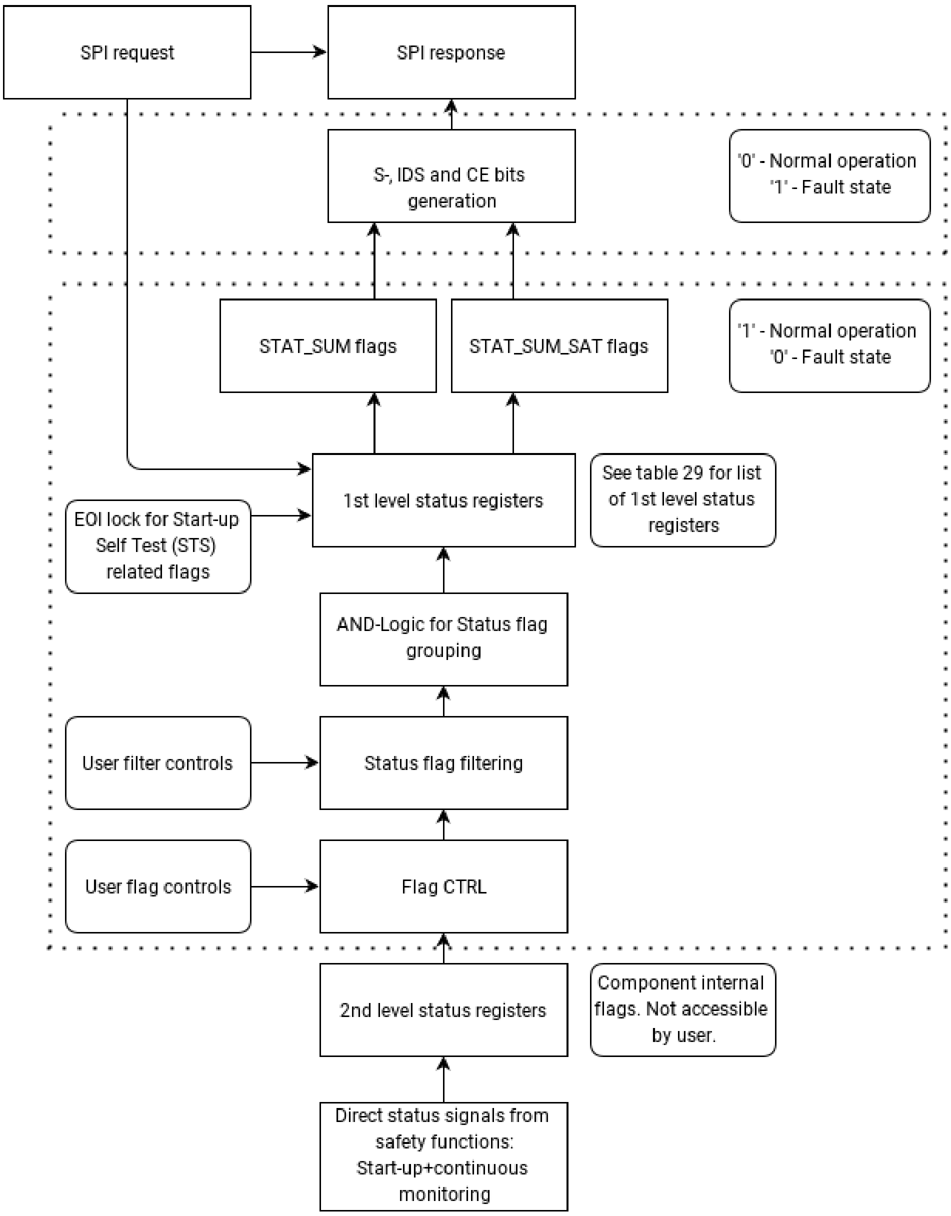

Figure 16 Status flag logic

6.5 Cyclic Redundancy Check (CRC)

6.5.1 SPI48BF CRC

SPI48BF uses 8-bit CRC (CRC8). CRC is calculated from MSB towards LSB for 40 MSB bits of the frame, i.e. from bit 47 to 8. Generator polynomial is b100101111 (POLY:9) and calculation is initialized to b11111111. The start value shall be added in the front of MSB of SPI frame. Final CRC is the direct value of the calculation. Different handling of start value can be used as long the same results are achieved as by XOR first MSB's with start value.

Table 22 CRC definition for 48bit frames

Parameter	Value
Name	CRC-8
Width	8 bit
Poly	12F'h (generator polynom: $X^8+X^5+X^3+X^2+X+1$) 97'h (Koopman)
Start	FF'h

6.5.2 SPI32BF CRC

SPI32BF uses 3-bit CRC (CRC3). CRC is calculated from MSB towards LSB for 29 MSB bits of the frame, i.e. from bit 31 to 3. Generator polynomial is b1011 (POLY:4) and calculation is initialized to b101. The start value shall be added in the front of MSB of SPI frame. Final CRC is the direct value of the calculation. Different handling of start value can be used as long the same results are achieved as by XOR first MSB's with start value.

Table 23 CRC definition for 32bit frames

Parameter	Value
Name	CRC-3
Width	3 bit
Poly	B'h (Generator polynom: X^3+X+1) 5'h (Koopman)
Start	5'h

6.6 Operations

This chapter describes some common SPI operations.

6.6.1 32bit Mode Operations

Binary frame has been spaced as follows:
(TA9 TA8 TA[7:0] RW 0 FrTyp DATA[15:0] CRC3)

Table 24 32bit mode operations and their equivalent SPI frames

Title	Register	SPI Binary Frame	SPI Hex frame
EN_SENSOR	CTRL_MODE	0 0 00110101 1 0 0 0000000000000001 010	0x0D60000A
EOI	CTRL_MODE	0 0 00110101 1 0 0 0000000000000011 100	0x0D60001C
Set LPF0 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000000000000 110	0x09600006
Set LPF0 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000000000000 000	0x09A00000
Set LPF1 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000001001001 100	0x0960024C
Set LPF1 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000001001001 010	0x09A0024A
Set LPF2 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000010010010 010	0x09600492

Set LPF2 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000010010010 100	0x09A00494
Set LPF3 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000011011011 000	0x096006D8
Set LPF3 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000011011011 110	0x09A006DE
Set RATE Dynamic Range to ±315°/s	CTRL_RATE	0 0 00101000 1 0 0 0010010000000000 000	0x0A212000
Set ACC Dynamic Range to ±80m/s²	CTRL_ACC12	0 0 00101001 1 0 0 0010010000000000 010	0x0A612002
Read RATE LPF setting	CTRL_FILT_RATE	0 0 00100101 0 0 0 0000000000000000 111	0x09400007
Read ACC LPF setting	CTRL_FILT_ACC12	0 0 00100110 0 0 0 0000000000000000 001	0x09800001
Read RATE_X1	RATE_X1	0 0 00000001 0 0 0 0000000000000000 001	0x00400001
Read RATE_Y1	RATE_Y1	0 0 00000010 0 0 0 0000000000000000 111	0x00800007
Read RATE_Z1	RATE_Z1	0 0 00000011 0 0 0 0000000000000000 101	0x00C00005
Read ACC_X1	ACC_X1	0 0 00000100 0 0 0 0000000000000000 000	0x01000000
Read ACC_Y1	ACC_Y1	0 0 00000101 0 0 0 0000000000000000 010	0x01400002
Read ACC_Z1	ACC_Z1	0 0 00000110 0 0 0 0000000000000000 100	0x01800004
Read ACC_X3	ACC_X3	0 0 00000111 0 0 0 0000000000000000 110	0x01C00006
Read ACC_Y3	ACC_Y3	0 0 00001000 0 0 0 0000000000000000 101	0x02000005
Read ACC_Z3	ACC_Z3	0 0 00001001 0 0 0 0000000000000000 111	0x02400007
Read RATE_X2	RATE_X2	0 0 00001010 0 0 0 0000000000000000 001	0x02800001
Read RATE_Y2	RATE_Y2	0 0 00001011 0 0 0 0000000000000000 011	0x02C00003
Read RATE_Z2	RATE_Z2	0 0 00001100 0 0 0 0000000000000000 110	0x03000006
Read ACC_X2	ACC_X2	0 0 00001101 0 0 0 0000000000000000 100	0x03400004
Read ACC_Y2	ACC_Y2	0 0 00001110 0 0 0 0000000000000000 010	0x03800002
Read ACC_Z2	ACC_Z2	0 0 00001111 0 0 0 0000000000000000 000	0x03C00000
Read Temperature	TEMP	0 0 00010000 0 0 0 0000000000000000 100	0x04000004
Read STAT_SUM	STAT_SUM	0 0 00010100 0 0 0 0000000000000000 111	0x05000007
Read STAT_SUM_SAT	STAT_SUM_SAT	0 0 00010101 0 0 0 0000000000000000 101	0x05400005
Read STAT_COM	STAT_COM	0 0 00010110 0 0 0 0000000000000000 011	0x05800003
Read STAT_RATE_COM	STAT_RATE_COM	0 0 00010111 0 0 0 0000000000000000 001	0x05C00001
Read STAT_RATE_X	STAT_RATE_X	0 0 00011000 0 0 0 0000000000000000 010	0x06000002
Read STAT_RATE_Y	STAT_RATE_Y	0 0 00011001 0 0 0 0000000000000000 000	0x06400000
Read STAT_RATE_Z	STAT_RATE_Z	0 0 00011010 0 0 0 0000000000000000 110	0x06800006
Read STAT_ACC_X	STAT_ACC_X	0 0 00011011 0 0 0 0000000000000000 100	0x06C00004
Read STAT_ACC_Y	STAT_ACC_Y	0 0 00011100 0 0 0 0000000000000000 001	0x07000001
Read STAT_ACC_Z	STAT_ACC_Z	0 0 00011101 0 0 0 0000000000000000 011	0x07400003

6.6.2 48bit Mode Operations

Binary frame has been spaced as follows:

(TA9 TA8 TA[7:0] RW 0 FrTyp AE[6:0] DATA[19:0] CRC8)

Table 25 48bit mode operations and their equivalent SPI frames

Title	Register	SPI Binary Frame	SPI Hex frame
EOI	CTRL_MODE	0 0 00110101 1 0 1 0000000 00000000000000000011 10001101	0x0D680000038D
EN_SENSOR	CTRL_MODE	0 0 00110101 1 0 1 0000000 00000000000000000001 11010011	0x0D68000001D3
Set LPF0 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 00000000000000000000 00010110	0x096800000016
Set LPF0 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 00000000000000000000 00100000	0x09A800000020
Set LPF1 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 00000000000001001001 10001000	0x096800004988
Set LPF1 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 00000000000001001001 10111110	0x09A8000049BE

Set LPF2 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 0000000000010010010 00000101	0x096800009205
Set LPF2 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 0000000000010010010 00110011	0x09A800009233
Set LPF3 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 0000000000011011011 10011011	0x09680000DB9B
Set LPF3 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 0000000000011011011 10101101	0x09A80000DBAD
Set RATE Dynamic Range to ±315°/s	CTRL_RATE	0 0 00101000 1 0 1 0000000 0000010010000000000 10100110	0x0A28002400A6
Set ACC Dynamic Range to ±80m/s²	CTRL_ACC12	0 0 00101001 1 0 1 0000000 0000010010000000000 01010001	0x0A6800240051
Read RATE LPF setting	CTRL_FILT_RATE	0 0 00100101 0 0 1 0000000 0000000000000000000 11111010	0x0948000000FA
Read ACC LPF setting	CTRL_FILT_ACC12	0 0 00100110 0 0 1 0000000 0000000000000000000 11001100	0x0988000000CC
Read RATE_X1	RATE_X1	0 0 00000001 0 0 1 0000000 0000000000000000000 10101100	0x0048000000AC
Read RATE_Y1	RATE_Y1	0 0 00000010 0 0 1 0000000 0000000000000000000 10011010	0x00880000009A
Read RATE_Z1	RATE_Z1	0 0 00000011 0 0 1 0000000 0000000000000000000 01101101	0x00C80000006D
Read ACC_X1	ACC_X1	0 0 00000100 0 0 1 0000000 0000000000000000000 11111001	0x0108000000F6
Read ACC_Y1	ACC_Y1	0 0 00000101 0 0 1 0000000 0000000000000000000 00000001	0x014800000001
Read ACC_Z1	ACC_Z1	0 0 00000110 0 0 1 0000000 0000000000000000000 00110111	0x018800000037
Read ACC_X3	ACC_X3	0 0 00000111 0 0 1 0000000 0000000000000000000 11000000	0x01C8000000C0
Read ACC_Y3	ACC_Y3	0 0 00001000 0 0 1 0000000 0000000000000000000 00101110	0x02080000002E
Read ACC_Z3	ACC_Z3	0 0 00001001 0 0 1 0000000 0000000000000000000 11011001	0x0248000000D9
Read RATE_X2	RATE_X2	0 0 00001010 0 0 1 0000000 0000000000000000000 11101111	0x0288000000EF
Read RATE_Y2	RATE_Y2	0 0 00001011 0 0 1 0000000 0000000000000000000 00011000	0x02C800000018
Read RATE_Z2	RATE_Z2	0 0 00001100 0 0 1 0000000 0000000000000000000 10000011	0x030800000083
Read ACC_X2	ACC_X2	0 0 00001101 0 0 1 0000000 0000000000000000000 01110100	0x034800000074
Read ACC_Y2	ACC_Y2	0 0 00001110 0 0 1 0000000 0000000000000000000 01000010	0x038800000042
Read ACC_Z2	ACC_Z2	0 0 00001111 0 0 1 0000000 0000000000000000000 10110101	0x03C8000000B5
Read Temperature	TEMP	0 0 00010000 0 0 1 0000000 0000000000000000000 10110001	0x0408000000B1
Read STAT_SUM	STAT_SUM	0 0 00010100 0 0 1 0000000 0000000000000000000 00011100	0x05080000001C
Read STAT_SUM_SAT	STAT_SUM_SAT	0 0 00010101 0 0 1 0000000 0000000000000000000 11101011	0x0548000000EB
Read STAT_COM	STAT_COM	0 0 00010110 0 0 1 0000000 0000000000000000000 11011101	0x0588000000DD
Read STAT_RATE_COM	STAT_RATE_COM	0 0 00010111 0 0 1 0000000 0000000000000000000 00101010	0x05C80000002A
Read STAT_RATE_X	STAT_RATE_X	0 0 00011000 0 0 1 0000000 0000000000000000000 11000100	0x0608000000C4
Read STAT_RATE_Y	STAT_RATE_Y	0 0 00011001 0 0 1 0000000 0000000000000000000 00110011	0x064800000033
Read STAT_RATE_Z	STAT_RATE_Z	0 0 00011010 0 0 1 0000000 0000000000000000000 00000101	0x068800000005
Read STAT_ACC_X	STAT_ACC_X	0 0 00011011 0 0 1 0000000 0000000000000000000 11110010	0x06C8000000F2
Read STAT_ACC_Y	STAT_ACC_Y	0 0 00011100 0 0 1 0000000 0000000000000000000 01101001	0x070800000069
Read STAT_ACC_Z	STAT_ACC_Z	0 0 00011101 0 0 1 0000000 0000000000000000000 10011110	0x07480000009E

7 Register Definition

7.1 Register Map User Guide

7.1.1 Value and address formats

Several value formats are used in this data sheet. These are described in table 24 below.

Table 26 Value formats

Decimal	5-bit decimal	5-bit signed hex	5-bit binary
13	5d13	5h0D	5b01101
-13	5d-13	5h13	5b10011

All user essential content of SCH1600 ASIC is mirrored to Public banks listed below.

15h0000
15h0010
15h0020
15h0030

The detailed register content is explained in next chapter. The whole ASIC content can be accessed only in factory test mode.
Address is the 4bit offset within bank. Final Public Address is formed by adding Address Hex to end of Public Bank Hex, example:
STAT_SUM
- Bank Hex: 15h0010
- Address offset 4h4
- Public Address: 15h0010 + 4h4 = 15h0014

7.1.2 Register Map overview

Banks, address offsets and data width can be seen in table 26 below.

Green: Data registers
Red: Counters
Blue: Status registers
Orange: Control registers
Purple: Misc registers

Table 27 Register map overview

Adress	15h0000	Data width	15h0010	Data width	15h0020	Data width	15h0030	Data width
4h0	Reserved	-	TEMP	16bit	Reserved	-	Reserved	-
4h1	RATE_X1	20bit	RATE_DCNT	12bit	Reserved	-	Reserved	-
4h2	RATE_Y1	20bit	ACC_DCNT	14bit	Reserved	-	Reserved	-
4h3	RATE_Z1	20bit	FREQ_CNTR	16bit	Reserved	-	CTRL_USER_IF	16bit
4h4	ACC_X1	20bit	STAT_SUM	16bit	Reserved	-	CTRL_ST	13bit
4h5	ACC_Y1	20bit	STAT_SUM_SAT	16bit	CTRL_FILT_RATE	9bit	CTRL_MODE	4bit
4h6	ACC_Z1	20bit	STAT_COM	16bit	CTRL_FILT_ACC12	9bit	CTRL_RESET	4bit
4h7	ACC_X3	20bit	STAT_RATE_COM	16bit	CTRL_FILT_ACC3	9bit	SYS_TEST	16bit
4h8	ACC_Y3	20bit	STAT_RATE_X	16bit	CTRL_RATE	15bit	SPARE_1	16bit
4h9	ACC_Z3	20bit	STAT_RATE_Y	16bit	CTRL_ACC12	15bit	SPARE_2	16bit
4hA	RATE_X2	20bit	STAT_RATE_Z	16bit	CTRL_ACC3	3bit	SPARE_3	16bit
4hB	RATE_Y2	20bit	STAT_ACC_X	16bit	CTRL_RATE_FLAG_1	15bit	ASIC_ID	12bit
4hC	RATE_Z2	20bit	STAT_ACC_Y	16bit	CTRL_RATE_FLAG_2	15bit	COMP_ID	16bit
4hD	ACC_X2	20bit	STAT_ACC_Z	16bit	CTRL_ACC_FLAG_1	15bit	SN_ID1	16bit
4hE	ACC_Y2	20bit	STAT_SYNC_ACTIVE	12bit	CTRL_ACC_FLAG_2	15bit	SN_ID2	16bit
4hF	ACC_Z2	20bit	STAT_INFO	9bit	Reserved	-	SN_ID3	16bit

7.2 Sensor Data Block

D1/D0 is specified according to Safe SPI standard.
D is the sensor data bit identifying if response contains sensor data or not (i.e. identifying frame format for response.
D=0: no sensor data, e.g. status data or read back of configuration data
D=1: sensor data format

Table 28 Overview of Sensor Data Block

Register Name	Register Description	R/RW	Public addr
RATE_X1	Output, x-axis gyroscope, interpolation, common low pass filter with RATE_X2	R	15h0001, D1
RATE_Y1	Output, y-axis gyroscope, interpolation, common low pass filter with RATE_Y2	R	15h0002, D1
RATE_Z1	Output, z-axis gyroscope, interpolation, common low pass filter with RATE_Z2	R	15h0003, D1
ACC_X1	Output, x-axis accelerometer, interpolation, common low pass filter with ACC_X2	R	15h0004, D1
ACC_Y1	Output, y-axis accelerometer, interpolation, common low pass filter with ACC_Y2	R	15h0005, D1
ACC_Z1	Output, z-axis accelerometer, interpolation, common low pass filter with ACC_Z2	R	15h0006, D1
ACC_X3	Output, x-axis accelerometer, redundant signal path with interpolation and individually configurable low pass filter setting.	R	15h0007, D1
ACC_Y3	Output, y-axis accelerometer, redundant signal path with interpolation and individually configurable low pass filter setting.	R	15h0008, D1
ACC_Z3	Output, z-axis accelerometer, redundant signal path with interpolation and individually configurable low pass filter setting.	R	15h0009, D1
RATE_X2	Output, x-axis gyroscope, configurable decimation filter, common low pass filter with RATE_X1	R	15h000A, D1
RATE_Y2	Output, y-axis gyroscope, configurable decimation filter, common low pass filter with RATE_Y1	R	15h000B, D1
RATE_Z2	Output, z-axis gyroscope, configurable decimation filter, common low pass filter with RATE_Z1	R	15h000C, D1
ACC_X2	Output, x-axis accelerometer, configurable decimation filter, common low pass filter with ACC_X1	R	15h000D, D1
ACC_Y2	Output, y-axis accelerometer, configurable decimation filter, common low pass filter with ACC_Y1	R	15h000E, D1
ACC_Z2	Output, z-axis accelerometer, configurable decimation filter, common low pass filter with ACC_Z1	R	15h000F, D1
TEMP	Output, temperature sensor	R	15h0010, D1

7.2.1 Example of Angular Rate Data Conversion

Interpolated output of X Rate is used as example. Data is stored as 2's complement to register.

7.2.1.1 16bit Mode

In 16bit mode, default sensitivity is 50LSB/°/s
If Rate X register (15h0001) read result is Rate X = 802**FFE0**7h, content is converted to angular rate as follows:

- 802h = 1 0 0 0000 0001 0b (contains D bit, address bits and first Status bit)
- FFE0h = 1111 1111 1110 0000b (Rate X register content)
  - FFE0h in 2's complement format = -32d
  - Angular rate = -32LSB/sensitivity = -32LSB/ (100LSB/(°/s)) = -0.32°/s
- 7h = CRC of 802FFE0h

7.2.1.2 20bit Mode

In 20bit mode, default sensitivity is 800LSB/°/s
If Rate X register (15h0001) read result is Rate X =80200**FFE00**ADh, content is converted to angular rate as follows:
- 80200h = 1 0 0 0000 0001 0 0 00 0000 0b (contains D-bit, address-, status- and DCNT bits and one empty bit)
- FFE00h = 1111 1111 1110 0000 0000b (Rate X register content)
  - FFE00h in 2's complement format = -512d
  - Angular rate = LSB/sensitivity = -512LSB/ (1600LSB/(°/s)) = -0.32°/s
- Adh = CRC of 80200FFE00h

7.2.2 Example of Acceleration Data Conversion

Interpolated output of ACC Y is used as example. Data is stored as 2's complement to register.

7.2.2.1 16bit Mode

In 16bit mode, default sensitivity is 200 LSB/(m/s^2)
If ACC Y register (15h0005) read result is ACC Y= 80A**00DC**6h, content is converted to acceleration as follows:
- 80Ah = 1 0 0 0000 0101 0b (contains D bit, address bits and first Status bit)
- 00DCh =0000 0000 1101 1100b (ACC Y register content)
  - 00DCh in 2's complement format = 220d
  - Acceleration = 220LSB/sensitivity = 220LSB/ (200LSB/(m/s^2)) ≈ 1.1m/s^2
- 6h = CRC of 80A00DC0h

7.2.2.2 20bit Mode

In 20bit mode, default sensitivity is 3200LSB/(m/s^2)
If ACC Y register (15h0005) read result is ACC Y= 80A00**00DC0**DBh, content is converted to acceleration as follows:
- 80A00h = 1 0 0 0000 0101 0 0 00 0000 0b (contains D-bit, address-, status- and DCNT bits and one empty bit)
- 00DC0h =0000 0000 1101 1100 0000b (ACC Y register content)
  - 00DC0h in 2's complement format = 3520d
  - Acceleration= 3520LSB/sensitivity = 3520LSB/ (3200LSB/(m/s^2)) ≈ 1.1m/s^2
- DBh = CRC of 80A00DC000h

7.2.3 Example of Temperature Data Conversion

7.2.3.1 16bit Mode

Temperature signal sensitivity is 100LSB/°C
If TEMP register (15h0010) read result is TEMP = 820**00DC**5h, content is converted to temperature as follows:
- 820h = 1 0 0 0001 0000 0b (contains D bit, address bits and first Status bit)
- 00DCh =0000 0000 1101 1100b (TEMP register content)
  - 00DCh in 2's complement format = 220d
  - Temperature= 220LSB/sensitivity = 220LSB/ (100LSB/°C) = 2.2°C
- 5h = CRC of 82000DC0h

7.2.3.2 20bit Mode

The temperature data is always 16bit wide. In 20bit mode, this needs to be taken into account. The user has two options:
1. Change frame type for temperature register read to 32bit by changing FT bit of previous MOSI frame from 1 to 0. Then, convert TEMP data as explained in previous chapter 7.2.3.1
2. Read TEMP register in 20bit mode. As data is only 16bits wide, the remaining LSBs will be all zeroes and they need to be dropped. After that, register content can be converted in similar manner as explained in previous chapter 7.2.3.1

If TEMP register (15h0010) read result is TEMP = 82000**00DC0**Eah, content is converted to temperature (°C) as follows:
- 82000h = 1 0 0 0001 0000 0 0 00 0000 0b (contains D-bit, address-, status- and DCNT bits and one empty bit)
- Drop out **0**h
- 00DCh =0000 0000 1101 1100b (TEMP register content)
    - 00DCh in 2's complement format = 220d
    - Temperature= 220LSB/sensitivity = 220LSB/ (100LSB/°C) = 2.2°C
- Eah = CRC of 82000DC000h

7.3 Sensor Status Block

Table 29 Overview of Sensor Status Block

Register Name	Register Description	R/RW	Public addr
RATE_DCNT	Data counter for RATE_XYZ2	R	15h0011, D0
ACC_DCNT	Data Counter for ACC_XYZ	R	15h0012, D0
FREQ_CNTR	Frequency / sample time counter	R	15h0013, D0
STAT_SUM	Status Summary for non-saturation related flags	R	15h0014, D0
STAT_SUM_SAT	Status summary for saturation flags	R	15h0015, D0
STAT_COM	Common Status flags, incl. TEMP, 1st level status register	R	15h0016, D0
STAT_RATE_COM	Common gyro status flags (primary channel), 1st level status register	R	15h0017, D0
STAT_RATE_X	RATE_X status flags, 1st level status register	R	15h0018, D0
STAT_RATE_Y	RATE_Y status flags, 1st level status register	R	15h0019, D0
STAT_RATE_Z	RATE_Z status flags, 1st level status register	R	15h001A, D0
STAT_ACC_X	ACC_X status flags, 1st level status register	R	15h001B, D0
STAT_ACC_Y	ACC_Y status flags, 1st level status register	R	15h001C, D0
STAT_ACC_Z	ACC_Z status flags, 1st level status register	R	15h001D, D0
STAT_SYNC_ACTIVE	Status of SYNC on each channel	R	15h001E, D0
STAT_INFO	Low power mode indications	R	15h001F, D0
Reserved	Reserved	R	15h0020, D0

7.3.1 Data counters

Table 30 Data Counter registers

Register Name	Register Description	R/RW	Public addr
RATE_DCNT	Data counter for RATE_XYZ2 output channel	R	15h0011, D0
ACC_DCNT	Data Counter for ACC_XYZ2 output channel	R	15h0012, D0

Table 31 RATE_DCNT register Bit description

Bit Name	Bit Description	Bits	Reset Value
RATE_Z_DCNT	4-bit data counter for RATE_Z output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[11:8]	4b0000
RATE_Y_DCNT	4-bit data counter for RATE_Y output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[7:4]	4b0000
RATE_X_DCNT	4-bit data counter for RATE_X output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[3:0]	4b0000

Table 32 ACC_DCNT register Bit description

Bit Name	Bit Description	Bits	Reset Value
ACC_Z_DCNT	4-bit data counter for ACC_Z output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[11:8]	4b0000
ACC_Y_DCNT	4-bit data counter for ACC_Y output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[7:4]	4b0000
ACC_X_DCNT	4-bit data counter for ACC_X output Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[3:0]	4b0000

7.3.2 Frequency counter / timestamp

Table 33 Register for frequency counter bits

Register Name	Register Description	R/RW	Public addr
FREQ_CNTR	Frequency / sample time counter	R	15h0013, D0

Table 34 FREQ_CNTR_BIT register Bit description

Bit Name	Bit Description	Bits
FREQ_CNTR_BIT	14bit counter. Counter value is updated (+1) with every 16th rising edge of master clock. If counter is not reset by reading FREQ_CNTR register and the counter reaches 14d16383, it rolls back to zero.	[13:0]

7.3.3 Status Summary

Table 35 Status summary register

Register Name	Register Description	Public addr
STAT_SUM	Status Summary for non-saturation related flags	15h0014, D0

Table 36 STAT_SUM register Bit description

Bit Name	Bit Description	Bits	Normal operation value
Reserved	Reserved	[15:8]	8b11111111
STAT_SUM_CMN	Common Status	[7:7]	1b1
STAT_SUM_RATE_X	RATE_X Status	[6:6]	1b1
STAT_SUM_RATE_Y	RATE_Y Status	[5:5]	1b1
STAT_SUM_RATE_Z	RATE_Z Status	[4:4]	1b1
STAT_SUM_ACC_X	ACC_X Status	[3:3]	1b1
STAT_SUM_ACC_Y	ACC_Y Status	[2:2]	1b1
STAT_SUM_ACC_Z	ACC_Z Status	[1:1]	1b1
SUM_STAT_INIT_RDY	Initialization Ready	[0:0]	1b1

7.3.4 Saturation Status Summary

Table 37 Saturation summary register

Register Name	Register Description	Public addr
STAT_SUM_SAT	Status summary for saturation flags	15h0015, D0

Table 38 STAT_SUM_SAT register Bit description

Bit Name	Bit Description	Bits	Normal operation value
Reserved	Reserved	[15:15]	1b1
STAT_SUM_SAT_RATE_X1	Saturation status for output RATE_X1	[14:14]	1b1
STAT_SUM_SAT_RATE_Y1	Saturation status for output RATE_Y1	[13:13]	1b1
STAT_SUM_SAT_RATE_Z1	Saturation status for output RATE_Z1	[12:12]	1b1
STAT_SUM_SAT_ACC_X1	Saturation status for output ACC_X1	[11:11]	1b1
STAT_SUM_SAT_ACC_Y1	Saturation status for output ACC_Y1	[10:10]	1b1
STAT_SUM_SAT_ACC_Z1	Saturation status for output ACC_Z1	[9:9]	1b1
STAT_SUM_SAT_ACC_X3	Saturation status for output ACC_X3	[8:8]	1b1
STAT_SUM_SAT_ACC_Y3	Saturation status for output ACC_Y3	[7:7]	1b1
STAT_SUM_SAT_ACC_Z3	Saturation status for output ACC_Z3	[6:6]	1b1
STAT_SUM_SAT_RATE_X2	Saturation status for output RATE_X2	[5:5]	1b1
STAT_SUM_SAT_RATE_Y2	Saturation status for output RATE_Y2	[4:4]	1b1
STAT_SUM_SAT_RATE_Z2	Saturation status for output RATE_Z2	[3:3]	1b1
STAT_SUM_SAT_ACC_X2	Saturation status for output ACC_X2	[2:2]	1b1
STAT_SUM_SAT_ACC_Y2	Saturation status for output ACC_Y2	[1:1]	1b1
STAT_SUM_SAT_ACC_Z2	Saturation status for output ACC_Z2	[0:0]	1b1

7.3.5 Common Status

Table 39 Common status register

Register Name	Register Description	Public addr
STAT_COM	Common Status flags, incl. TEMP	15h0016, D0

Table 40 STAT_COM register Bit description

Bit Name	Bit Description	Bits	Normal operation value
Reserved	Reserved	[15:11]	5b11111
MCLK_OK	Status of ASIC master clock.	[10:10]	1b1
DUAL_CLOCK_OK	Clock Reference status flag	[9:9]	1b1
DSP_OK	Register content integrity status flag	[8:8]	1b1
SVM_OK	SVM Self-test status flag	[7:7]	1b1
HV_CP_OK	HV Charge Pump status flag	[6:6]	1b1
SUPPLY_OK	Voltage supply status flag	[5:5]	1b1
TEMP_OK	Temperature sensor channel status flag	[4:4]	1b1
NMODE_OK	Normal Mode status flag	[3:3]	1b1
NVM_STS_OK	NVM Start-up Self-test status flag	[2:2]	1b1
CMN_STS_OK	Start-up Self-test status for TEMP and common digital blocks.	[1:1]	1b1
CMN_STS_RDY	Start-up Self-test ready for TEMP and common digital blocks.	[0:0]	1b1

7.3.6 Rate Common Status

Table 41 Rate Common Status register

Register Name	Register Description	Public addr
STAT_RATE_COM	Common gyro status flags (primary channel)	15h0017, D0

Table 42 STAT_RATE_COM register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:8]	8b11111111
PRI_AGC_OK	Gyro primary loop status	[7:7]	1b1
GYRO_PRI_OK	Gyro primary loop status	[6:6]	1b1
PRI_START_OK	Gyro primary loop start-up status	[5:5]	1b1
GYRO_HV_OK	Gyro High Voltage status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
GYRO_SD_STS_OK	Gyro Shield Detection Start-up Self-test status	[2:2]	1b1
GYRO_BOND_STS_OK	Gyro Bond wire Start-up Self-test status	[1:1]	1b1
GYRO_STS_RDY_OK	Gyro Start-up Self-test ready status flag	[0:0]	1b1

7.3.7 Rate Status XYZ

Table 43 Rate status registers

Register Name	Register Description	R/RW	Public addr
STAT_RATE_X	RATE_X status flags	R	15h0018, D0
STAT_RATE_Y	RATE_Y status flags	R	15h0019, D0
STAT_RATE_Z	RATE_Z status flags	R	15h001A, D0

Table 44 STAT_RATE_X register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:10]	6b111111
RATE_DEC_X_SAT_OK	Decimated Rate (X2) Output saturation.	[9:9]	1b1
RATE_INTP_X_SAT_OK	Interpolated Rate (X1) Output saturation.	[8:8]	1b1
RESERVED	Reserved	[7:7]	1b1
RATE_X_STC_DIG_OK	Status of RATE X Digital Continuous Self-test	[6:6]	1b1
RATE_X_STC_ANA_OK	Status of RATE X Analog Continuous Self-test	[5:5]	1b1
RATE_X_QC_OK	Status of rate X signal	[4:4]	1b1
RESERVED	Reserved	[3:2]	1b1
RESERVED	Reserved	[1:1]	1b1
RESERVED	Reserved	[0:0]	1b1

Table 45 STAT_RATE_Y register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:10]	6b111111
RATE_DEC_Y_SAT_OK	Decimated Rate (Y2) Output saturation.	[9:9]	1b1
RATE_INTP_Y_SAT_OK	Interpolated Rate (Y1) Output saturation.	[8:8]	1b1
RESERVED	Reserved	[7:7]	1b1
RATE_Y_STC_DIG_OK	Status of RATE Y Digital Continuous Self-test	[6:6]	1b1
RATE_Y_STC_ANA_OK	Status of RATE Y Analog Continuous Self-test	[5:5]	1b1
RATE_Y_QC_OK	Status of rate Y signal	[4:4]	1b1
RESERVED	Reserved	[3:2]	1b1
RESERVED	Reserved	[1:1]	1b1
RESERVED	Reserved	[0:0]	1b1

Table 46 STAT_RATE_Z register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:10]	6b111111
RATE_DEC_Z_SAT_OK	Decimated Rate (Z2) Output saturation.	[9:9]	1b1
RATE_INTP_Z_SAT_OK	Interpolated Rate (Z1) Output saturation.	[8:8]	1b1
RESERVED	Reserved	[7:7]	1b1
RATE_Z_STC_DIG_OK	Status of RATE Z Digital Continuous Self-test	[6:6]	1b1
RATE_Z_STC_ANA_OK	Status of RATE Z Analog Continuous Self-test	[5:5]	1b1
RATE_Z_QC_OK	Status of rate Z signal	[4:4]	1b1
RESERVED	Reserved	[3:2]	1b1
RESERVED	Reserved	[1:1]	1b1
RESERVED	Reserved	[0:0]	1b1

7.3.8 ACC Status XYZ

Table 47 ACC Status registers

Register Name	Register Description	R/RW	Public addr
STAT_ACC_X	ACC_X status flags	R	15h001B, D0
STAT_ACC_Y	ACC_Y status flags	R	15h001C, D0
STAT_ACC_Z	ACC_Z status flags	R	15h001D, D0

Table 48 STAT_ACC_X register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:11]	5b11111
ACC_X3_SAT_OK	ACC_X3 output saturation.	[10:10]	1b1
ACC_X_DEC_SAT_OK	Decimated ACC (X2) output saturation.	[9:9]	1b1
ACC_X_INTP_SAT_OK	Interpolated ACC (X1) output saturation.	[8:8]	1b1
ACC_X_STC_DIG_OK	Accelerometer X Axis Continuous Self-test status 4	[7:7]	1b1
ACC_X_STC_TCAP_OK	Accelerometer X Axis Test-Cap Continuous Self-test status	[6:6]	1b1
ACC_X_STC_SDD_OK	Accelerometer X Axis Continuous Self-test status 2	[5:5]	1b1
ACC_X_STC_N_OK	Accelerometer X Axis Tone Continuous Self-test status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
ACC_X_SD_STS_OK	Accelerometer X Axis Shield Detection Start-up Self-test status	[2:2]	1b1
ACC_X_STS_OK	Accelerometer X Axis Start-up Self-test status	[1:1]	1b1
ACC_X_STS_RDY_OK	Accelerometer X Axis Start-up Self-test ready	[0:0]	1b1

Table 49 STAT_ACC_Y register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:11]	5b11111
ACC_Y3_SAT_OK	ACC_Y3 output saturation.	[10:10]	1b1
ACC_Y_DEC_SAT_OK	Decimated ACC (Y2) output saturation.	[9:9]	1b1
ACC_Y_INTP_SAT_OK	Interpolated ACC (Y1) output saturation.	[8:8]	1b1
ACC_Y_STC_DIG_OK	Accelerometer Y Axis Continuous Self-test status 4	[7:7]	1b1
ACC_Y_STC_TCAP_OK	Accelerometer Y Axis Test-Cap Continuous Self-test status	[6:6]	1b1
ACC_Y_STC_SDD_OK	Accelerometer Y Axis Continuous Self-test status 2	[5:5]	1b1
ACC_Y_STC_N_OK	Accelerometer Y Axis Tone Continuous Self-test status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
ACC_Y_SD_STS_OK	Accelerometer Y Axis Shield Detection Start-up Self-test status	[2:2]	1b1
ACC_Y_STS_OK	Accelerometer Y Axis Start-up Self-test status	[1:1]	1b1
ACC_Y_STS_RDY_OK	Accelerometer Y Axis Start-up Self-test ready	[0:0]	1b1

Table 50 STAT_ACC_Z register Bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:11]	15b11111
ACC_Z3_SAT_OK	ACC_Z3 output saturation.	[10:10]	1b1
ACC_Z_DEC_SAT_OK	Decimated ACC (Z2) output saturation.	[9:9]	1b1
ACC_Z_INTP_SAT_OK	Interpolated ACC (Z1) output saturation.	[8:8]	1b1
ACC_Z_STC_DIG_OK	Accelerometer Z Axis Continuous Self-test status 4	[7:7]	1b1
ACC_Z_STC_TCAP_OK	Accelerometer Z Axis Test-Cap Continuous Self-test status	[6:6]	1b1
ACC_Z_STC_SDD_OK	Accelerometer Z Axis Continuous Self-test status 2	[5:5]	1b1
ACC_Z_STC_N_OK	Accelerometer Z Axis Tone Continuous Self-test status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
ACC_Z_SD_STS_OK	Accelerometer Z Axis Shield Detection Start-up Self-test status	[2:2]	1b1
ACC_Z_STS_OK	Accelerometer Z Axis Start-up Self-test status	[1:1]	1b1
ACC_Z_STS_RDY_OK	Accelerometer Z Axis Start-up Self-test ready	[0:0]	1b1

7.3.9 Additional Status registers

Table 51 Additional status registers

Register Name	Register Description	R/RW	Public addr
STAT_SYNC_ACTIVE	Status of SYNC on each channel	R	15h001E, D0
STAT_INFO	Low power mode indications	R	15h001F, D0
Reserved	Reserved	-	15h0020, D0

Table 52 STAT_SYNC_ACTIVE register Bit description

Bit Name	Bit Description	Bits	Reset value
SYNC_ACTIVE_ACC_Z2	SYNC active in output ACC_Z2	[11:11]	1b0
SYNC_ACTIVE_ACC_Y2	SYNC active in output ACC_Y2	[10:10]	1b0
SYNC_ACTIVE_ACC_X2	SYNC active in output ACC_X2	[9:9]	1b0
SYNC_ACTIVE_RATE_Z2	SYNC active in output RATE_Z2	[8:8]	1b0
SYNC_ACTIVE_RATE_Y2	SYNC active in output RATE_Y2	[7:7]	1b0
SYNC_ACTIVE_RATE_X2	SYNC active in output RATE_X2	[6:6]	1b0
SYNC_ACTIVE_ACC_Z1	SYNC active in output ACC_Z1	[5:5]	1b0
SYNC_ACTIVE_ACC_Y1	SYNC active in output ACC_Y1	[4:4]	1b0
SYNC_ACTIVE_ACC_X1	SYNC active in output ACC_X1	[3:3]	1b0
SYNC_ACTIVE_RATE_Z1	SYNC active in output RATE_Z1	[2:2]	1b0
SYNC_ACTIVE_RATE_Y1	SYNC active in output RATE_Y1	[1:1]	1b0
SYNC_ACTIVE_RATE_X1	SYNC active in output RATE_X1	[0:0]	1b0

Table 53 STAT_INFO register Bit description

Bit Name	Bit Description	Bits	Reset value
Reserved	Reserved	[8:7]	1b0
Reserved	Reserved	[4:3]	1b0
Reserved	Reserved	[6:5]	1b0
ACC_LPM_OK	Accelerometer in Low Power Mode	[2:2]	1b0
RATE_LPM_OK	Gyroscope in Low Power Mode	[1:1]	1b0
SENSOR_LPM_OK	Start-up State Machine in Sensor Low Power Mode	[0:0]	1b0

7.4 Sensor Control Block

Table 54 Sensor Control Block register overview

Register Name	Register Description	R/RW	Public addr
Reserved	Reserved	RW	15h0021, D0
CTRL_FILT_RATE	RATE_XYZ Filter settings. Common filter for each axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0025, D0
CTRL_FILT_ACC12	ACC filter setting. Common filter for each ACC axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0026, D0
CTRL_FILT_ACC3	Filter setting for ACC_X3, ACC_Y3 and ACC_Z3.	RW	15h0027, D0
CTRL_RATE	Settings for Gyro post-processing decimation ratio and shift value (dynamic range)	RW	15h0028, D0
CTRL_ACC12	Settings for ACC_X12, ACC_Y12, ACC_Z12 post-processing decimation ratio and shift value (dynamic range)	RW	15h0029, D0
CTRL_ACC3	Settings for ACC_X3, ACC_Y3, ACC_Z3 post-processing shift value (dynamic range)	RW	15h002A, D0
CTRL_RATE_FLAG_1	RATE_XYZ Pre PP SAT_OK Filter user conf	RW	15h002B, D0
CTRL_RATE_FLAG_2	RATE_XYZ PP SAT_OK Filter user conf	RW	15h002C, D0
CTRL_ACC_FLAG_1	ACC_XYZ Pre PP SAT_OK Filter user conf	RW	15h002D, D0
CTRL_ACC_FLAG_2	ACC_XYZ PP SAT_OK Filter user conf	RW	15h002E, D0
CTRL_USER_IF	User controls for SYNC, Data Ready, Strength of SPI PD/PU, slew rate ctrl, hi-speed	RW	15h0033, D0
CTRL_ST	Self test controls (enable ST and/or request STS)	RW	15h0034, D0
CTRL_MODE	Test mode, EOI, EN_SENSOR	RW	15h0035, D0
CTRL_RESET	SPI soft reset command	RW	15h0036, D0
SYS_TEST	Empty register for testing read/write	RW	15h0037, D0

7.4.1 Filter settings

Table 55 Filter setting registers

Register Name	Register Description	R/RW	Public addr
CTRL_FILT_RATE	RATE_XYZ Filter settings. Common filter for each axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0025, D0
CTRL_FILT_ACC12	ACC filter setting. Common filter for each ACC axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0026, D0
CTRL_FILT_ACC3	Filter setting for ACC_X3, ACC_Y3 and ACC_Z3.	RW	15h0027, D0

For detailed Filter characteristics, please refer table 9

Table 56 Bits for setting of filters.

Name	Bits	Nominal Cut-off Frequency (-3dB)
LPF0	'000'	68Hz (default)
LPF1	'001'	30Hz
LPF2	'010'	13Hz
LPF3	'011'	280Hz
LPF4	'100'	370Hz
LPF5	'101'	235Hz
LPF6	'110'	TBD
LPF7	'111'	Bypass

Table 57 CTRL_FILT_RATE register Bit description

Bit Name	Bit Description	Bits	Reset Value
FILT_SEL_RATE_Z	Filter setting for RATE_Z1 and RATE_Z2 outputs	[8:6]	3b000
FILT_SEL_RATE_Y	Filter setting for RATE_Y1 and RATE_Y2 outputs	[5:3]	3b000
FILT_SEL_RATE_X	Filter setting for RATE_X1 and RATE_X2 outputs	[2:0]	3b000

Table 58 CTRL_FILT_ACC12 register Bit description

Bit Name	Bit Description	Bits	Reset Value
FILT_SEL_ACC_Z12	Filter setting for ACC_Z1 and ACC_Z2 outputs	[8:6]	3b000
FILT_SEL_ACC_Y12	Filter setting for ACC_Y1 and ACC_Y2 outputs	[5:3]	3b000
FILT_SEL_ACC_X12	Filter setting for ACC_X1 and ACC_X2 outputs	[2:0]	3b000

Table 59 CTRL_FILT_ACC3 register Bit description

Bit Name	Bit Description	Bits	Reset Value
FILT_SEL_ACC_Z3	Filter setting for ACC_Z3 output	[8:6]	3b000
FILT_SEL_ACC_Y3	Filter setting for ACC_Y3 output	[5:3]	3b000
FILT_SEL_ACC_X3	Filter setting for ACC_X3 output	[2:0]	3b000

7.4.2 Dynamic range and Decimation

Table 60 Registers for dynamic range and decimation setting

Register Name	Register Description	R/RW	Public addr
CTRL_RATE	Settings for Gyro post-processing decimation ratio and shift value (dynamic range)	RW	15h0028, D0
CTRL_ACC12	Settings for ACC_X12, ACC_Y12, ACC_Z12 post-processing decimation ratio and shift value (dynamic range)	RW	15h0029, D0
CTRL_ACC3	Settings for ACC_X3, ACC_Y3, ACC_Z3 post-processing shift value (dynamic range)	RW	15h002A, D0

Table 61 Bits for setting of RATE dynamic range

Name	Bits	Measurement range	Typical Electrical Headroom	Nominal Sensitivity, 16 bit	Nominal Sensitivity, 20bit
Undefined	'000'	-	n.a.	n.a.	n.a.
DYN1 (default)	'001'	±300 °/s	±327.5 °/s	100 LSB/°/s	1600 LSB/°/s
DYN2	'010'	±300 °/s	±327.5 °/s	100 LSB/°/s	1600 LSB/°/s
DYN3	'011'	±125 °/s	±163.75 °/s	200 LSB/°/s	3200 LSB/°/s
DYN4	'100'	±62.5 °/s	±81.875 °/s	400 LSB/°/s	6400 LSB/°/s

Table 62 Bits for setting of ACC12 dynamic range

Name	Bits	Measurement Range	Typical Electrical Headroom	Nominal Sensitivity, 16 bit	Nominal Sensitivity, 20bit
Undefined	'000'	-	n.a.	n.a.	n.a.
DYN1 (default)	'001'	±80 m/s^2	±163.4 m/s^2	200 LSB/m/s^2	3200 LSB/m/s^2
DYN2	'010'	±60 m/s^2	±81.92 m/s^2	400 LSB/ m/s^2	6400 LSB/m/s^2
DYN3	'011'	±30 m/s^2	± 40.96 m/s^2	800 LSB/m/s^2	12800 LSB/m/s^2
DYN4	'100'	±15 m/s^2	±20.48 m/s^2	1600 LSB/m/s^2	25600 LSB/m/s^2

Table 63 Bits for setting of ACC3 dynamic range

Name	Bits	Measurement Range	Typical Electrical Headroom	Nominal Sensitivity, 16 bit	Nominal Sensitivity, 20bit
DYN0 (default)	'000'	±80 m/s^2	±260 m/s^2	100 LSB/m/s^2	1600 LSB/m/s^2
DYN1	'001'	±80 m/s^2	±163.4 m/s^2	200 LSB/m/s^2	3200 LSB/m/s^2
DYN2	'010'	±60 m/s^2	±81.92 m/s^2	400 LSB/ m/s^2	6400 LSB/m/s^2
DYN3	'011'	±30 m/s^2	± 40.96 m/s^2	800 LSB/m/s^2	12800 LSB/m/s^2
DYN4	'100'	±15 m/s^2	±20.48 m/s^2	1600 LSB/m/s^2	25600 LSB/m/s^2

Table 64 Bits for setting of Decimation Ratio

Name	Bits	Reduction Factor	Output sample rate	With Nominal F_PRIM (kHz)	f3dB (Hz)
DEC1	'000' (no decimation)	1	F_PRIM/2	11.8	NA
DEC2	'001'	2	F_PRIM/4	5.9	5975
DEC3	'010'	4	F_PRIM/8	2.95	2987
DEC4	'011'	8	F_PRIM/16	1.475	1494
DEC5	'100'	16	F_PRIM/32	0.7375	747

Table 65 RATE_CTRL Register Bit description

Bit Name	Bit Description	Bits	Reset Value
DYN_RATE_XYZ1	Dynamic Range for RATE_X1/Y1/Z1 outputs.	[14:12]	3b001
DYN_RATE_XYZ2	Dynamic Range for RATE_X2/Y2/Z2 outputs.	[11:9]	3b001
DEC_RATE_Z2	Decimation ratio for RATE_Z2 output	[8:6]	3b000
DEC_RATE_Y2	Decimation ratio for RATE_Y2 output	[5:3]	3b000
DEC_RATE_X2	Decimation ratio for RATE_X2 output	[2:0]	3b000

Table 66 ACC12_CTRL Register Bit description

Bit Name	Bit Description	Bits	Reset Value
DYN_ACC_XYZ1	Dynamic Range for ACC_X1/Y1/Z1 outputs.	[14:12]	3b001
DYN_ACC_XYZ2	Dynamic Range for ACC_X2/Y2/Z2 outputs.	[11:9]	3b001
DEC_ACC_Z2	Decimation ratio for ACC_Z2 output	[8:6]	3b000
DEC_ACC_Y2	Decimation ratio for ACC_Y2 output	[5:3]	3b000
DEC_ACC_X2	Decimation ratio for ACC_X2 output	[2:0]	3b000

Table 67 ACC3_CTRL Register Bit description

Bit Name	Bit Description	Bits	Reset Value
DYN_ACC_XYZ3	Dynamic Range for ACC_X3/Y3/Z3 outputs.	[2:0]	3b000

7.4.3 Saturation Flag User control

The registers listed in below table are used to control saturation flag

Table 68 Registers for Saturation flag user control

Register Name	Register Description	R/RW	Public addr
CTRL_RATE_FLAG_1	RATE_XYZ Pre PP SAT_OK Filter user conf	RW	15h002B, D0
CTRL_RATE_FLAG_2	RATE_XYZ PP SAT_OK Filter user conf	RW	15h002C, D0
CTRL_ACC_FLAG_1	ACC_XYZ Pre PP SAT_OK Filter user conf	RW	15h002D, D0
CTRL_ACC_FLAG_2	ACC_XYZ PP SAT_OK Filter user conf	RW	15h002E, D0

Table 69 CTRL_RATE_FLAG_1 register Bit description

Bit Name	Bit Description	Bits	Reset Value
RATE_Z_SAT_CTRL1	User configuration for RATE_Z saturation flags before post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[14:10]	5d00000
RATE_Y_SAT_CTRL1	User configuration for RATE_Y saturation flags before post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[9:5]	5d00000
RATE_X_SAT_CTRL1	User configuration for RATE_X saturation flags before post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[4:0]	5d00000

Table 70 CTRL_RATE_FLAG_2 register Bit description

Bit Name	Bit Description	Bits	Reset Value
RATE_Z_SAT_CTRL2	User configuration for RATE_Z saturation flags in post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[14:10]	5d00000
RATE_Y_SAT_CTRL2	User configuration for RATE_Y saturation flags in post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[9:5]	5d00000
RATE_X_SAT_CTRL2	User configuration for RATE_X saturation flags in post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[4:0]	5d00000

Table 71 CTRL_ACC_FLAG_1 register Bit description

Bit Name	Bit Description	Bits	Reset Value
ACC_Z_SAT_CTRL1	User configuration for ACC_Z saturation flags before post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[14:10]	5d00000
ACC_Y_SAT_CTRL1	User configuration for ACC_Y saturation flags before post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[9:5]	5d00000
ACC_X_SAT_CTRL1	User configuration for ACC_X saturation flags before post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[4:0]	5d00000

Table 72 CTRL_ACC_FLAG_2 register Bit description

Bit Name	Bit Description	Bits	Reset Value
ACC_Z_SAT_CTRL2	User configuration for ACC_Z saturation flags in post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[14:10]	5d00000
ACC_Y_SAT_CTRL2	User configuration for ACC_Y saturation flags in post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[9:5]	5d00000
ACC_X_SAT_CTRL2	User configuration for ACC_X saturation flags in post processing block. Please refer to chapter X(TBD) in SCH1600 Failsafe Specification for detailed description.	[4:0]	5d00000

7.4.4 User interface control

Table 73 Register for user interface control

Register Name	Register Description	R/RW	Public addr
CTRL_USER_IF	User controls for SYNC, Data Ready, Strength of SPI PD/PU, slew rate ctrl, hi-speed	RW	15h0033, D0

Table 74 CTRL_USER_IF register Bit description

Bit Name	Bit Description	Bits	Reset Value
SPI_SUPPLY	SPI_MISO and DRY buffer supply range: x0 - 3.3V+/-10% or 2.5V+/-10% (default) 01 - 1.8V+/-8%	[15:14]	2b00
FTREE_TDEL	Typical delay time of 1st level status clearance. When user reads data register, the associated 1st level status register is cleared after TDEL. 00 - 0.078 ms 01 - 0.625 ms 10 - 2.5 ms (default) 11 – 5 ms	[13:12]	2b10
SYNC_POL	SYNC polarity control. 0 - high active (rising edge) (default) 1 - low active (falling edge).	[11:11]	1b0
SYNC_TOC_TH	SYNC time-out counter control. Counter starts to increase value after rising edge of SYNC_DRY. When counter reaches threshold value selected by SYNC_TOC_TH, data collection is restarted. Counter is reset by falling edge of SYNC_DRY. 00 - 2^15 x MCLK (1.275...1.448ms) 01 - 2^16 x MCLK (2.550...2.896ms) 10 - 2^17 x MCLK (5.100...5.792ms) 11 - 2^18 x MCLK (10.199...11.584ms)	[10:9]	2b00
SYNC_DEC_EN	Enables data freezing for Decimated output registers and their corresponding data counter registers. Can be set both simultaneously and separately with SYNC_INTP_EN. If user enables SYNC and Data ready simultaneously, Data ready takes priority. 0 - Disable 1 - Enable	[8:8]	1b0
SYNC_INTP_EN	Enables data freezing for interpolated output registers and their corresponding data counter registers. Can be set both simultaneously and separately with SYNC_DEC_EN. If user enables SYNC and Data ready simultaneously, Data ready takes priority. 0 - Disable 1 - Enable	[7:7]	1b0

DRY_POL	Data Ready polarity control. 0 - high active (default) 1 - low active	[6:6]	1b0
DRY_DRV_EN	Enables Data ready function. Writing this bit to 1 disables SYNC function, as they cannot be used simultaneously due to common I/O pin. 1 - DRY buffer enabled 0 - DRY buffer disabled.	[5:5]	1b0
SPI_PULL_WEAK	Control of SPI pull-down resistor strength 0- strong pull-down (default) 1 - weak pull-down.	[4:4]	1b0
MISO_SR_CTRL	MISO Slew Rate control 0 - SR control disabled without static current (fast rise/fall time ~<1ns). (contact sales office before enabling) 1 - SR control enabled with static current (default)	[3:3]	1b1
DRY_SR_CTRL	DRY Slew Rate control 0 - SR control disabled without static current (fast rise/fall time ~<1ns). (contact sales office before enabling) 1 - SR control enabled with static current (default)	[2:2]	1b1
DRY_HI_SPD	DRY High-Speed mode control 0 - 10MHz mode, SafeSPI2 standard 1 - 25MHz mode, non-standard high-speed SPI (contact sales office before enabling)	[1:1]	1b0
MISO_HI_SPD	MISO High Speed mode control 0 - 10MHz mode, SafeSPI2 standard 1 - 25MHz mode, non-standard high-speed SPI. (contact sales office before enabling)	[0:0]	1b0

7.4.5 Self-test controls

Table 75 Register for Self-test controls

Register Name	Register Description	R/RW	Public addr
CTRL_ST	Self-test controls (enable ST and/or request STS)	RW	15h0034, D0

Table 76 CTRL_ST register Bit description

Bit Name	Bit Description	Bits	Reset Value
LBIST_REQ_CTRL	Request Logic build-in self-test by writing bit to '1'. The user must write bit back to '0' after test is completed. Recommended wait time before writing '0' is 20ms. Test is done automatically during start-up.	[12:12]	1b0
RATE_Z_STC_CTRL	Disable RATE_Z continuous self-test by writing bit to '0'	[11:11]	1b1
RATE_Y_STC_CTRL	Disable RATE_Y continuous self-test by writing bit to '0'	[10:10]	1b1
RATE_X_STC_CTRL	Disable RATE_X continuous self-test by writing bit to '0'	[9:9]	1b1
ACC_Z_STC_MASK1	Mask ACC_Z continuous self-test flag (STC_N) by writing bit to '0'. The user may opt to mask ACC_Z_STC_N_OK flag if it is not needed in application and a locked flag value is preferred.	[8:8]	1b1
ACC_Y_STC_MASK1	Mask ACC_Y continuous self-test flag (STC_N) by writing bit to '0'. The user may opt to mask ACC_Y_STC_N_OK flag if it is not needed in application and a locked flag value is preferred.	[7:7]	1b1
ACC_X_STC_MASK1	Mask ACC_X continuous self-test flag (STC_N) by writing bit to '0'. The user may opt to mask ACC_X_STC_N_OK flag if it is not needed in application and a locked flag value is preferred.	[6:6]	1b1
ACC_Z_STC_MASK2	Mask ACC_Z continuous self-test flag (STC_SDD) by writing bit to '0'. The user may opt to mask ACC_Z_STC_SDD_OK flag if it is not needed in application and a locked flag value is preferred.	[5:5]	1b1
ACC_Y_STC_MASK2	Mask ACC_Y continuous self-test flag (STC_SDD) by writing bit to '0'. The user may opt to mask ACC_Y_STC_SDD_OK flag if it is not needed in application and a locked flag value is preferred.	[4:4]	1b1
ACC_X_STC_MASK2	Mask ACC_X continuous self-test flag (STC_SDD) by writing bit to '0'. The user may opt to mask ACC_X_STC_SDD_OK flag if it is not needed in application and a locked flag value is preferred.	[3:3]	1b1
ACC_STS_CTRL	Disable ACC start-up self-test by writing bit to '0'	[2:2]	1b1
TEMP_STS_CTRL	Disable Temperature sensor Self-test by writing bit to '0'	[1:1]	1b1
ACC_STS_REQ	Request ACC start-up self-test by writing bit to '1'. The user must write bit back to '0' after test is completed. Recommended wait time before writing '0' is 155ms. Test is done automatically during start-up.	[0:0]	1b0

7.4.6 Sensor mode control and soft reset

Table 77 Registers for setting EN_SENSOR, EOI and Soft Reset

Register Name	Register Description	R/RW	Public addr
CTRL_MODE	EOI, EN_SENSOR	RW	15h0035, D0
CTRL_RESET	SPI soft reset command	RW	15h0036, D0

Table 78 CTRL_MODE register Bit description

Bit Name	Bit Description	Bits	Reset Value
Reserved	Reserved	[3:2]	2b00
EOI_CTRL	End of Initialization, lock all R/W registers, except soft reset control and SYS_TEST. This bit can only be set when there are no errors in common status.	[1:1]	1b0
EN_SENSOR	Enable RATE and ACC measurement	[0:0]	1b0

Table 79 CTRL_RESET register Bit description

Bit Name	Bit Description	Bits	Reset Value
SOFTRESET_CTRL	Writing b'1010 to this bit vector generates a SPI soft reset. SPI Communication is not allowed during 2ms after SPI SOFTRESET.	[3:0]	4b0000

7.4.7 Whomi, Traceability, Identification and Spare Registers

Table 80 Miscellaneous registers

Register Name	Register Description	R/RW	Public addr
SYS_TEST	Empty register for testing read/write	RW	15h0037, D0
SPARE_1	Empty spare register	R	15h0038, D0
SPARE_2	Empty spare register	R	15h0039, D0
SPARE_3	Empty spare register	R	15h003A, D0
ASIC_ID	ASIC revision	R	15h003B, D0
COMP_ID	Component type	R	15h003C, D0
SN_ID1	Component Serial Number 1	R	15h003D, D0
SN_ID2	Component Serial Number 2	R	15h003E, D0
SN_ID3	Component Serial Number 3	R	15h003F, D0

Table 81 SYS_TEST Register Bit description

Bit Name	Bit Description	Bits	Reset Value
SYS_TEST	16bit read/write register which can be used to check the accessibility of the device or if multiple devices are connected to the SPI bus, to check if the CS signals are working properly. Due to Off-frame protocol, test sequence should be as follows: 1. Write data into SYS_TEST register 2. Read SYS_TEST register content 3. Issue a dummy read command to receive response from previous frame SYS_TEST register is not locked by EOI bit.	[15:0]	16b0

Table 82 ASIC_ID register Bit description

Bit Name	Bit Description	Bits
ASIC_TYPE	ASIC type, always 0000 for SCH1-series products	[11:8]
ASIC_REV	ASIC major revision	[7:4]
ASIC_REV_MINOR	ASIC minor revision	[3:0]

Table 83 COMP_ID register Bit description

Bit Name	Bit Description	Bits
COMP_ID	Component version. e.g. SCH1633-D01	[15:0]

The SMD component shall be traceable by a unique electronically readable serial number.
Serial number string format: **DDDYYFHHHHH0X**

Serial number is stored in NVM registers SN_ID1, SN_ID2 and SN_ID3.

H0 is a fixed value and not therefore stored to NVM.

SN_ID1 [3:0] content corresponds to “F” part of serial number (4bit hex to string, 0...F)

Example register content: 0000, therefore 0

SN_ID1 [6:4] content corresponds to “X” part of serial number (3bit hex to string, 0…7) determining product series. For SCH1600 Series the value is fixed to 0

SN_ID2 [15:0] content corresponds to “DDDYY” part of serial number (16 unsigned integer to decimal string, 0....65535)

Example register content: 1000 1010 0101 1111, therefore 35423

,
SN_ID3 [15:0] content corresponds to “HHHH” part of serial number (16bit hexadecimal running number)

Example: 0001 0100 1001 0111
0001 = 1
0100 = 4
1001 = 9
0111 = 7

therefore1497

Serial number result is 3542301497H00

Table 84 SN_ID1 register Bit description

Bit Name	Bit Description	Bits
SN_ID1	“F” part of component serial number (4bit hex to string, 0...F) Format: DDDYYFHHHHH0X	[3:0]
SN_ID1	“X” part of component serial number (3bit hex to string, 0…7) Format: DDDYYFHHHHH0X. For SCH1600 Series the value is fixed to 0	[6:4]

Table 85 SN_ID2 register Bit description

Bit Name	Bit Description	Bits
SN_ID2	"DDDYY" part of serial number (16 unsigned integer to decimal string, 0....65535). DDD is the production day as ordinal number from the beginning of the year and YY is production year. Format: DDDYYFHHHHHH0X	[15:0]

Table 86 SN_ID3 register Bit description

Bit Name	Bit Description	Bits
SN_ID3	"HHHH" part of component serial number (16bit hexadecimal running number) Format: DDDYYFHHHHHH0X	[15:0]

8 Application Information

8.1 Application Circuitry and External Component Characteristics

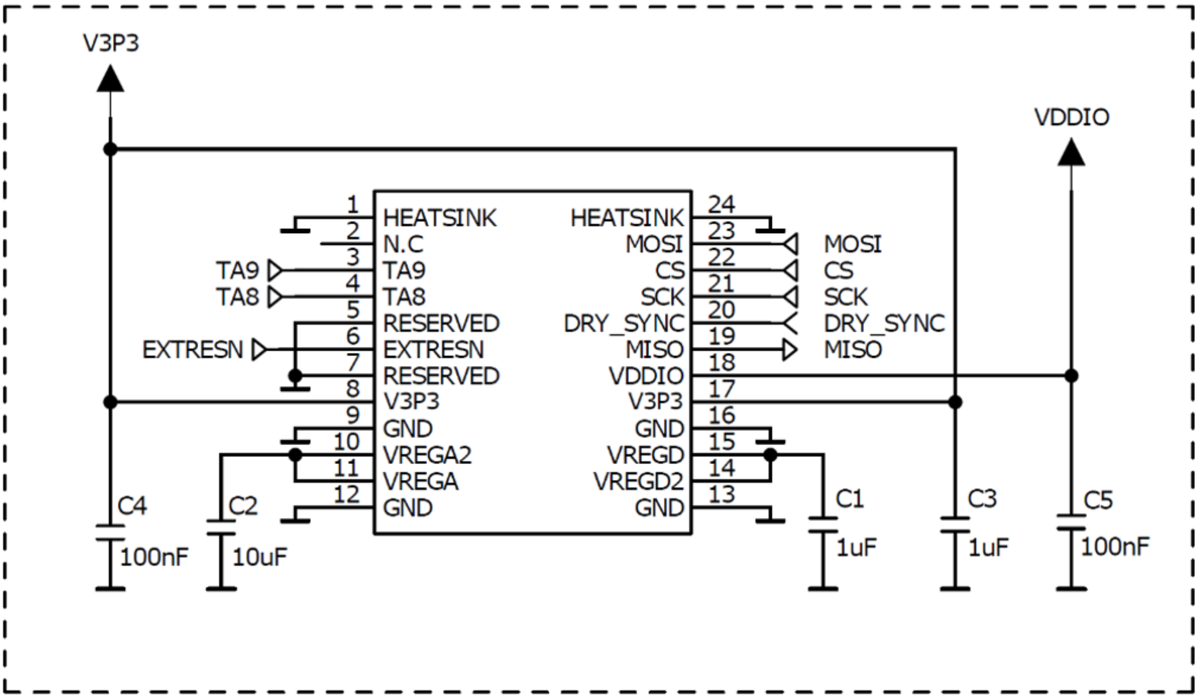

Figure 17 Application schematic

Table 87 External component description for SCH1600

Symbol	Description	Min	Nom.	Max	Unit
C1 C3	Decoupling capacitor between VREGD/VREGD2 (C1)/3p3 pin17 (C3) and GND (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF
C2	Decoupling capacitor between VREGA/VREGA2 and GND (ESR <100mOhm @ 1 MHz)	4.6	10	15	uF
C4 C5	Decoupling capacitor between V3p3 pin8 (C4)/VDDIO (C5) and GND (ESR <100mOhm @ 1 MHz)	70	100	130	nF

- All GND and I/O need to be connected with below exceptions.
- TA8 and TA9 shall be connected to ground, unless application needs to communicate with multiple slaves via single Chip Select.
- If EXTRESN pin is not driven by MCU, it shall be connected to VDDIO directly or with max 20kohm PU resistor.
- DRY_SYNC shall be left floating if these features are not used.
- N.C. pin 2 shall be left floating as indicated by schematic

8.2 General Application PCB layout

A PCB layout example of the SCH1600 Series component is presented in figure 16. The presented layout can be used as such or used only as reference. When designing the PCB, it is advised to follow the general layout guidelines below.

- Connect SMD decoupling capacitors right next to the component on top layer
- A ground plate under the component is not recommended
- Signal lines of this component (SCH1600 series) can be freely routed under the component. It is expected that signal lines of other components have also no effect on the SCH1600 component, but the user is advised to verify functionality before implementation.
- Keep all routing as low resistance as possible

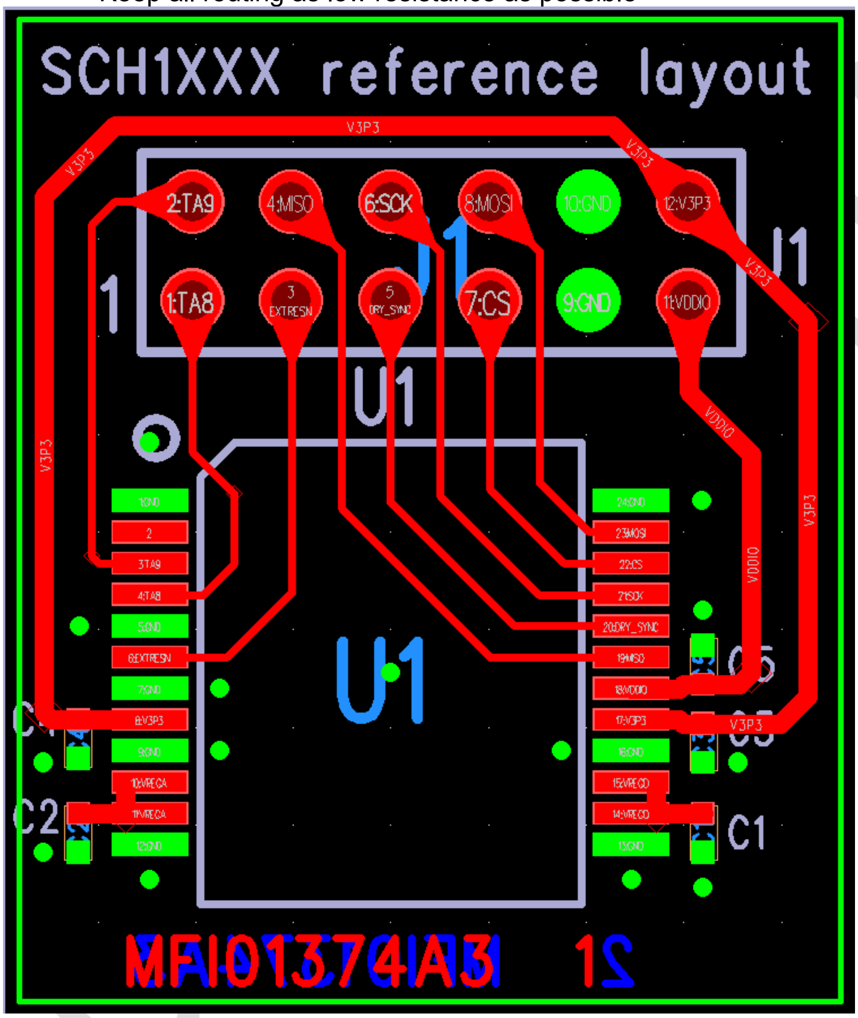

Figure 18 SCH1600 Series reference layout

For additional reference layout solutions, please refer to the document “APP 10871 Rev.1 Assembly instructions for SCH1600 Series"

9 Assembly Instructions

The design of the use application PCB, design of fixtures, conformal coating, vibration and mechanical shocks, material selections, use application environment, and component assembly process can have an impact on the sensor performance. Please refer to the document “APP 10871 Rev.1 Assembly instructions for SCH1600 Series" for related details.

10 Errata

Table 88 List of currently known issues

Category	Description	Effect	Workaround
Feature	DCNT not operational with 32bit SPI mode	DCNT feature cannot be used reliably in 32bit SPI mode	Issue is solved with qualified B-samples
FuSa	Bug in Saturation Flag User Control (chapter 7.4.3)	It is not allowed to change Saturation flag user control settings	Issue solved with qualified B-Samples

11 Document change control

Rev.	Date	Change Description	Author
Rev1	31.10.2022	- First release	NMAL
Rev2	25.04.2023	- Cover sheet: Measurement range update - Table 2 Decimated output update rate re-defined - Table 4 added Repeatability and 20dps linearity specification - Table 4 Noise specification values updated - Table 4 Angle random walk unit and measurement range corrected - Table 5 added Repeatability and Noise Density footnote and corrected foot note A, D and L - Table 6: corrected “conditions”, added parameters - Table 7 corrected foot note A, added foot notes J, K and L - Chapter 3.8 Added Temperature conversion equation - Table 9 added settling times - Updated chapter 5.2 and figure 8 - Added note to Figure 4 caption - Added chapter 5.3 Component output channels. - Added table 15 to chapter 5.3. - Chapter 5.4.1 re-written, Added chapters 5.4.2., 5.4.6., 5.4.7 - Added Multi-Slave operation chapter 6.3 - Chapter 6.4 added status flag logic figure 16 - Table 25 ACC_X Hex corrected - Table 29 added notation of 1st level status registers - Added reset /normal operation value to all RW registers - Corrected SYS_TEST register width to register map table - Chapter 7.2.3: Corrected missing zeroes in 20bit Hex frames - Table 47-49 specified saturation channels to X3/Y3/Z3 - Table 56: Added default filter notation - Table 61-63 measurement ranges updated - Table 69-72 bit description updated - Table 74: Improved bit description - Rearranged content of chapters 7.4.6-7.4.8 - Chapter 7.4.7 added serial number coding - Table 87 updated C2 capacitor specification - Added chapter 8.2	NMAL
Rev3		- Table 4 updated ARS total sensitivity error, linearity error - Table 6 updated ACC total sensitivity error, Temperature drift velocity, total error, added orthogonality and cross-axis sensitivity specification - Table 7 added foot notes for orthogonality and cross-axis sensitivity - Table 8 temperature offset updated - Table 10 Temperature sensor requirement updated - Table 11 added default state/structure to pins 3,4 and 6 - Table 12 added specification to weak input pull-up/down - Chapter 6.5 CRC calculation updated - Table 26 address example corrected - Table 34 FREQ_CNTR bit description updated - Tables 42,48-50 SD_STS_OK flag description corrected - Table 61 DYN1 sensitivity and dynamic range updated - Table 76 bit descriptions updated	NMAL

		- Chapter 10 updated	

Signatures:

Controlled Document Approval:	I approve this document.		
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