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TP74LVC14ATS14

Hex inverting Schmitt tigger with 5 V tolerant input

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Features

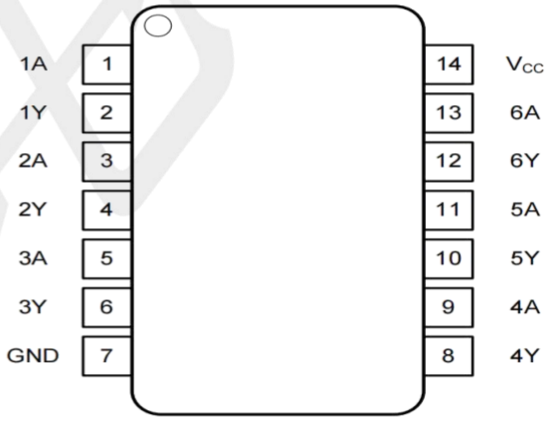
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power dissipation
- Overvoltage tolerant inputs to 5.5 V
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- ESD protection:
  HBM ANSI/ESDA/JEDEC JS-00
  Class 3A exceeds 6000 V
  CDM ANSI/ESDA/JEDEC JS-002
  Class C3 exceeds 2000 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  JESD8-7 (1.65 V to 1.95 V)
  JESD8-5 (2.3 V to 2.7 V)
  JESD8C (2.7 V to 3.6 V)
  JESD36 (4.5 V to 5.5 V)
- Packaging: TSSOP-14

General Description

The is a hex inverter with Schmitt-trigger inputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

PIN CONFIGURATIONS (Top view)



TSSOP-14

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION	PIN NO.	PIN NAME	DESCRIPTION
1	1A	Data input	8	4Y	Data output
2	1Y	Data output	9	4A	Data input
3	2A	Data input	10	5Y	Data output
4	2Y	Data output	11	5A	Data input
5	3A	Data input	12	6Y	Data output
6	3Y	Data output	13	6A	Data input
7	GND	ground (0 V)	14	V_{CC}	supply voltage

Functional diagram

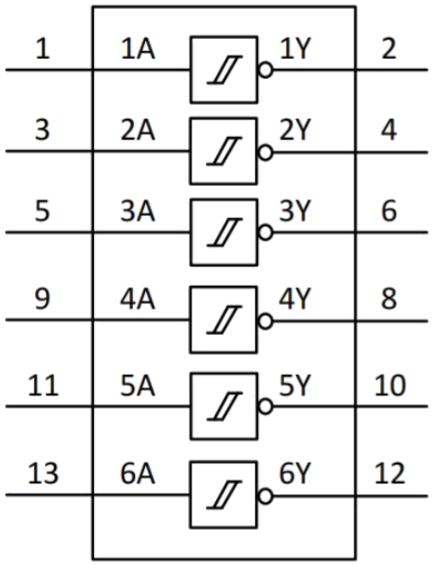


Fig. 1. Logic symbol

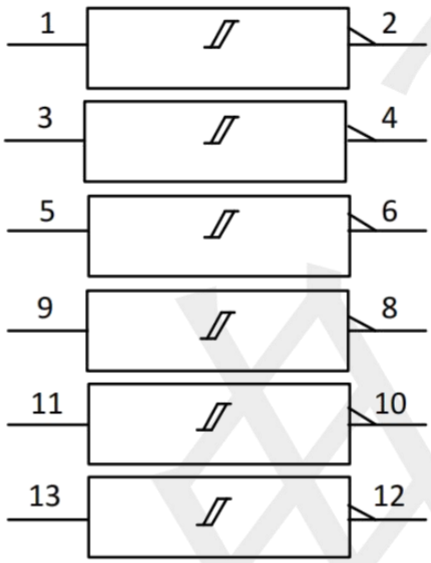


Fig. 2. IEC logic symbol

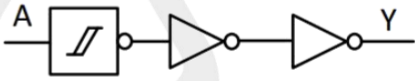


Fig. 3. Logic diagram(one gate)

Functional Description

Function table

Input nA	Output nY
L	H
H	L

H = HIGH voltage level; L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System. Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	--	mA
V_I	input voltage	(1)	-0.5	6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	--	±50	mA
V_O	output voltage	Active mode (1)	0	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V (1)	0	6.5	V
I_O	output current	V_O = 0 V to V_{CC}	--	±50	mA
I_{CC}	supply current		--	100	mA
I_{GND}	ground current		-100	--	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C	--	500	mW
T_{stg}	storage temperature		-65	150	°C

Note:1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
		functional	1.2	--	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		-40	125	°C

Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = -100μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	--	--	V_{CC} - 0.1	--	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	--	--	1.05	--	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	--	--	1.7	--	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	--	--	2.05	--	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.4	--	--	2.25	--	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	--	--	3.5	--	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = 100μA; V_{CC} = 1.65 V to 5.5 V	--	--	0.10	--	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	--	--	0.45	--	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	--	--	0.30	--	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	--	--	0.40	--	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	--	--	0.55	--	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	--	--	0.55	--	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND ; V_{CC} = 0 V to 5.5 V	--	±0.1	±5	--	±20	μA
I_{OFF}	power-off leakage current	V_{CC} = 0V ; V_I or V_O = 5.5 V	--	±0.1	±10	--	±20	μA
I_{CC}	supply current	V_I = 5.5V or GND ; I_O = 0A ; V_{CC} = 1.65V to 5.5V	--	0.03	10	--	40	μA
ΔI_{CC}	additional supply current	per input pin ; V_{CC} = 2.3V to 5.5V ; V_I = V_{CC} -0.6V ; I_O = 0A	--	0.8	500	--	5000	μA
C_I	input capacitance	V_{CC} = 3.3V ; V_I = GND to V_{CC}	--	4	--	--	--	pF

Note:All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25 °C.

Dynamic Characteristics

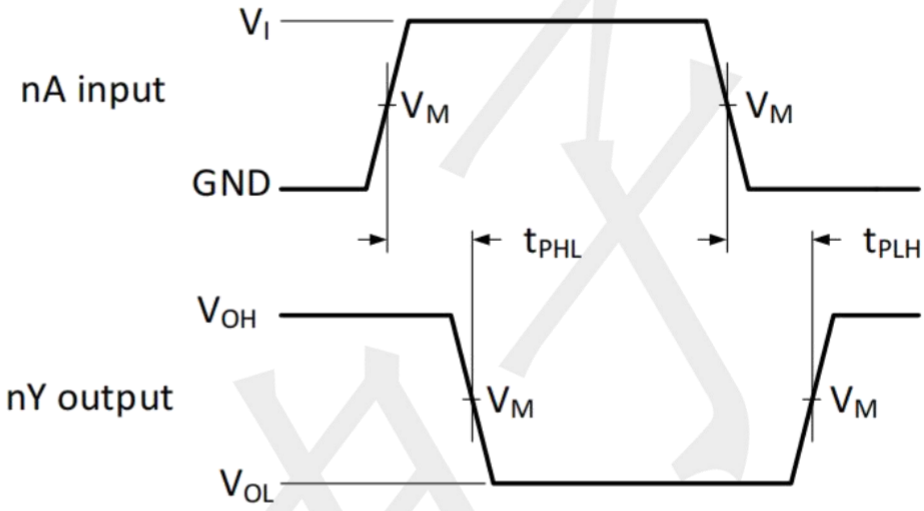
Voltages are referenced to GND (ground = 0 V); for test circuit see

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	nA to nY						
		V_{CC} = 1.2 V	--	46	--	--	--	ns
		V_{CC} = 1.65 V to 1.95 V	4	12.3	24	4	25	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	7.4	12	2.5	13	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	5.7	8.5	1.5	9	ns
		V_{CC} = 4.5 V to 5.5 V	1	3.5	6	1	6.5	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	--	--	1.0	--	1.5	ns
C_{PD}	power dissipation capacitance	per buffer ; V_I = GND to V_{CC}						
		V_{CC} = 1.65 V to 1.95 V	--	12.7	--	--	--	pF
		V_{CC} = 2.3 V to 2.7 V	--	13.3	--	--	--	pF
		V_{CC} = 3.0 V to 3.6 V	--	14.3	--	--	--	pF
		V_{CC} = 4.5 V to 5.5 V	--	16.5	--	--	--	pF

Note:

Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V respectively.
t_{pd} is the same as t_{PLH} and t_{PHL}.
Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF; V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Waveforms and test circuit

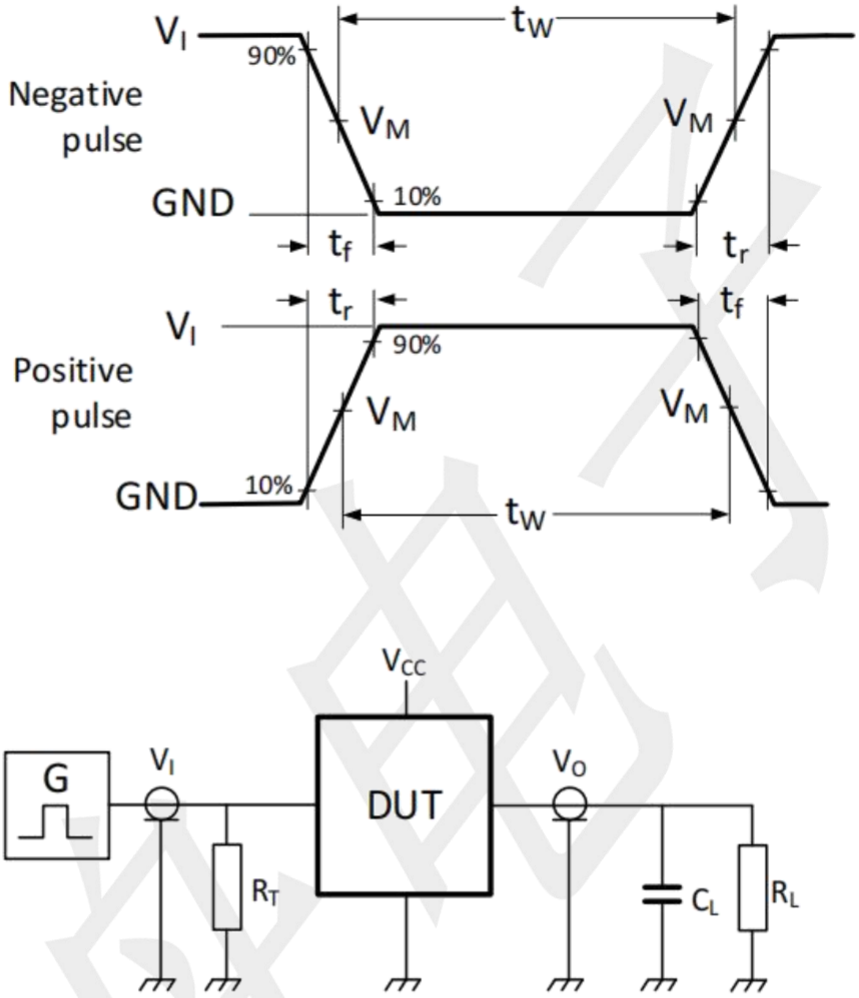


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The input nA to output nY propagation delays

Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	0.5V_{CC}	0.5V_{CC}
1.65 V to 1.95 V	0.5V_{CC}	0.5V_{CC}
2.3 V to 2.7 V	0.5V_{CC}	0.5V_{CC}
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5V_{CC}	0.5V_{CC}

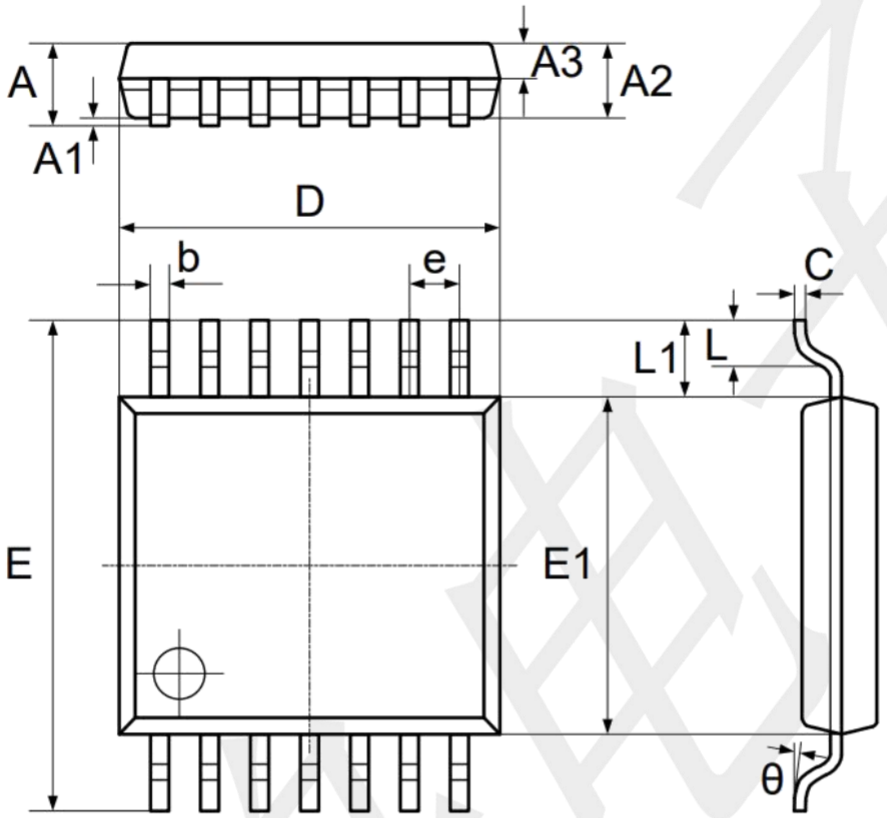


Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Test data

Supply voltage	Input		Load	
V_{CC}	V_I	$t_r = t_f$	C_L	R_L
1.2 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
3.0 V to 3.6 V	3 V	≤ 2.0 ns	15 pF	500 Ω
4.5 V to 5.5 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω

Package informantion TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
A3	0.390	0.490	0.015	0.019
b	0.200	0.290	0.008	0.011
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.191	0.199
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 TYP.		0.026 TYP.	
L1	1.000 REF.		0.039 REF.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°