

General Description:

The LWP3005A4 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge and operation with gate voltage as low as 4.5V. It can be used in a wide variety of applications. The package form is TO-252, which accords with the ROHS standard and Halogen Free standard.

Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Applications:

- Battery switching application
- Hard switched and high frequency circuits
- Power Management

100% DVDS Tested

100% Avalanche Tested



Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
P3005/LW A4/D.C.	LWP3005A4	TO-252	Reel	2500 Pcs

Absolute Maximum Ratings:

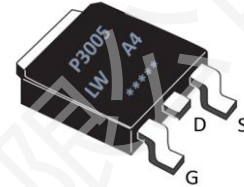
Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-30	V
I_D	Continuous Drain Current	$T_C=25^{\circ}\text{C}$	-120	A
	Continuous Drain Current	$T_C=100^{\circ}\text{C}$	-76	A
I_{DM}^{a1}	Pulsed Drain Current		-480	A
E_{AS}^{a2}	Single pulse avalanche energy		925	mJ
V_{GS}	Gate-to-Source Voltage		± 20	V
P_D	Power Dissipation		110	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	$^{\circ}\text{C}$
T_L	Maximum Temperature for Soldering		260	$^{\circ}\text{C}$

Thermal Characteristics:

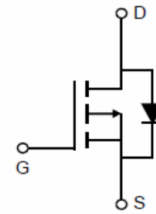
Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.14	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}^{a3}$	Thermal Resistance, Junction-to-Ambient	50	$^{\circ}\text{C}/\text{W}$

V_{DSS}	-30	V
I_D	-120	A
P_D	110	W
$R_{DS(ON) \text{ TYPE}}$	2.8	$\text{m}\Omega$

Marking and Pin Assignment



Inner Equivalent Principium Chart



Electrical Characteristic ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise specified):

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=-30V, V_{GS}=0V$	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=-20V, V_{DS}=0V$	--	--	-100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=+20V, V_{DS}=0V$	--	--	100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.3	-1.7	-2.1	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	$V_{GS}=-10V, I_D=-20A$	--	2.8	3.5	$m\Omega$
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	$V_{GS}=-4.5V, I_D=-10A$	--	4.5	6.0	$m\Omega$

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0V$	--	6239	--	pF
C_{oss}	Output Capacitance	$V_{DS}=-15V$	--	1115	--	
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	--	1027	--	
R_G	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	--	7.5	--	Ω

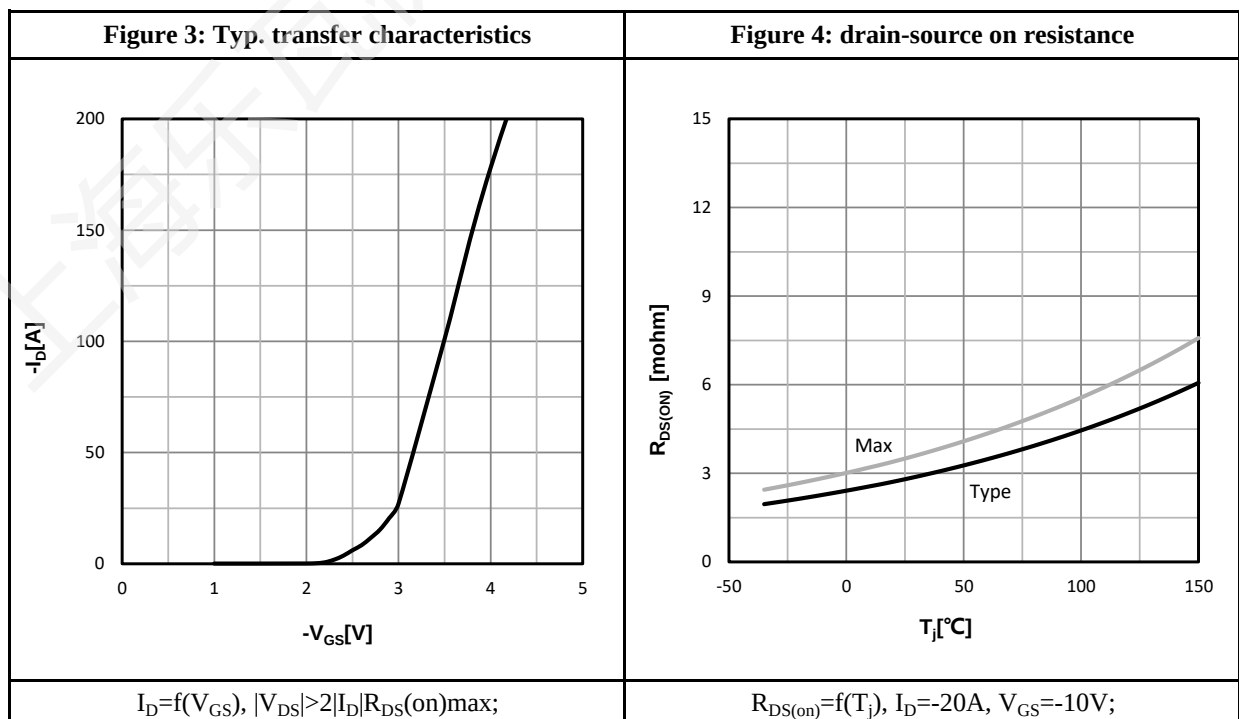
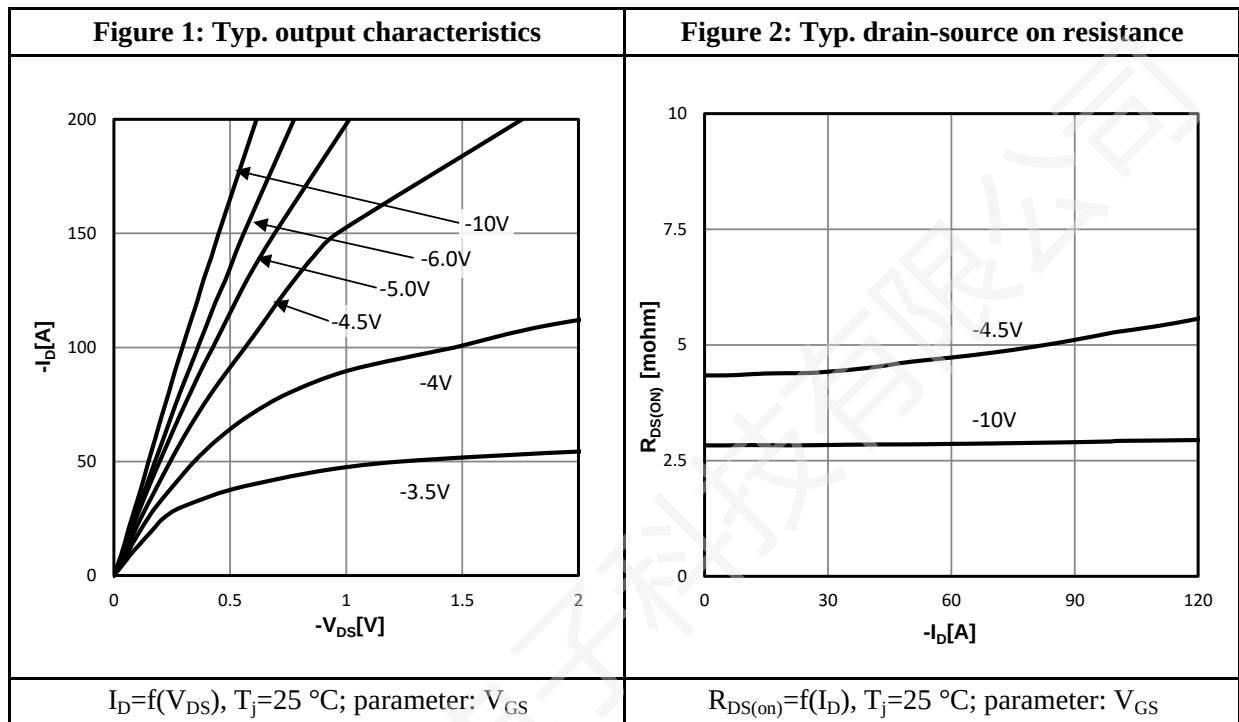
Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=-20A$	--	15	--	ns
t_r	Rise Time	$V_{DS}=-15V$	--	18	--	
$t_{d(OFF)}$	Turn-Off Delay Time	$V_{GS}=-10V$	--	110	--	
t_f	Fall Time	$R_G=3.0\Omega$	--	85	--	
Q_g	Total Gate Charge	$V_{GS}=-10V$	--	118.7	--	nC
Q_{gs}	Gate to Source Charge	$V_{DS}=-15V$	--	15.6	--	
Q_{gd}	Gate to Drain Charge	$I_D=-10A$	--	26	--	

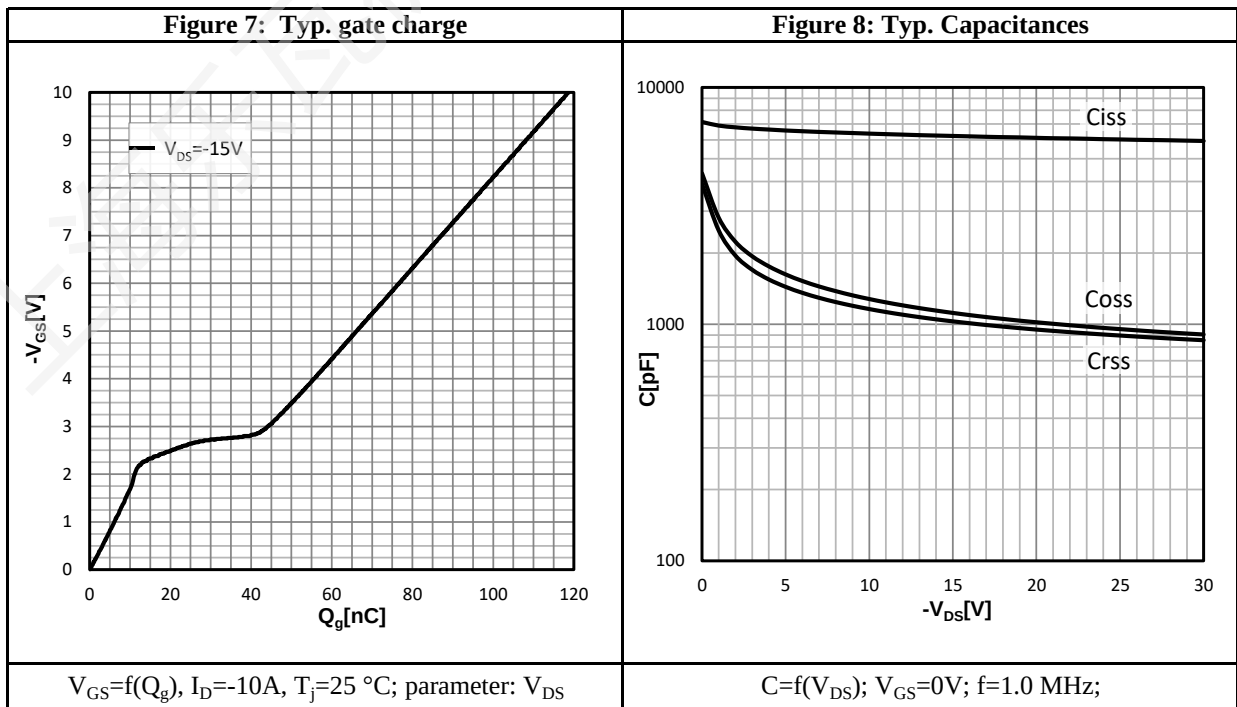
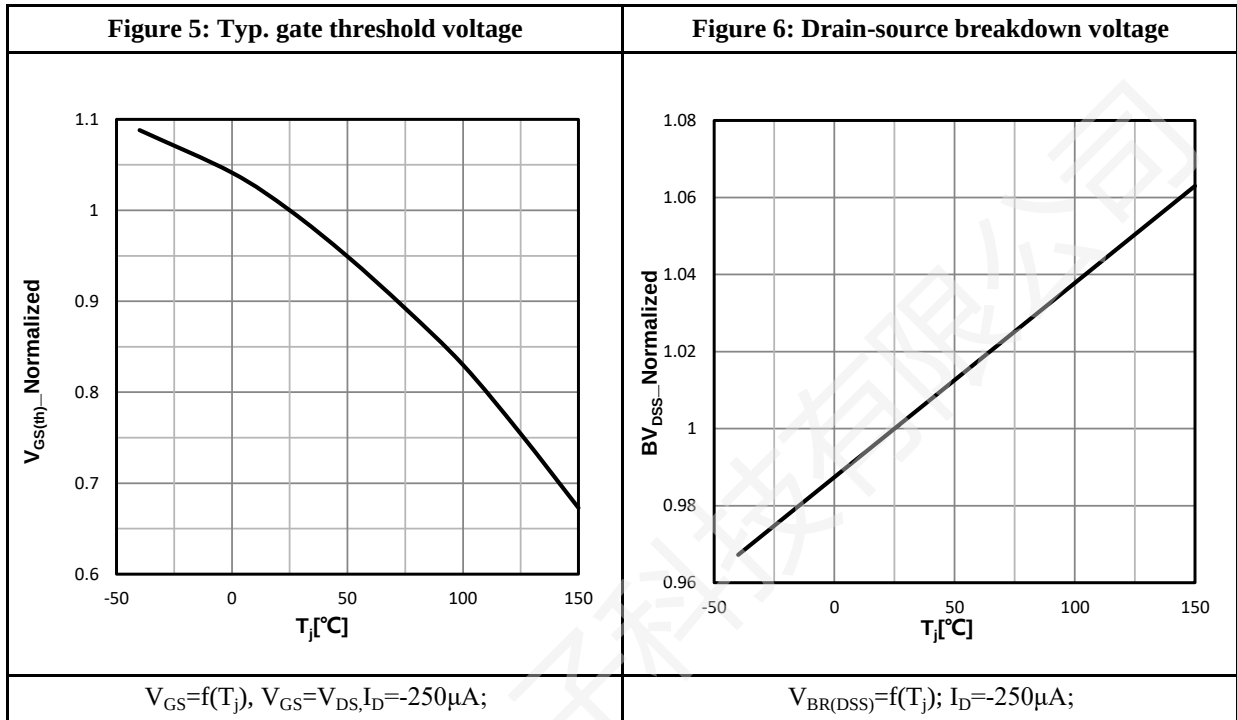
Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	$T_C=25\text{ }^{\circ}\text{C}$	--	--	-120	A
V_{SD}	Diode Forward Voltage	$I_S=-15A, V_{GS}=0V$	--	--	-1.2	V

a1: Repetitive rating; pulse width limited by maximum junction temperature

a2: $V_{DD}=-30V, L=0.5mH, R_G=25\Omega$, Starting $T_J=25\text{ }^{\circ}\text{C}$

a3: Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection.

Characteristics Curve:




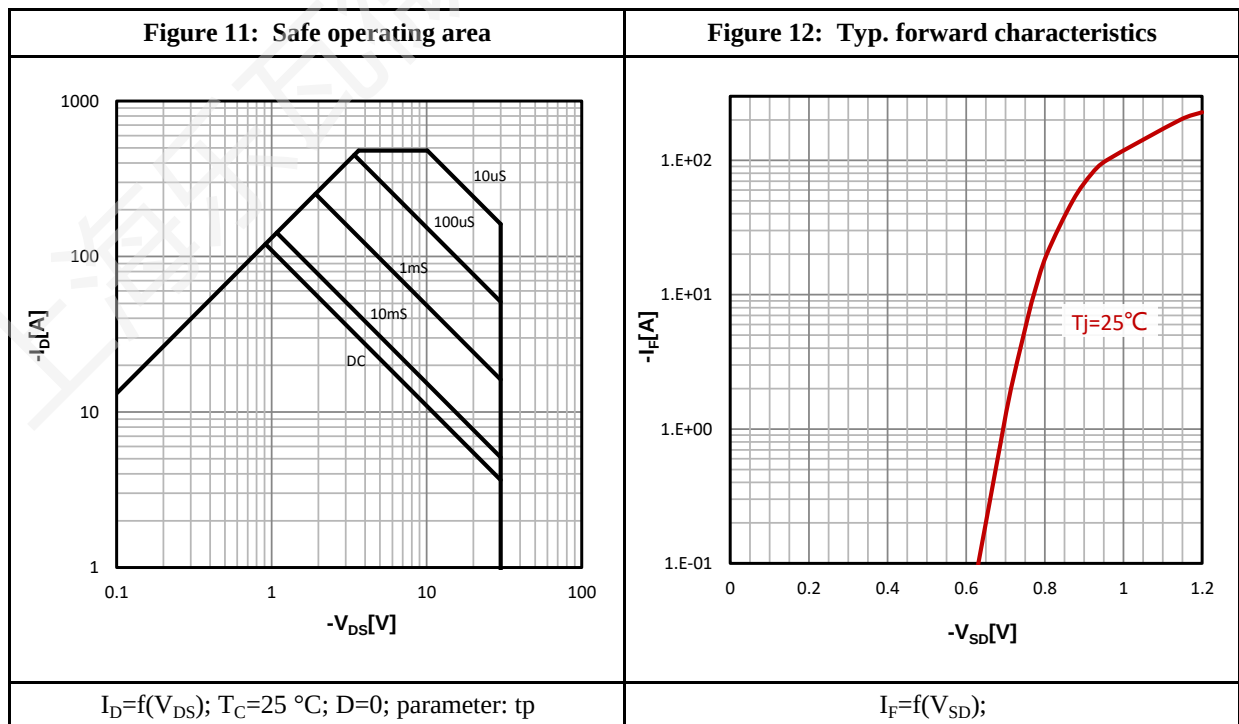
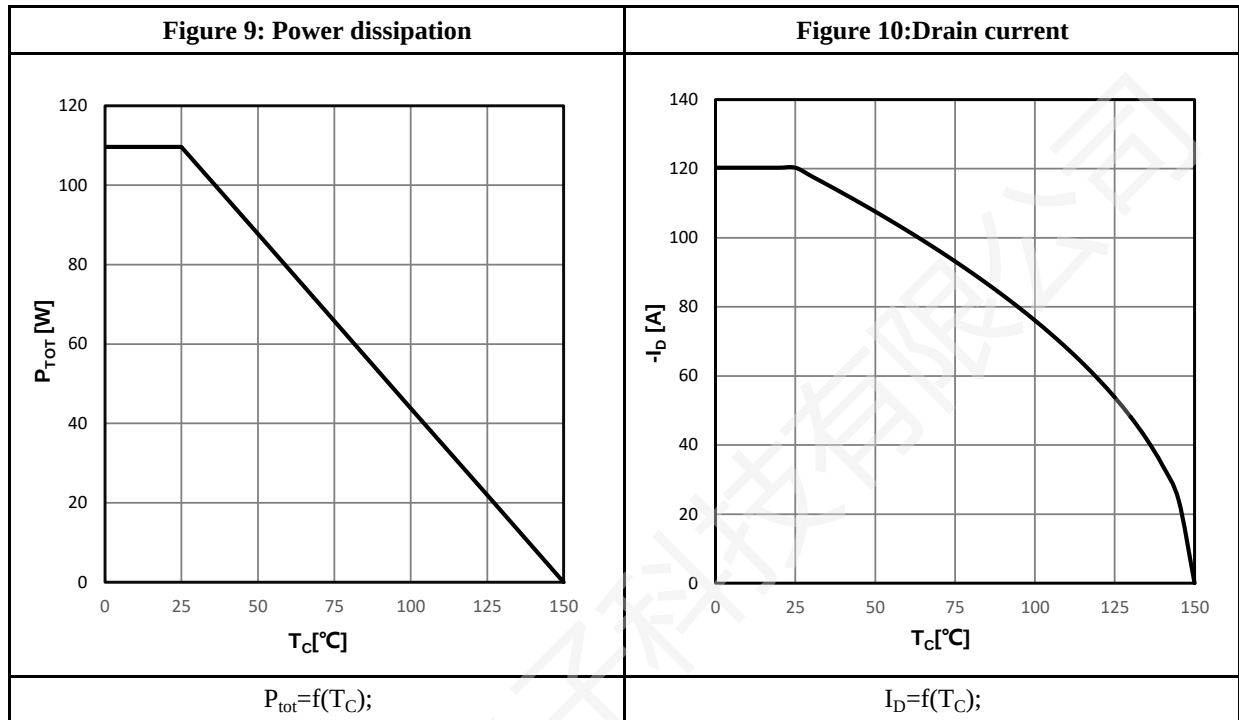
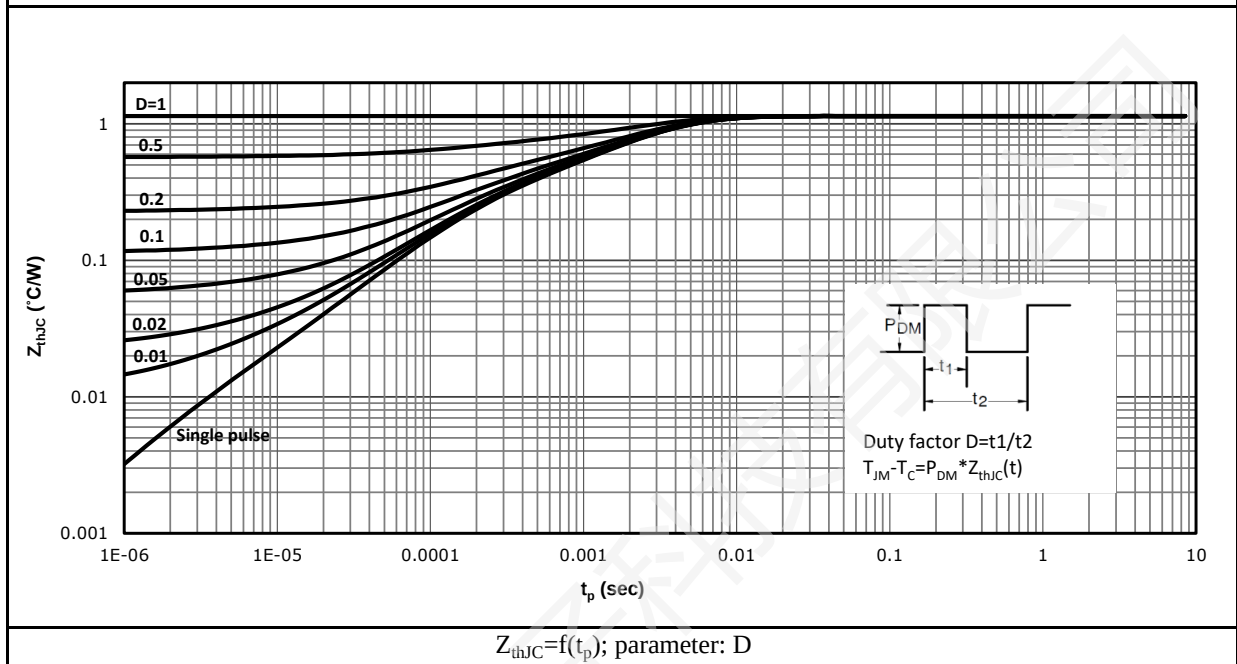
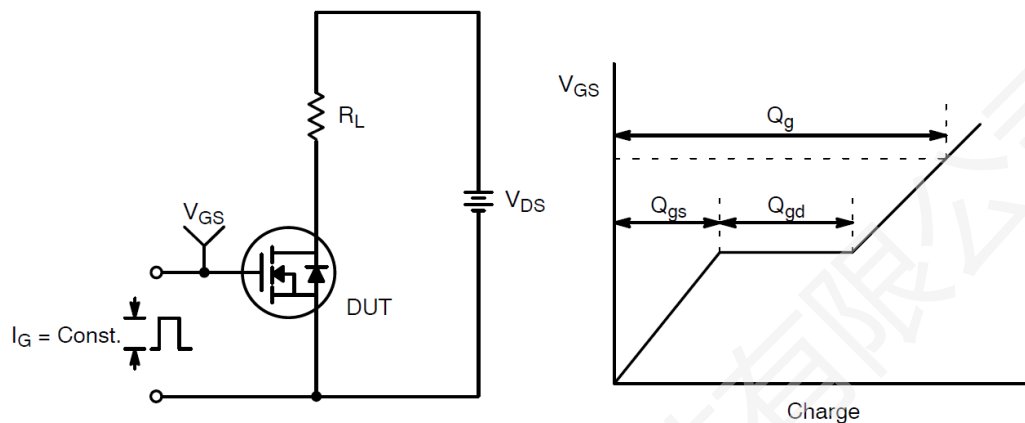
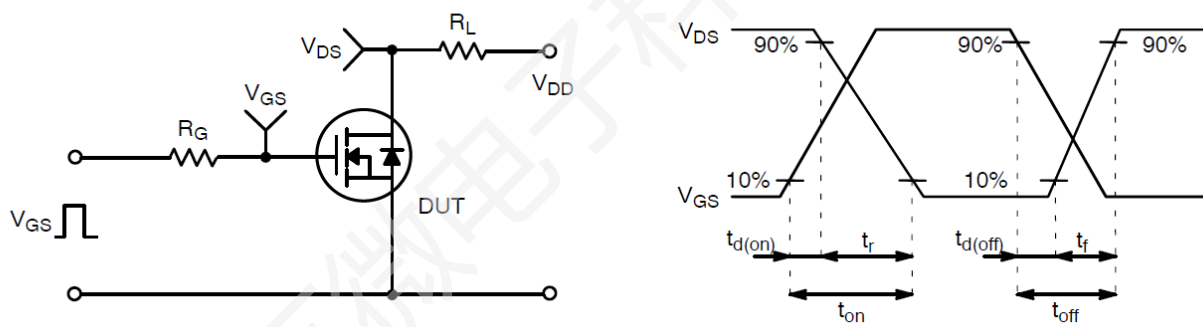
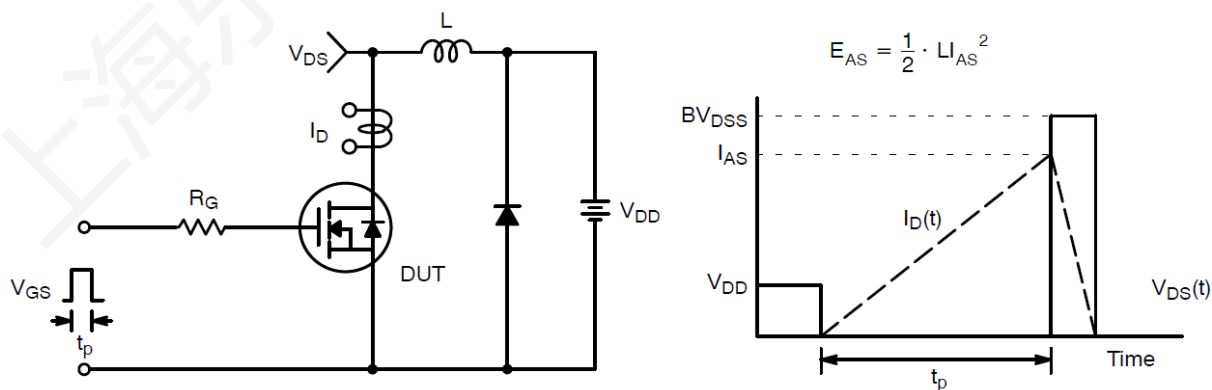
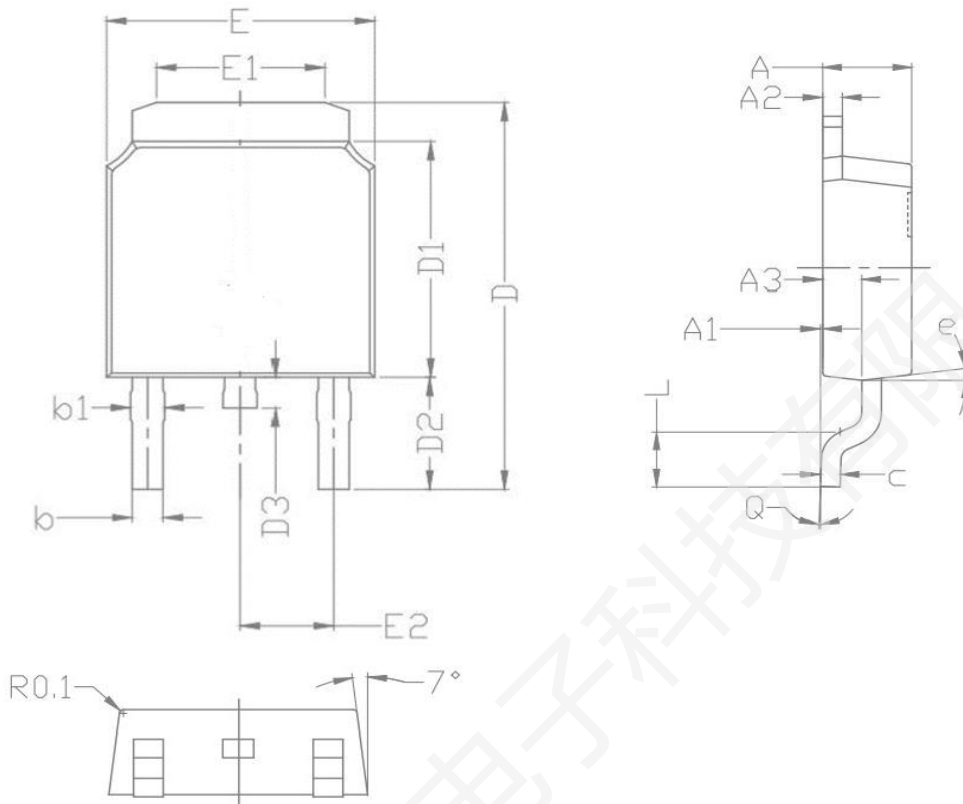


Figure 13: Max. Transient Thermal Impedance


Test Circuit & Waveform:

Figure 14: Gate Charge Test Circuit & Waveform

Figure 15: Resistive Switching Test Circuit & Waveforms

Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:


COMMON			
PKG	TO-252		
Symbol	Min	Nom	Max
A	2.200	2.300	2.400
A1	0.000	0.075	0.150
A2	0.460	0.525	0.590
A3	0.960	1.010	1.060
b	0.640	0.720	0.800
C	0.450	0.515	0.580
D	9.800	10.025	10.350
D1	6.000	6.100	6.200
D2	2.850	2.900	3.100
D3	0.490	0.800	1.000
E	6.400	6.550	6.700
E1	4.050	4.130	4.600
E2	2.250	2.286	2.300
L	1.400	1.550	1.700
e	7°	8°	9°
Q	0°	5°	10°

Revision History:

Revison	Date	Descriptions
Rev 1.1	July.2025	Initial Version

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