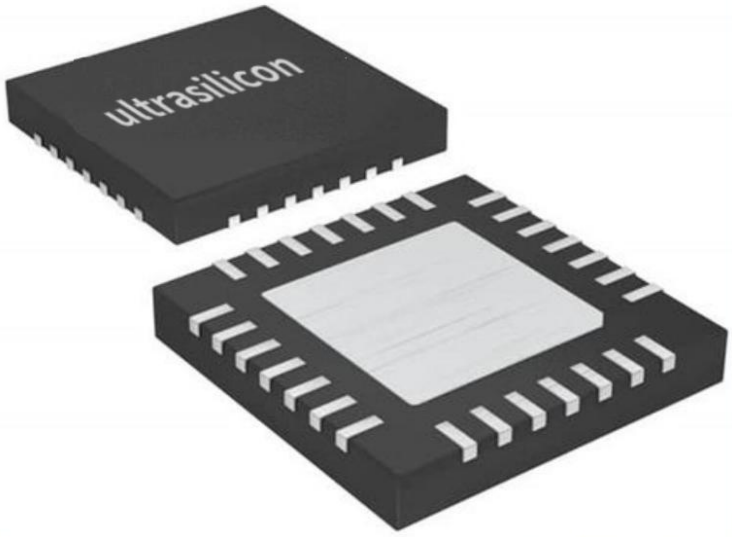
Description

The US5D2104D is a 2-GHz,8-output differential high-performance clock fanout buffer.

The US5D2104D clock buffer distributes two selectable clock inputs to 8 pairs of differential LVDS clock outputs with minimum skew for clock distribution. The US5D2104D can accept one clock sources into an input multiplexer. The inputs can either be LVDS,LVPECL, or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 2.5V/3.3V core power supply, and either a 2.5V/3.3V output operating supply.



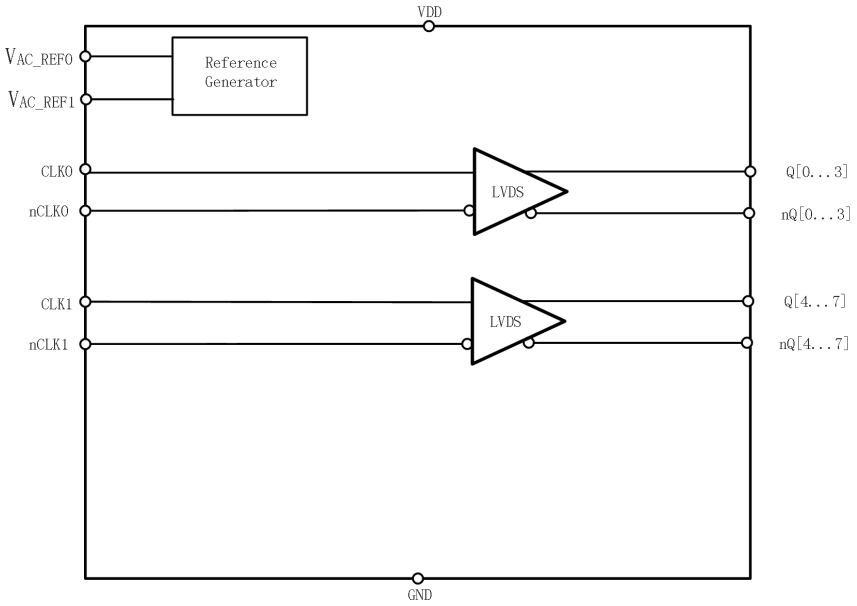
Features

- Dual 1:4 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS and LVCMOS
- 8 LVDS output
- Maximum Output Frequency
  LVDS - 2-GHz
- Maximum Propagation Delay: 0.5ns(typical)
- Output skew: 30 ps (Maximum)
- Additive RMS phase jitter 3.3V@ 156.25MHz:
  88 fs RMS (10kHz - 20MHz)
- Supply voltage mode VDD: 2.5V±5%,3.3V±5%
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-28(5x5) package

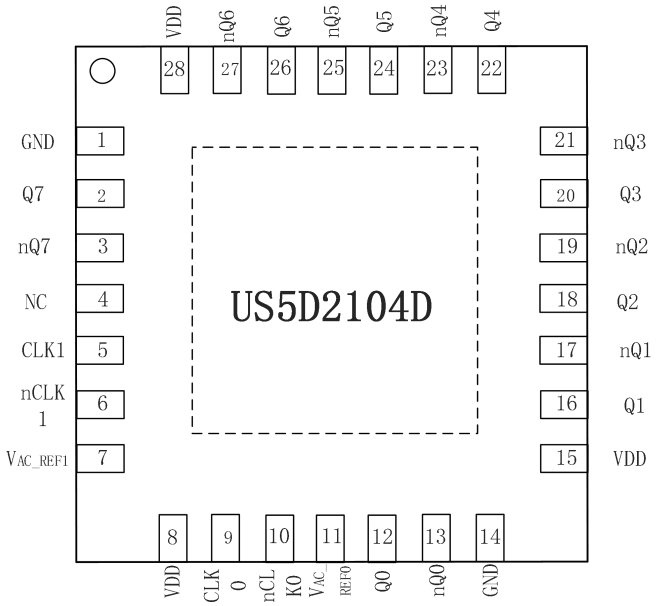
Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Block Diagram



Pin Assignment for QFN-28 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
14	GND	Power	Ground.
4	NC	NC	No connect.
5	CLK1	Input	Differential input pair. Unused input pair can be left floating.
6	nCLK1	Input	Inverting differential input pair . Unused input pair can be left floating.
8	VDD	Power	2.5V/3.3V supply for the device.
15	VDD	Power	2.5V/3.3V supply for the device.
28	VDD	Power	2.5V/3.3V supply for the device.
9	CLK0	Input	Differential input pair. Unused input pair can be left floating.
10	nCLK0	Input	Inverting differential input pair . Unused input pair can be left floating.
11	VAC_REF0	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1-μF to GND on this pin.
7	VAC_REF1	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1-μF to GND on this pin.
12	Q0	Output	Differential LVDS output pair number 0.
13	nQ0	Output	Differential LVDS output pair number 0.
16	Q1	Output	Differential LVDS output pair number 1.
17	nQ1	Output	Differential LVDS output pair number 1.
18	Q2	Output	Differential LVDS output pair number 2.
19	nQ2	Output	Differential LVDS output pair number 2.
20	Q3	Output	Differential LVDS output pair number 3.
21	nQ3	Output	Differential LVDS output pair number 3.
22	Q4	Output	Differential LVDS output pair number 4.
23	nQ4	Output	Differential LVDS output pair number 4.
24	Q5	Output	Differential LVDS output pair number 5.
25	nQ5	Output	Differential LVDS output pair number 5.
26	Q6	Output	Differential LVDS output pair number 6.
27	nQ6	Output	Differential LVDS output pair number 6.
2	Q7	Output	Differential LVDS output pair number 7.
3	nQ7	Output	Differential LVDS output pair number 7.

Table 2. Output Selection Table

CLOCK INPUTS	CLOCK OUTPUTS
INP0,INN0	Q0~ Q3 enabled andQ4~ Q7 disabled
INP1,INN1	Q0~ Q3 disabled andQ4~ Q7 enabled

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	2.5-5% 3.3-5%	2.5 3.3	2.5+5% 3.3+5%	V

Electrical Characteristics

VDD = 2.375 V to 2.625 V and TA = –40°C to 85°C (unless otherwise noted).

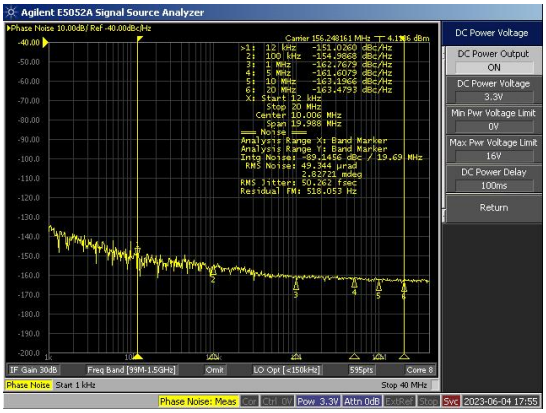
Parameter		Test Conditions	Min	Typ	Max	Unit
IDD	Power supply current	VDD=3.3V,FIN=20MHz	-	136	-	mA
		VDD=2.5V,FIN=20MHz	-	132	-	mA
LVCMOS INPUT						
FIN	Input frequency	VDD=3.3V	0.1		250	MHz
Vth	input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
VIH	Input high voltage		0.7*VDD		VDD	V
VIL	Input low voltage		GND		0.3*VDD	V
IIH	Input high current	VDD = 2.625V, VIH = 2.625 V			10	μA
IIL	Input low current	VDD = 2.625V, VIL = 0 V			-10	μA
C_{IN}	Input capacitance			2.5		pF

Electrical Characteristics(continued)

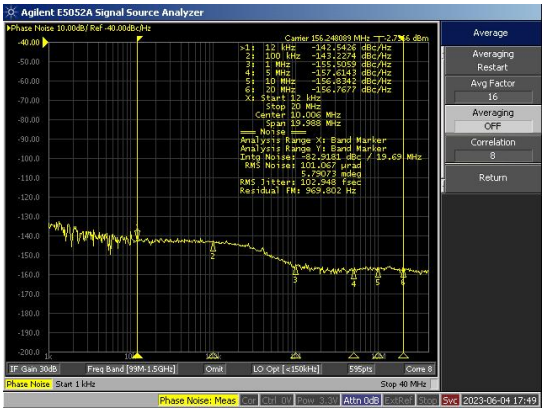
VDD = 2.375 V to 2.625 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT						
FIN	Input frequency	VDD=3.3V	0.1		2000	MHz
V IN,DIFF	Differential input voltage Peak-to-peak	VICM=1.25V	0.3		1.6	VPP
V ICM	Input common mode voltage	VIN, DIFF, PP > 0.4 V	1		VDD-0.3	V
IIH	Input high current	VDD = 2.625V, VIH = 2.625 V			10	μA
IIL	Input low current	VDD = 2.625V, VIL = 0 V			-10	μA
C_{IN}	Input capacitance			2.5		pF
LVDS OUTPUT						
VOD	Differential output voltage magnitude	VIN, DIFF, PP = 0.3 V,RL = 100 Ω	250		450	mV
ΔVOD	Change in differential output voltage magnitude	VIN, DIFF, PP = 0.3 V,RL = 100 Ω	-15		15	mV
VOC(ss)	Steady-state common mode output voltage	VIN, DIFF, PP = 0.3 V,RL = 100 Ω	1.1		1.375	V
ΔVOC(ss)	Steady-state common mode output voltage	VIN, DIFF, PP = 0.3 V,RL = 100 Ω	-15		15	mV
Vring	Output overshoot and undershoot	Percentage of output amplitude VOD			10%	
t_{PD}	Propagation delay	3.3V@100MHz		0.5	1.5	ns
$t_{SK,pp}$	Part-to-part skew				600	ps
$t_{SK,O}$	Output skew			15	30	ps
$t_{SK,P}$	Pulse skew	50% duty cycle input,crossingpoint-to-crossing-point distortion	-50		50	ps
t_{RJIT}	Random additive jitter	50% duty cycle input, 10 kHz to 20 MHz, 156.25MHz		88	300	fs
t_R/t_F	Output rise time	20% to 80%		200	300	ps
	Output fall time	20% to 80%		200	300	ps
ΔV/ΔT	Slew rate	20% to 80%@100MHz			3.0	V/ns
V_{AC_REF}	Reference output voltage	VDD = 2.5 V, I_{load} = 100 μA	1.1	1.25	1.35	V

Phase Noise Plot



Low jitter SPXO(156.25MHz)(50fs)



Output Phase Noise(102fs)

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

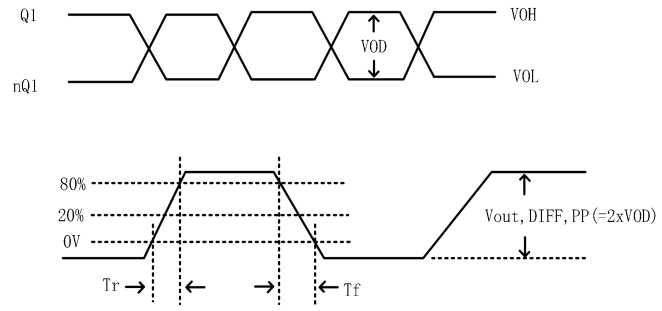
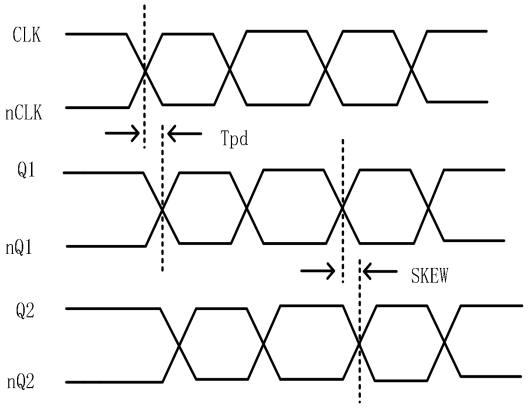


Figure 1.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 2.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

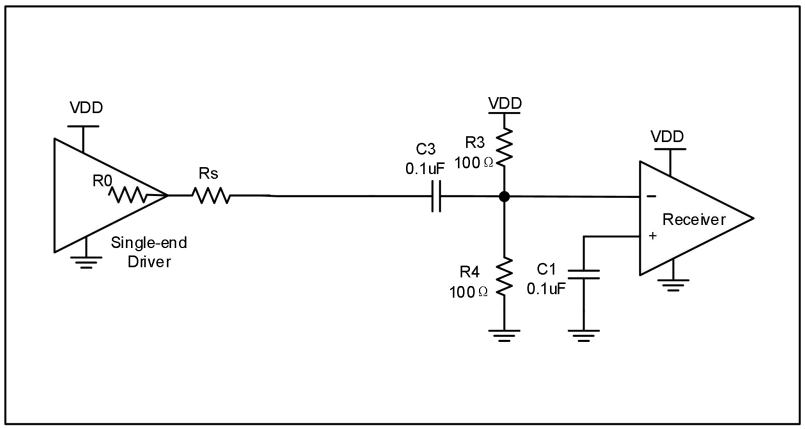
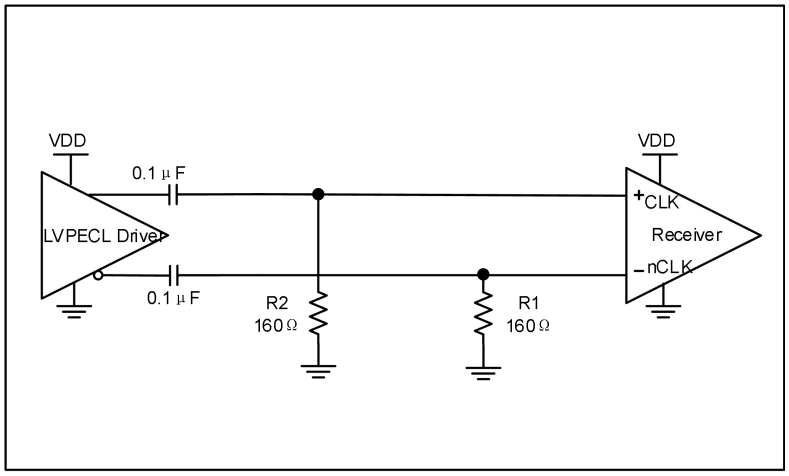
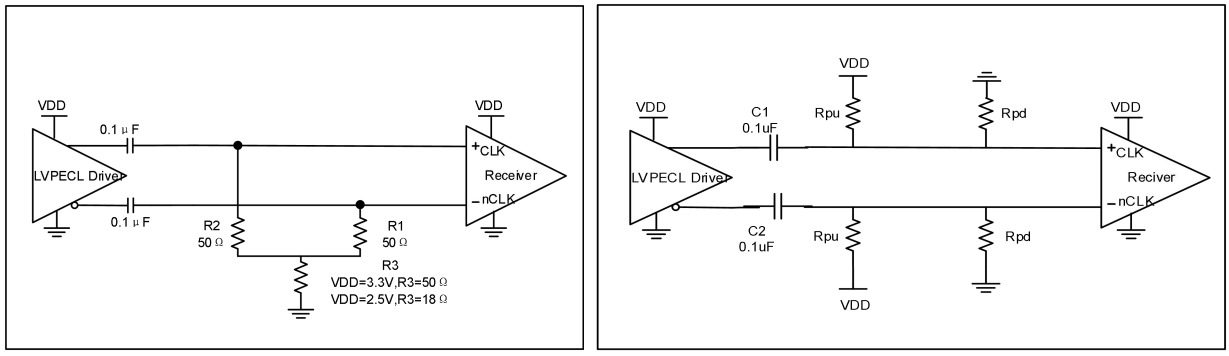


Figure3.Single-ended input

Input connection circuit

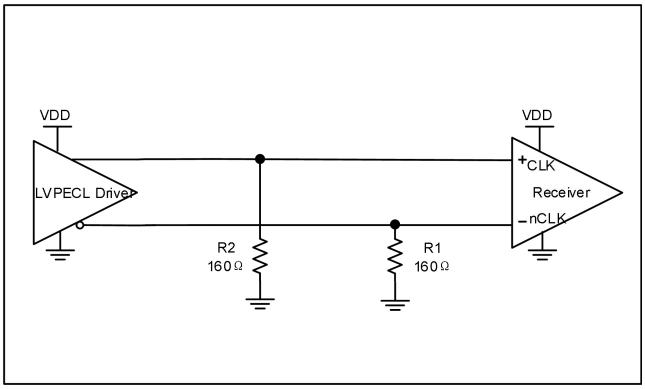
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure4 to Figure7 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

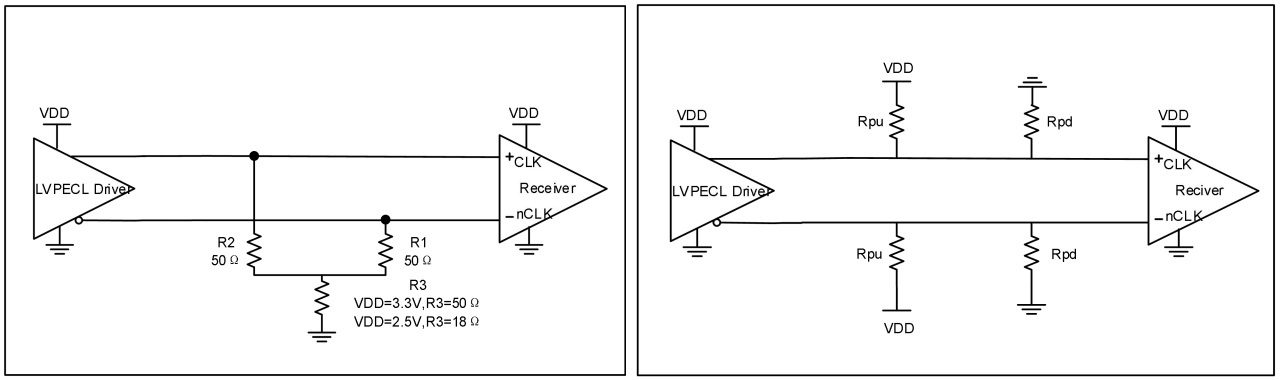




VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

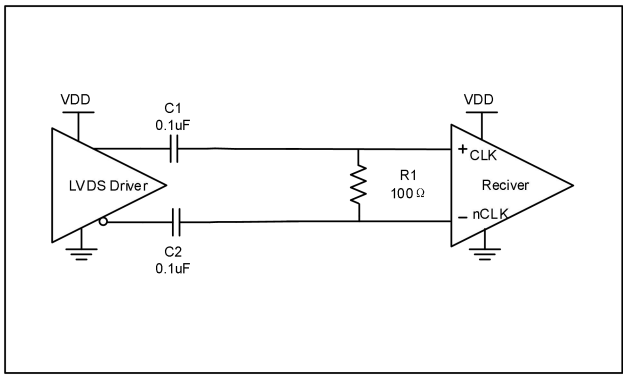
Figure4.LVPECL Driver(AC)



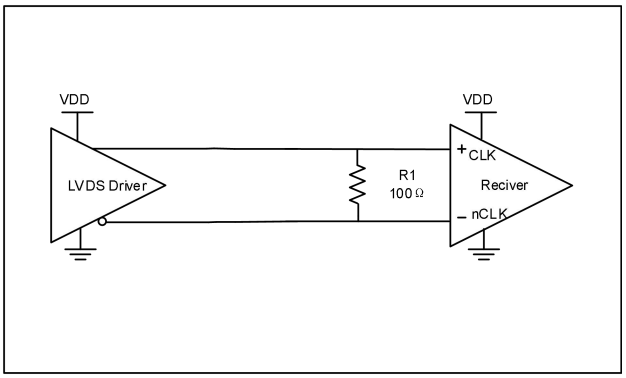


VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure5.LVPECL Driver(DC)

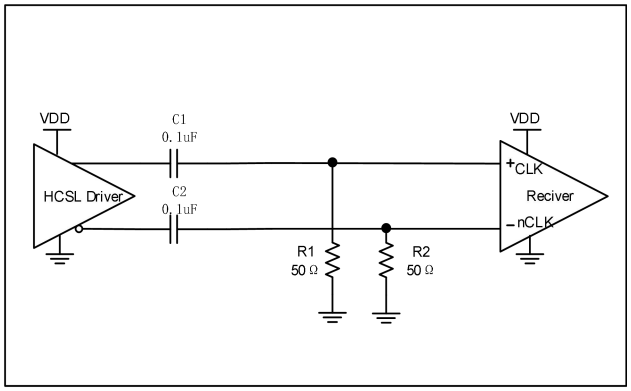


a)AC coupling

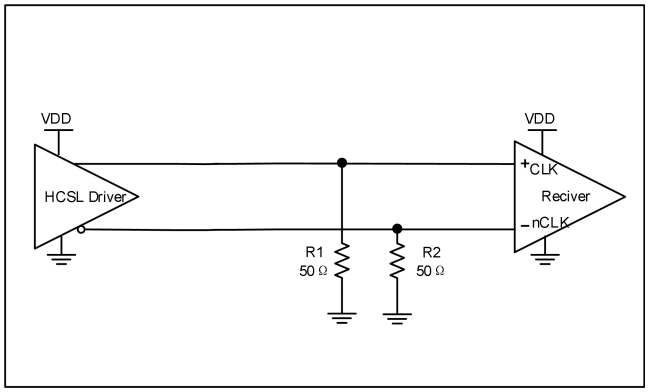


b)DC coupling

Figure6.LVDS Driver



a)AC coupling



b)DC coupling

Figure7.HCSL Driver

Output connection circuit

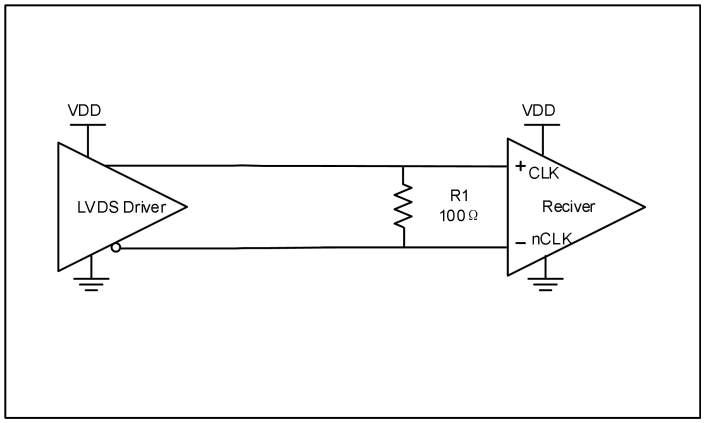
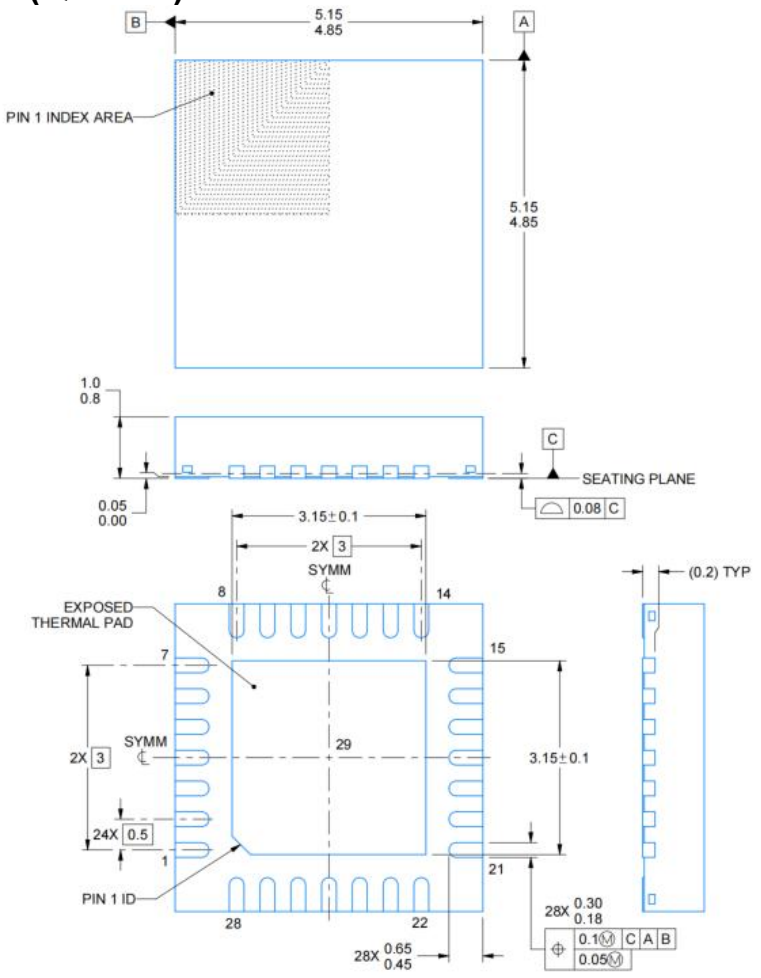


Figure8.LVDS Driver

PACKAGE DIMENSIONS(QFN-28)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.45	0.55	0.65
A3	-	0.20Ref	-	aaa	0.05		
b				bbb	0.10		
D	5.00BSC			ccc	0.10		
E	5.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	3.05	3.15	3.25				
E2	3.05	3.15	3.25				

Reflow profile

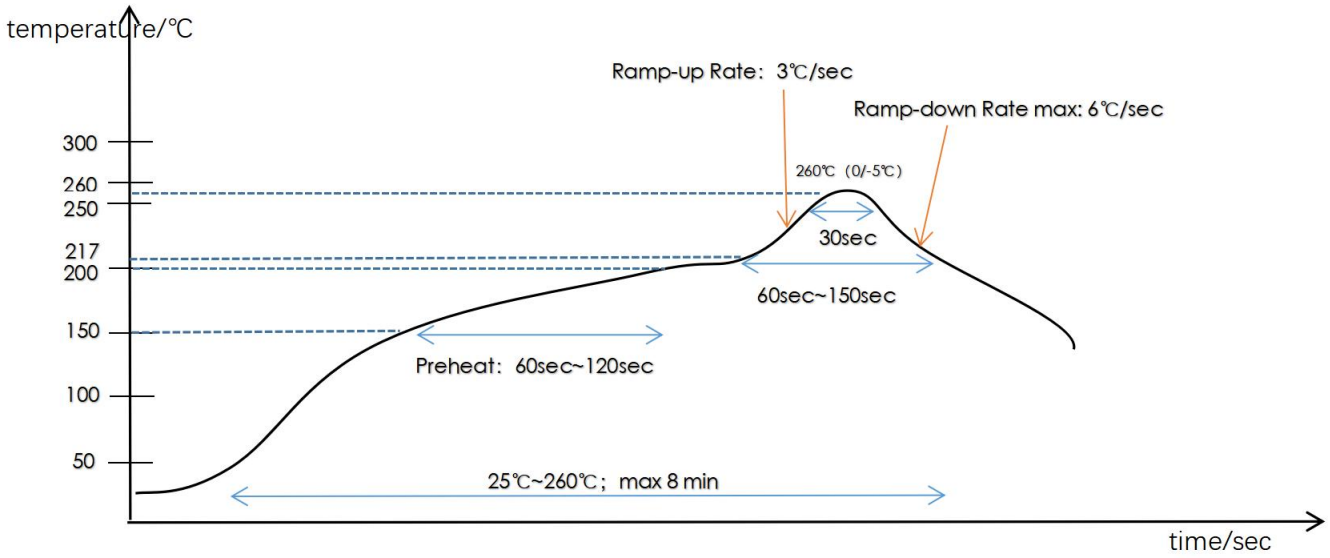


Figure9: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2022.4.27	First Draft.	1.0
2023.8.1	Parameter value update.	1.5
2023.12.05	Modify the LVCMOS input connection	2.0