钍地半导体
Tudi Semiconductor

Product Specification

TUDI-PT7C4302

Real-time Clock Module (3-wire Interface)

网址 www.sztdbdt.com

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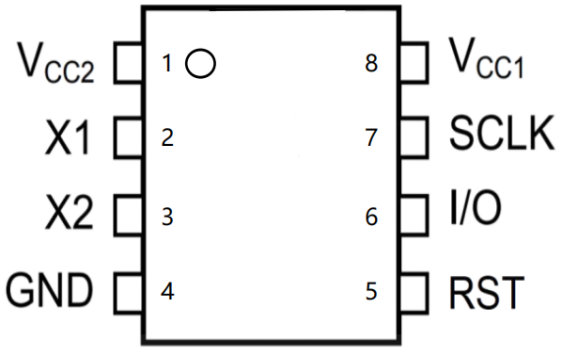
semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- This device uses an external 32.768kHz quartz crystal.
- It features a real-time clock (RTC) that counts seconds, minutes, hours, the date of the month, the month, the day of the week, and the year, with leap-year compensation that remains valid up to the year 2099.
- It contains 31 bytes of RAM for data storage.
- The time-keeping voltage range is from 2.0V to 5.5V.
- It consumes less than 300nA at a voltage of 2.0V.
- It employs a simple 3-wire interface.
- It uses a serial I/O interface to minimize the pin count.
- It supports a burst mode for reading and writing successive addresses in the clock/RAM.
- It is TTL-compatible, with a VCC of 5V.
- It offers an optional industrial temperature range of -40°C to +85°C.
- It can be backed up by a battery.
- It has an on-chip trickle charger for rechargeable energy source backup.
- It is totally lead-free and fully RoHS compliant.
- It is halogen and antimony free, making it a "Green" Device.
- Package form: DIP8 and SOP8



Pin Diagram

Description

The PT7C4302 serial real-time clock is a low-power clock/calendar with a programmable square-wave output and 31 bytes of RAM.Address and data are transferred serially via a 3-wire bus.The clock/calendar provides seconds, minutes, hours, day, date, month, and year information.The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year.The clock supports either the 24-hour or 12-hour format with an AM/PM indicator.More details are shown in the section: overview of functions.

Applications

- Portable instrument
- mobile telephone
- Rechargeable electricity meter,IC card water meter,IC card gas meter
- electrograph

Pin Description

Pin number	Symbol	Function
1	Vcc_2	Primary power supply
2	X1	32.768 kHz crystal
3	X2	32.768 kHz crystal
4	GND	The earth
5	RST	Reset
6	I/O	Data input/output
7	SCLK	Serial clock input
8	Vcc_1	Back up power

Block Diagram

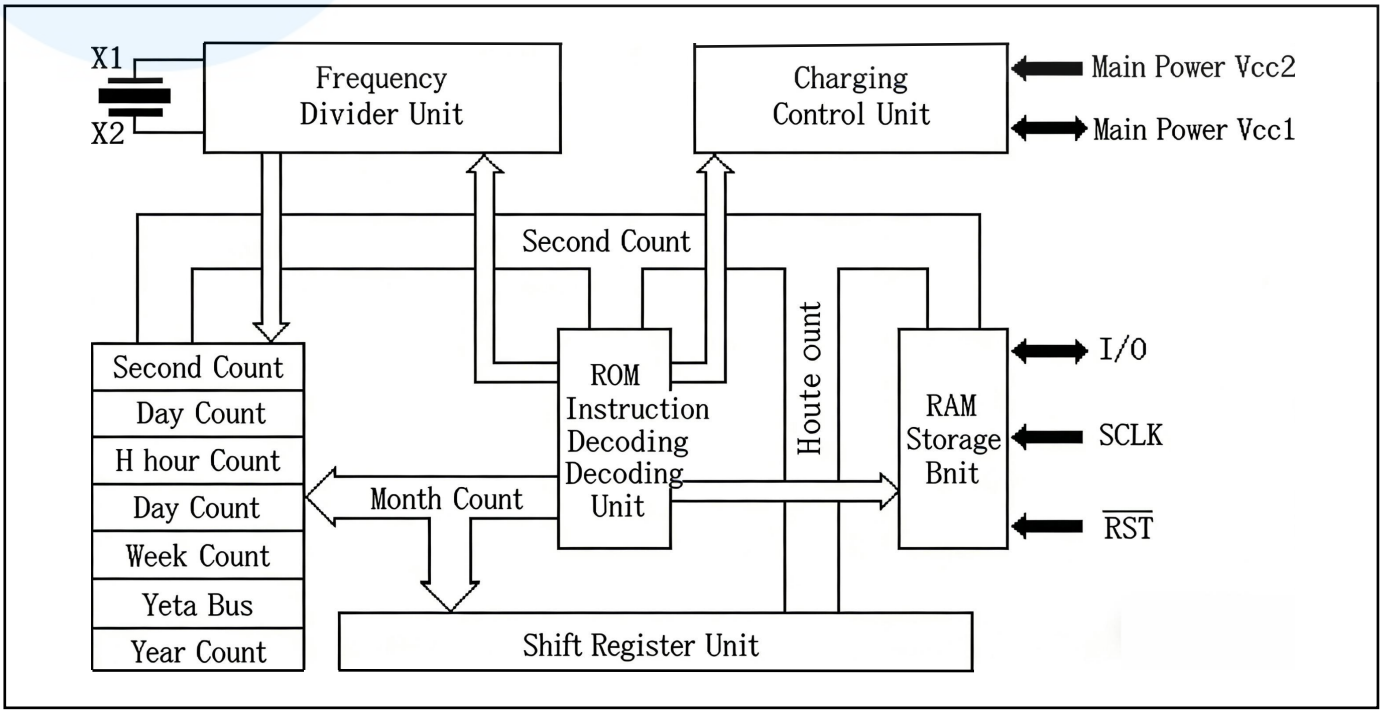
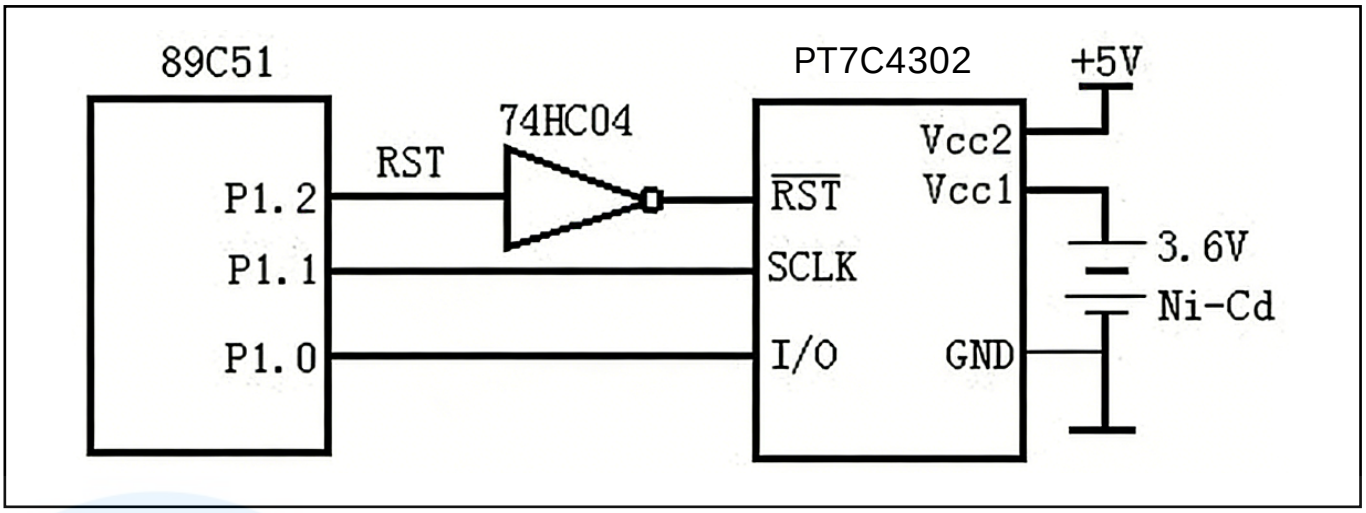


Figure 1 PT7C4302 Internal Block Diagram

Applicative Circuit Diagram



Maximum Rating

Recommended DC operating conditions (=0℃~70℃) Capacitor (TA=25)

Parameter name	Symbol	Rating	Unit
Pin to ground voltage	Vp	-0.5～+7.0	V
Working temperature	TA	-40～+85	℃
Storage temperature	Ts	-55～+125	℃
Welding temperature(10s)	TH	260	℃

Parameter name	Symbol	Test condition	Least value	Representative value	Crest value	Unit
Supply voltage	Vcc1,Vcc2		2.0		5.5	V
Logical 1 input voltage	VIH		2.0		Vcc+0.3	V
Logical 0 input voltage	VIL	VCC=2.0V	-0.3		+0.3	V
		VCC=5V	-0.3		+0.8	V
Input capacitance	C			10		pF
I/O electric capacity	C_{IO}			15		pF
Crystal oscillator capacitor	Cx			6		pF

Note: Limit parameters refer to the limit value that cannot be exceeded under any conditions. If the limit value is exceeded, physical damage such as product deterioration may occur. At the same time, the chip cannot be guaranteed to work properly when approaching the limit parameters.

Electrical Characteristics

DC characteristics (0°C to 70°C; =2.5V to 5.5V)

Parameter name	Symbol	Test condition	Least value	Representative value	Crest value	Unit
Input currenton	ILI				500	μA
I/O leakage current	ILO				500	μA
Logical 1 output voltage	VOH	Vcc=2.5V	1.6			V
		Vcc=5V	2.4			
Logical 0 output voltage	VOL	Vcc=2.5V			0.4	V
		Vcc=5V			0.4	
Supply current	ICC1A	Vcc1=2.5V			0.4	mA
		Vcc1=5V			1.2	
Time holding current	ICC1T	Vcc1=2.5V			0.3	μA
		Vcc1=5V			1	
Quiescent current	ICC1S	Vcc1=2.5V		100		nA
		Vcc1=5V		100		
Supply current	ICC2A	Vcc_2=2.5V			0.425	mA
		Vcc2=5V			1.28	
Time holding current	ICC2T	Vcc2=2.5V			25.3	μA
		Vcc_2=5V			81	
Quiescent current	ICC2S	Vcc2=2.5V			25	μA
		Vcc_2=5V			80	
Charging resistance of trickle current	R1			2		kΩ
	R2			4		
	R3			8		
Charge diode voltage drop of trickle current	VTD			0.7		V

Electrical Characteristics (continuation)

AC characteristics (TA: 0 ° C to 70 ° C; VCC: +5V ±10%

Parameter name	Symbol	Test condition	Least value	Representative value	Crest value	Unit
CLK to RST hold	tcch	Vcc=2V	240			ns
		Vcc=5V	60			
RST of no avail	tcwh	Vcc=2V	4			ns
		Vcc=5V	1			
RST to I/O high impedance	tcdz	Vcc=2V			280	ns
		Vcc=5V			70	
SCLK to I/O high impedance	tccz	Vcc=2V			280	ns
		Vcc=5V			70	
Establish Data to CLK	tdc	Vcc=2V	200			ns
		Vcc=5V	50			
CLK to Data hold	tcdh	Vcc=2V	280			ns
		Vcc=5V	70			
CLK to Data delay	tcdd	Vcc=2V			800	ns
		Vcc=5V			200	
CLK low	tcl	Vcc=2V	1000			ns
		Vcc=5V	250			
CLK Gao	tch	Vcc=2V	1000			ns
		Vcc=5V	250			
CLK frequency	tclk	Vcc=2V			0.5	MHz
		Vcc=5V	DC		2.0	
CLK up and down	tr,tf	Vcc=2V			2000	ns
		Vcc=5V			500	
RST to CLK setup	tcC	Vcc=2V	4			μs
		Vcc=5V	1			

Direction for use ：

The principal components of the serial clock chip are shown in Fig. 1: shift register control logic, oscillator, real-time clock, RAM.
Operating principle: as shown in the figure, after the RST signal is active, the shift register unit receives an 8-bit instruction byte serially from I/O under the control of the SCLK synchronous pulse signal, then the 8-bit instruction byte is converted from serial to parallel and sent to the ROM instruction unit. The ROM instruction decoding unit decodes the 8-bit instruction byte to determine the address of the internal register and the read/write state. Then, under the control the next SCLK synchronous pulse signal, the 8-bit data is written into or read out from the corresponding register. Data transmission can also be in a multi- manner, first write the corresponding 8-bit instruction byte, and then under the synchronization of the continuous SCLK pulse signal, the data byte is continuously written or read out the calendar/clock register (or RAM unit). The number of SCLK pulses in the single-byte mode is 8 plus 8, and in the multi - mode it is 8 plus the maximum number of up to 248.

Reset and Clock Control

All data transfers are initiated by driving RST input to high level. RST input has two functions. First, RST connects the control logic to shift register, allowing the address command sequence to be entered. Second, RST can abort the data transfer.
Data must be valid at the rising edge of the clock during input, and the data bit is output at the falling edge of the clock. If the RST input is low, all data transfers are aborted and the I/O pins put in high-impedance state. The data transfer is illustrated in Fig. 3. RST must be logic 0 at power up until VCC is greater than equal to 2.5V, and SCLK must be logic 0 when RST is driven to logic 1.

Presentation of Information

After following the input read command byte for SCLK cycles, the data byte is output on the falling edge of the subsequent SCLK cycles. Note that each transmitted data bit occurs on the first falling edge after the last bit of the read command byte. As long as the RST remains high, additional SCLK cycles will resend the data byte. This operation enables continuous multi-byte reading capability. Additionally, at each rising edge of the SCLK, the I/O pin remains tri-state. Data output begins from bit .

Data-In

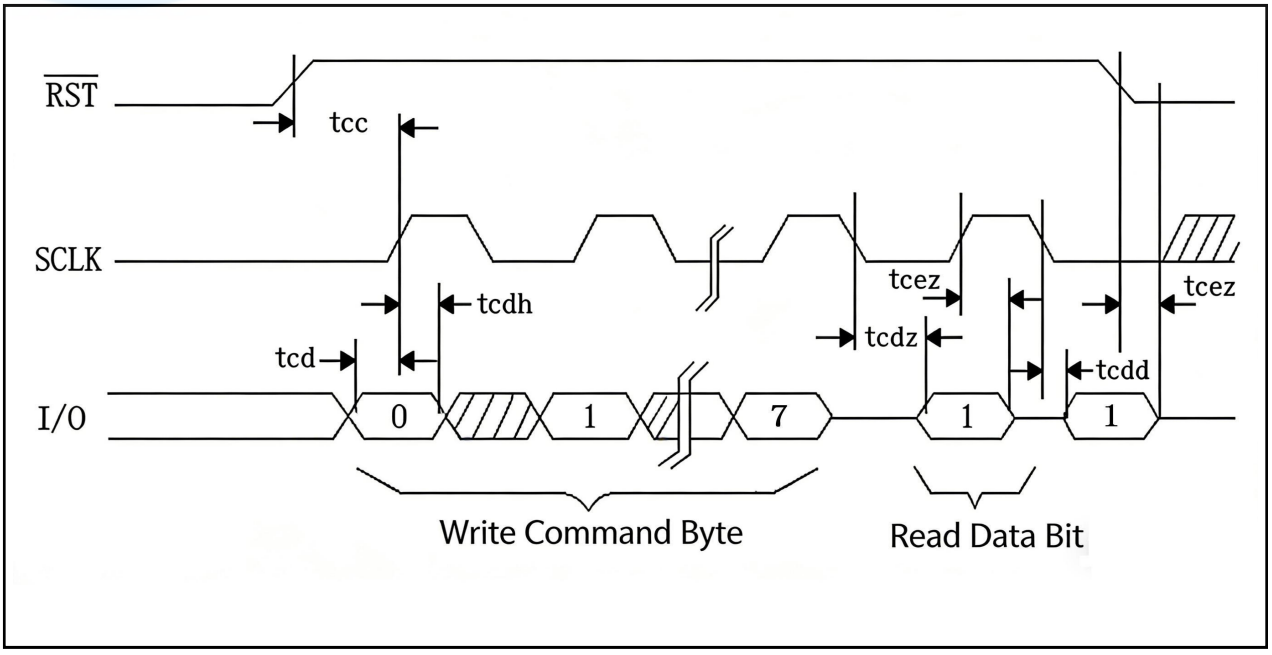
Follow the input write command byte with SCLK cycles, and input data on the rising edge of the next SCLK cycles. Any additional SCLK cycles will be ignored. The input starts from bit .

Multibyte Mode

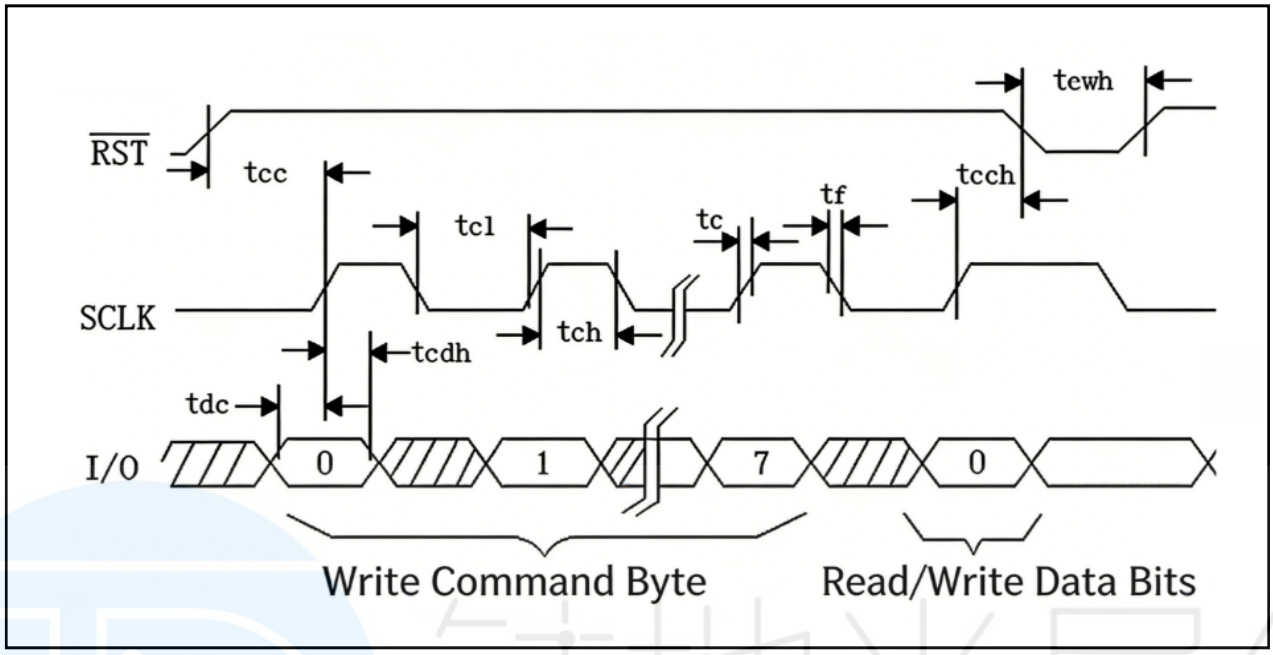
Addressing the clock/calendar or RAM registers as multi-bytes by the 31 (decimal) address (address/command located in to 5 = logical 1). As stated before, bit 6 defines the clock or RAM and bit 0 defines the read or write. Addresses 9 to31 in the clock/calendar register or address 31 in the RAM register cannot store data. Reading or writing in the multi-byte mode starts at bit 0 of 0. When writing the clock register in the multi-byte mode, the first 8 registers have to be written in the order of transmission of the data. However, when the RAM in the multi-byte mode, it is not necessary to write all 31 bytes to transmit the data. Regardless of whether all 31 bytes are written or, each written byte will be transmitted to the RAM.

Function	Bytes	Pulse count
CLOCK	8	72
RAM	31	256

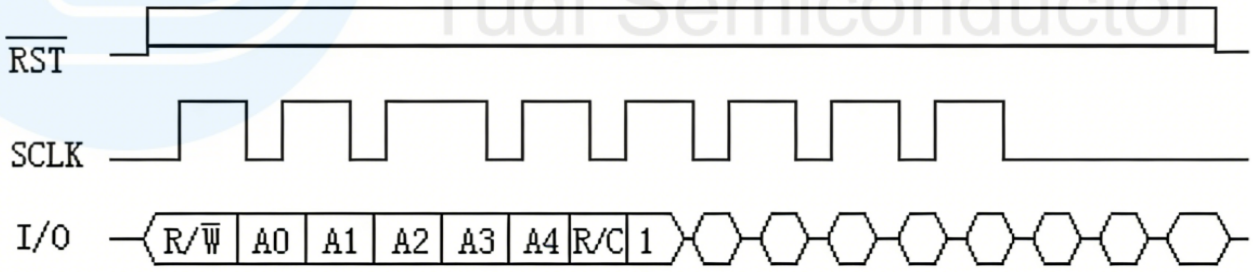
Sequence Diagram: Read Data



Sequence Diagram: Write Data



Single byte read time sequence



Single byte write timing

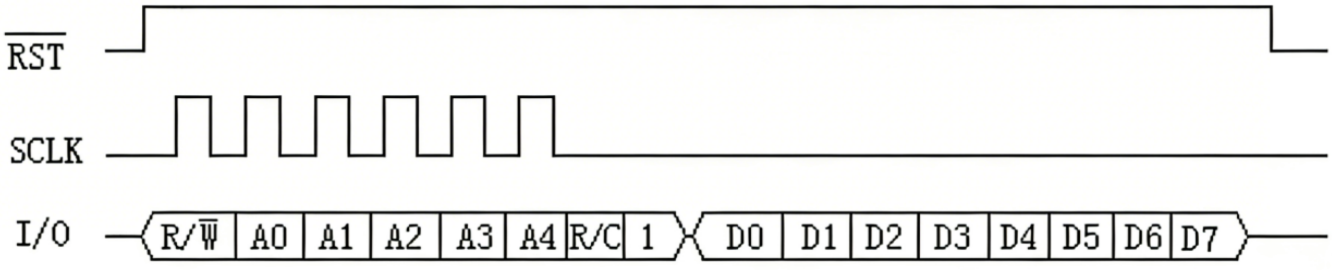


Figure 2 Data Transfer Summary

Command Byte

Command Byte is shown in Fig. 2: each data transfer is initialized by the command byte, the most significant bit MSB (bit 7 must be logical 1. If it is zero, writing to the PT7C4302 is inhibited. Bit 6 is logical 0 for specifying clock/calendar data.ical 1 specifies RAM data. Bits 1 to 5 specify the part -icular register to be read or written to. The least significant bit LSB (bit 0) logical 0 for specifying a write operation (input); logical 1 specifies a read operation (output). The command byte is always entered starting with the least significant LSB bit0.

1	RAM/CLK	A4	A3	A2	A1	A0	Read/Write

Figure 3 Address/Command Byte

Stop the Clock

Bit 7 of the seconds register is defined as the clock halt bit. When this bit is set to a logic 1, the clock oscillator stops and PT7C4302 is placed in low-power standby mode with a current consumption less than 100 nanoamps. When this bit is written to a logic 0 the clock is started.

Write Protection Register

Bit 7 of the write protect register is the write protect bit. Bits 7 down (bits 0-6) are set to zero and read back as zero on a read operation.Bit 7 must be zero before writing to the clock or RAM. When it is high, the write protect bit prevents writing to other register.

AM-PM/12-24 Mode

The bit of the hour register is defined as the or hour mode selection bit. When it is high, the hour mode is selected. In the hour mode, bit is the AM/PM bit, which is logic high to indicate PM. In the hour mode, bit is the th hour bit (hours).

Clock/Calendar

As shown in Figure 4, the clock/calender is contained in 7 write/read registers. The data contained in the clock/calender register is binary-decimal (BCD) code.

Slow Charging (Trickle Charge)Register

This register controls the PT7C4302 trickle charge feature. The simplified circuit in Fig. 4 represents the basic components of the trick charger.The trickle charge select (TCS) bit (bits 4-7) controls the selection of the trickle charger. To prevent it from being accidentally enabledonly the 1010 mode will enable the trickle charger, all other modes will disable the trickle charger. The trickle charger is disabled on power-up the PT7C4302.
The diode select (DS) bits (bits 2-3) select whether one or two diodes are connected between Vcc2 Vcc1. If DS is 01, then one diode is selected; if DS is 10, then two diodes are selected.
If DS is 0 or 11, then the charger is disabled, TCS is not relevant. The RS bits (bits 0-1) select the resistor connected between Vcc and Vcc1. The resistor selected by the resistor select (RS) bits is as follows:

RS bit	Resistor	Typical value
00	/	/
01	R1	2kΩ
10	R2	4k
11	R3	8kΩ

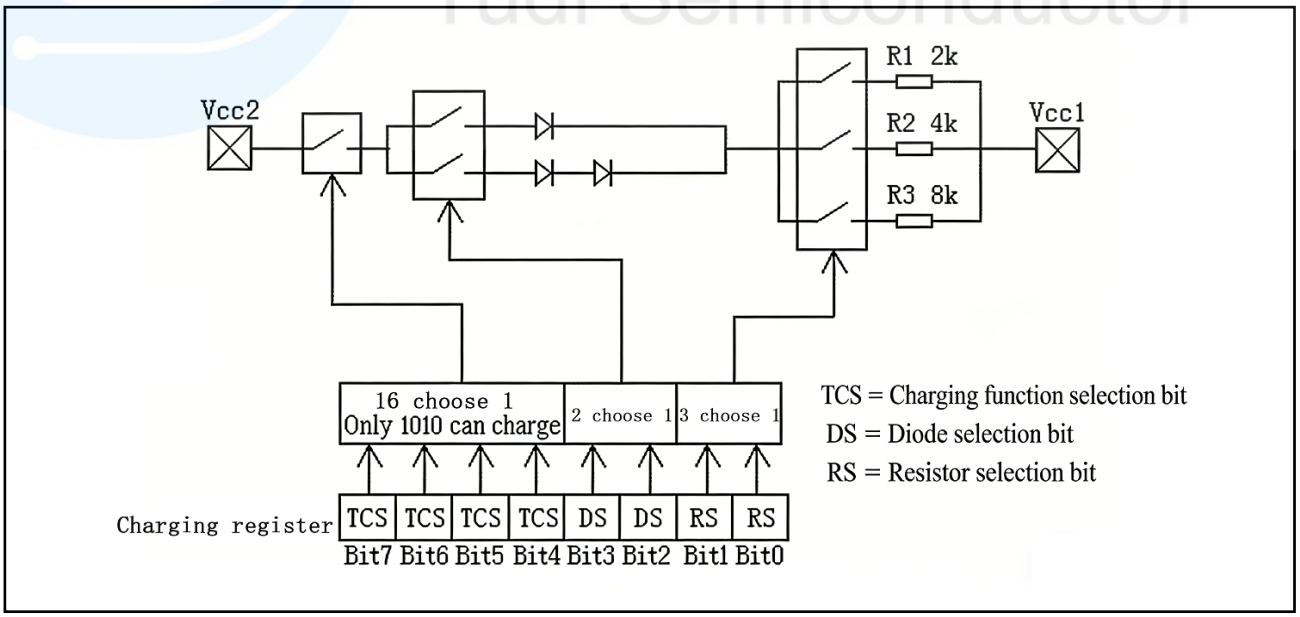


Figure 4 PT7C4302 Programmable Slow Charger

If RS is 00, the charger is disabled, independent of TCS.

The selection of diodes and resistors is determined by the maximum current required for charging the battery and ultracapacitor. The maximum charging current can be specified as follows: The calculation is performed as described. Assume the 5V system power supply is connected to Vcc2 while the supercapacitor is connected to Vcc1. Furthermore, assume a diode and resistor R1 are connected between Vcc2 and Vcc1 during slow charger operation. The maximum current can be calculated as follows:

$$Imax = (5.0V\text{-diode voltage drop}) / R1 = (5.0V\text{-}0.7V) / 2k\Omega = 2.2mA$$

Obviously, when the supercapacitor is charged, the voltage between Vcc2 and Vcc1 decreases, and therefore the charging current will decrease

Clock/Calendar Multi-Byte (Burst) Mode

The clock/calendar command byte can specify the multi-byte operation mode. In this mode the first 8 clock/calendar registers can be read or written starting with bit 0 of address 0 (see Fig. 4).
When the multi-byte mode for writing the clock/calendar is specified, no data is to any of the 8 clock/calendar registers (including the control register) if the write protection bit is set to high level. The slow charger is not accessible in the multibyte mode.

RAM

Static RAM is a sequential 31 x8 byte in the RAM address space.

RAM Multi-Byte Mode

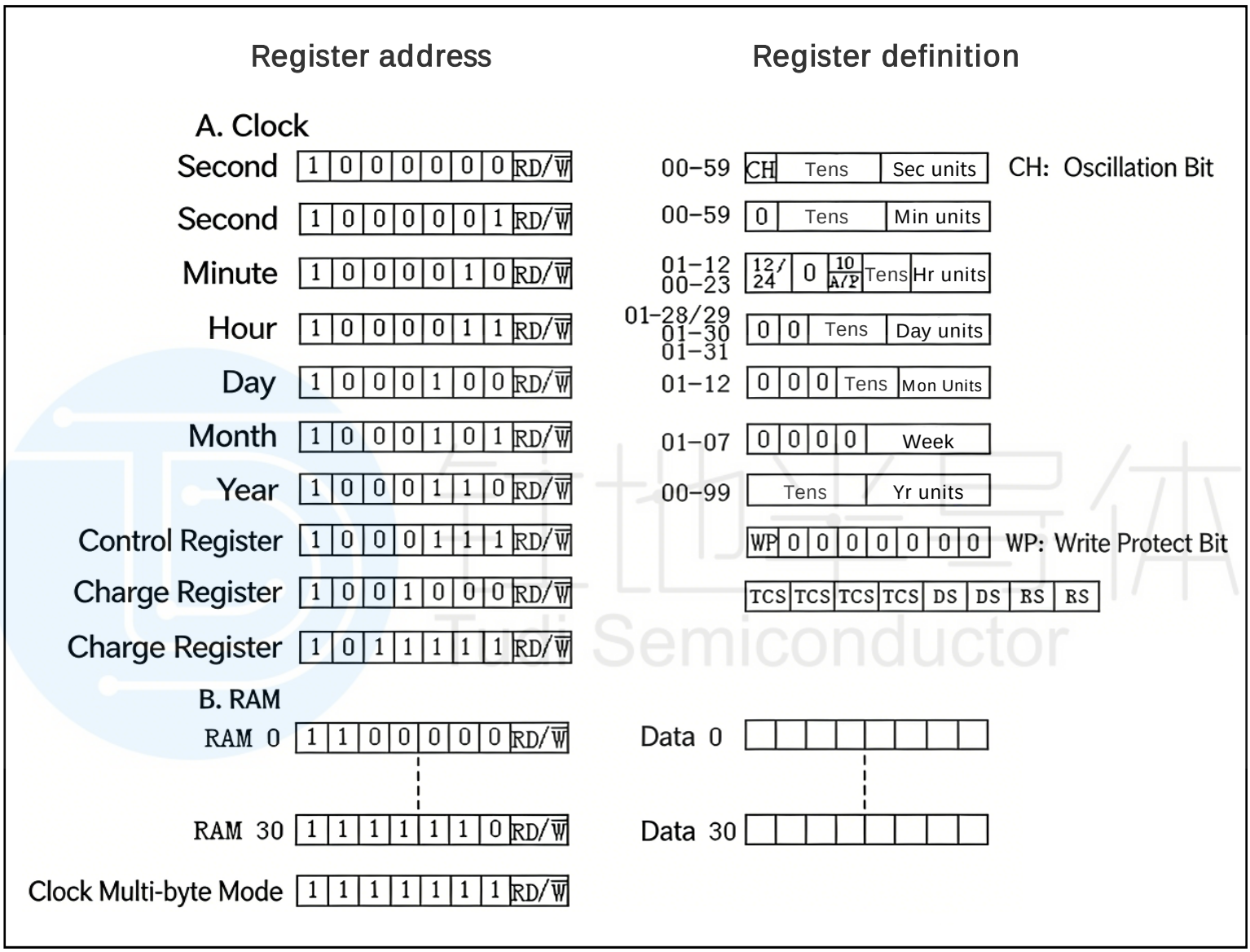
RAM command bytes can specify multi-byte working mode. In this mode, the byte RAM register can be read or written sequentially from the bit of address (see Figure).

Crystal Selection

The crystal oscillator at 32.768kHz can be directly connected to PT7C4302 through pins 2 and 3 (X 1 and X2). The specified load capacitance (CL) of the selected crystal oscillator should be 6 pF.

Register Overview

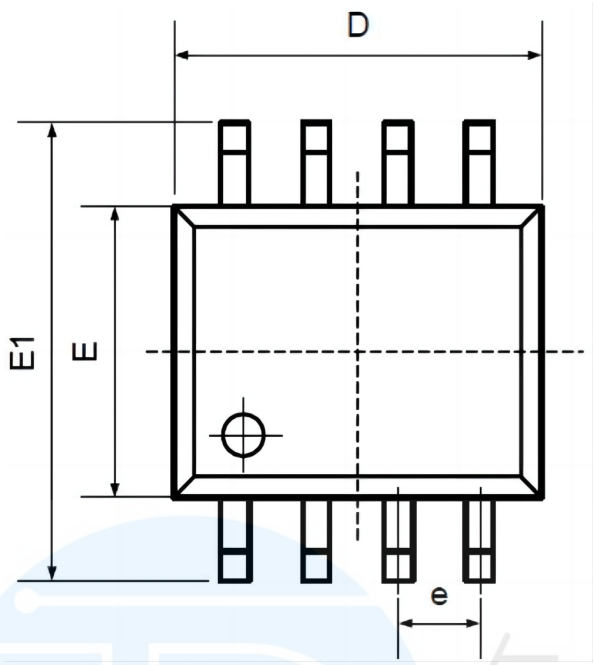
The register data format is summarized in Figure 5.

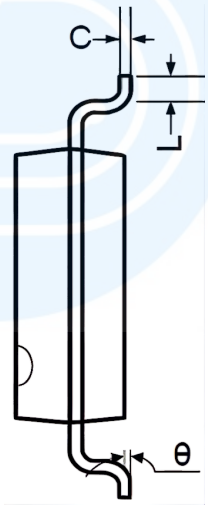


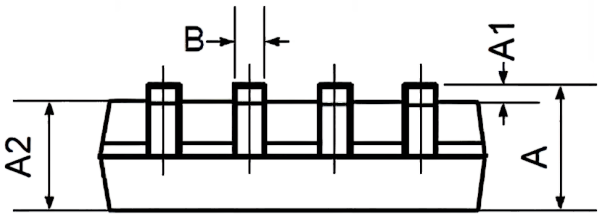
Power Supply Control

Vcc1 provides low power in a single power supply and battery powered system and provides low power battery backup. Vcc2 provides the primary power supply in a dual power supply system, at which time Vcc1 is connected to the backup power supply to save time information and data in the absence of the primary power supply. The PT7C4302 is powered by the higher of Vcc1 or Vcc2. When Vcc2 exceeds Vcc1+0.2V, the PT7C4302 is powered by Vcc2. When Vcc2 +0.2V is lower than Vcc1, the PT7C4302 is powered by Vcc1.

Package SOP8

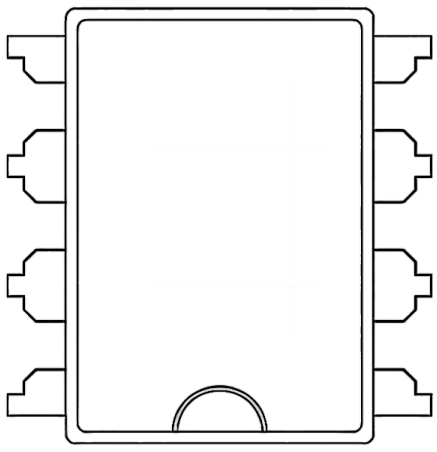


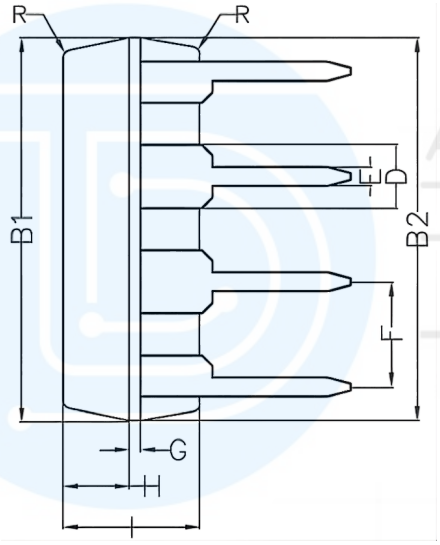


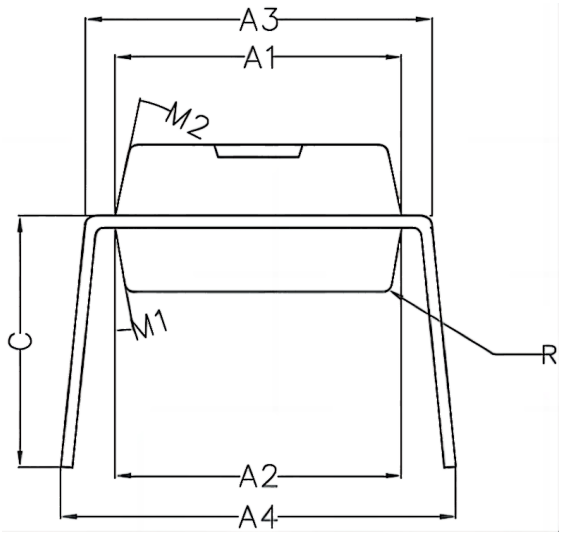


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature	Operating Voltage
PT7C4302PE-TUDI	DIP8	Tube,50,A box of 2000	PT7C4302PE	- 40°C to 85°C	2.0-5.5V
PT7C4302WEX-TUDI	SOP8	Tape,Reel,2500	PT7C4302WE		

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