
3D LF Receiver and UHF Transmitter

Introduction

The ATA5700/ATA5702 is a highly integrated, ultra-low power car access controller for Passive Entry/Passive Start (PEPS) and Remote Keyless Entry (RKE) applications with an embedded AVR[®] 8-bit microcontroller in a single QFN 38 package. The device includes a highly sensitive 3D Low Frequency (LF) receiver, an immobilizer front end, and an Ultra High Frequency (UHF) Amplitude Shift Keying (ASK)/Frequency Shift Keying (FSK) Radio Frequency (RF) transmitter. It combines ultra-low power LF technology with outstanding RF performance.

The low power microcontroller is based on the AVR-enhanced Reduced Instruction Set Computer (RISC) architecture. It has a rich set of digital peripherals, including a watchdog timer, a real time counter (RTC) several 8/16-bit timers, serial interfaces (SPI, TWI) and 19 General Purpose Input Output (GPIO) ports. It is equipped with low power memories such as Static RAM (SRAM), 32 KB Flash memory, and Secure EEPROM.

In addition, the core is supported by power-saving co-processing units, such as a powerful Advanced Encryption Standard (AES) cipher engine and an autonomous operating protocol handler unit to support the data communication of LF receiver and transponder.

The highly sensitive 3D LF receiver enables the Integrated Chip (IC) to listen perpetually for wake-up pattern during the low power standby mode. If the IC is woken up and active, the LF receiver serves as a receive path for the data communication. In combination with the integrated and highly accurate logarithmic 3D Received Signal Strength Indicator (RSSI), the LF receiver supports PEPS positioning requirements.

The RSSI control unit supports logarithmic to linear conversion, 3D vector sum calculation and the RSSI calibration algorithm.

The ATA5702 has an RF transmitter implemented with a fractional-N Phased Locked Loop (PLL) for high data rates, and is equipped with Gaussian waveshaping capability. The transmitter is designed for the ISM frequency bands in the ranges of 310 MHz to 318 MHz, 418 MHz to 477 MHz and 836 MHz to 956 MHz.

To support immobilizer functions, the IC is prepared for battery-less emergency operation. It contains a built-in 3D transponder front end for wireless power supply and bidirectional communication via the LF antennas.

The ATA5700/ATA5702 is well prepared for PEPS applications with its low power AVR RISC microcontroller with high performance security AES Crypto Unit, and power-saving digital and analog peripherals combined with sufficient memory space.

Features

- System solution for immobilizer and PEPS functionality
- Optional integrated open source immobilizer software stack supports automotive immobilizer

- Supply voltage range from 2.0V to 4.2V
- Temperature Range from -40 to +85°C
- Excellent ESD protection at all pins (± 4 kV HBM)
- Small 5x7 mm² QFN 38 pin package with wettable flanks

Ultra-low power AVR Microcontroller

- 32 Kbyte flash
- EEPROM, 100000 write cycles at 25°C, 20 years of data retention
- Secure EEPROM – Flexible memory lock and protection features
- SRAM
- 19 GP I/Os
- 2 SPI, 2 TWI interfaces, debug-wire
- 128-bit AES crypto unit
- Secure and fast direct access to AES key memory
- Enhanced LF debug features (output mode for LF receiver and transponder signals)
- Low power Power-on Reset (POR) and brown-out detection
- Voltage monitor for battery surveillance

3D LF Receiver

- Supports LF frequency range from 100 kHz to 150 kHz
- Integrated resonance frequency tuning for 3D antenna
- Integrated quality factor tuning for 3D antenna
- Programmable high and low quality factor receive mode
- Data rates: 1.95, 3.9 and 7.8 Kbit/s with 125 kHz carrier, OOK, Manchester coded
- Programmable Manchester violation codes ($\frac{1}{2}$ bit step size, max. 2 bit L/H)
- Programmable wake-up receiver sensitivities for achieving a range of up to 10m
- Low supply current for all three channels (extended power-down listen mode)
- Ultra-low power LF polling mode for enhanced battery life

LF RSSI

- Fast logarithmic 9-bit digital RSSI field strength measurement of all three channels simultaneously
- High RSSI accuracy due to internal calibration procedure against gain impairment between channels due to aging, drift and variations of supply voltage
- RSSI control unit supports logarithmic to linear conversion, vector sum calculation and the calibration algorithm

3D Transponder

- Transponder operation (cap charging, gap detection and load modulation) on all three channels in parallel with or without battery
- Battery-less operation down to coupling factors < 1%
- Bi-phase, Manchester modulation with programmable NRZ code insertion for code violation
- Autonomous operating Codecs for enhanced LF communication range: Manchester (uplink) and BPLM, QPLM telegrams (downlink)
- Data rates: 1.95 and 3.9 Kbit/s with 125 kHz carrier, OOK, Manchester and bi-phase coded
- Power management unit

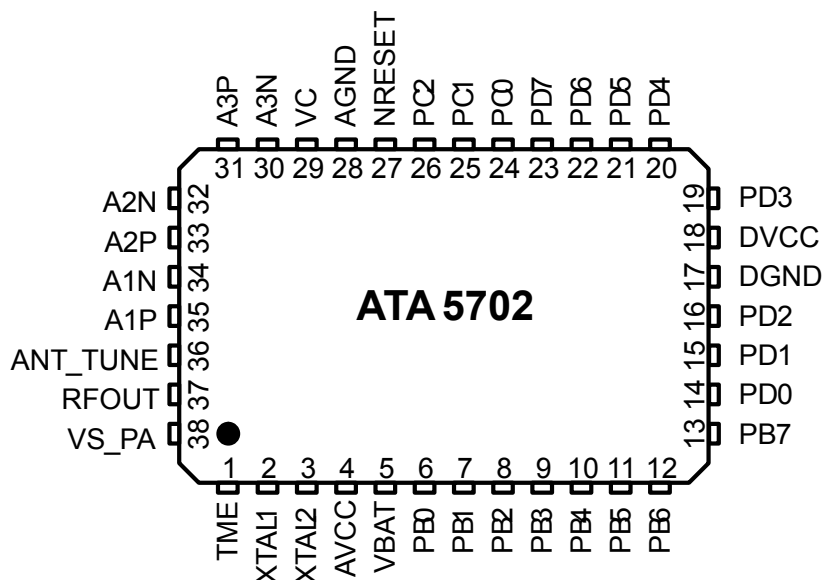
UHF Transmitter (ATA5702 only)

- Supports UHF frequency ranges with one 24.305 MHz crystal
- Low Band – 310 to 318 MHz, 418 to 477 MHz
- High Band – 836 to 956 MHz
- Programmable channel frequency with Fractional-N PLL
- Programmable output power from -12 to +14.5 dBm
- Supported modulations – ASK, FSK and GFSK (FSK deviation: ± 0.375 to ± 93 kHz)
- Data rates up to 80 Kbit/s (buffered, Manchester coded)
- Integrated resonance frequency tuning for loop antenna

1. Pin Description

The pin description of the ATA5702 is illustrated in the following figure.

Figure 1-1. ATA5702 Pin Description



The pin description of the ATA5702 is provided in the following table.

Table 1-1. Pin Description

Pin No	Pin Name	Standard Function	Pad Cell Function Wake-up Input	Alternate Function
1	TME	Test mode enable	-	-
2	XTAL1	Crystal oscillator input pin	-	-
3	XTAL2	Crystal oscillator output pin	-	-
4	AVCC	RF front-end supply regulator output	-	-
5	VBAT	Power supply voltage for battery	-	-
6	PB0	I/O port	-	PCINT0: Pin Change Interrupt 0 MISO2: SPI 2 Master In Slave Out SDA2: TWI 2 Serial Data TRC_VAL_N: Trace Not Valid
7	PB1	I/O port	-	PCINT1: Pin Change Interrupt 1

Pin No	Pin Name	Standard Function	Pad Cell Function Wake-up Input	Alternate Function
				MOSI2: SPI2 Master Out Slave In SCL2: TWI 2 Serial Clock TRC_CLK: Trace Clock
8	PB2	I/O port	-	PCINT2: Pin Change Interrupt 2 SCK2: SPI 2 Clock TRC_DAT: Trace Data
9	PB3	I/O port	-	PCINT3: Pin Change Interrupt 3 TM4: Timer modulator 4 output
10	PB4	I/O port	-	PCINT4: Pin Change Interrupt 4
11	PB5	I/O port	-	PCINT5: Pin Change Interrupt 5 MISO: SPI Master In Slave Out
12	PB6	I/O port	-	PCINT6: Pin Change Interrupt 6 MOSI: SPI Master Out Slave In
13	PB7	I/O port	-	PCINT7: Pin Change Interrupt 7 SCK: SPI Clock
14	PD0	I/O port	-	PCINT8: Pin Change Interrupt 8

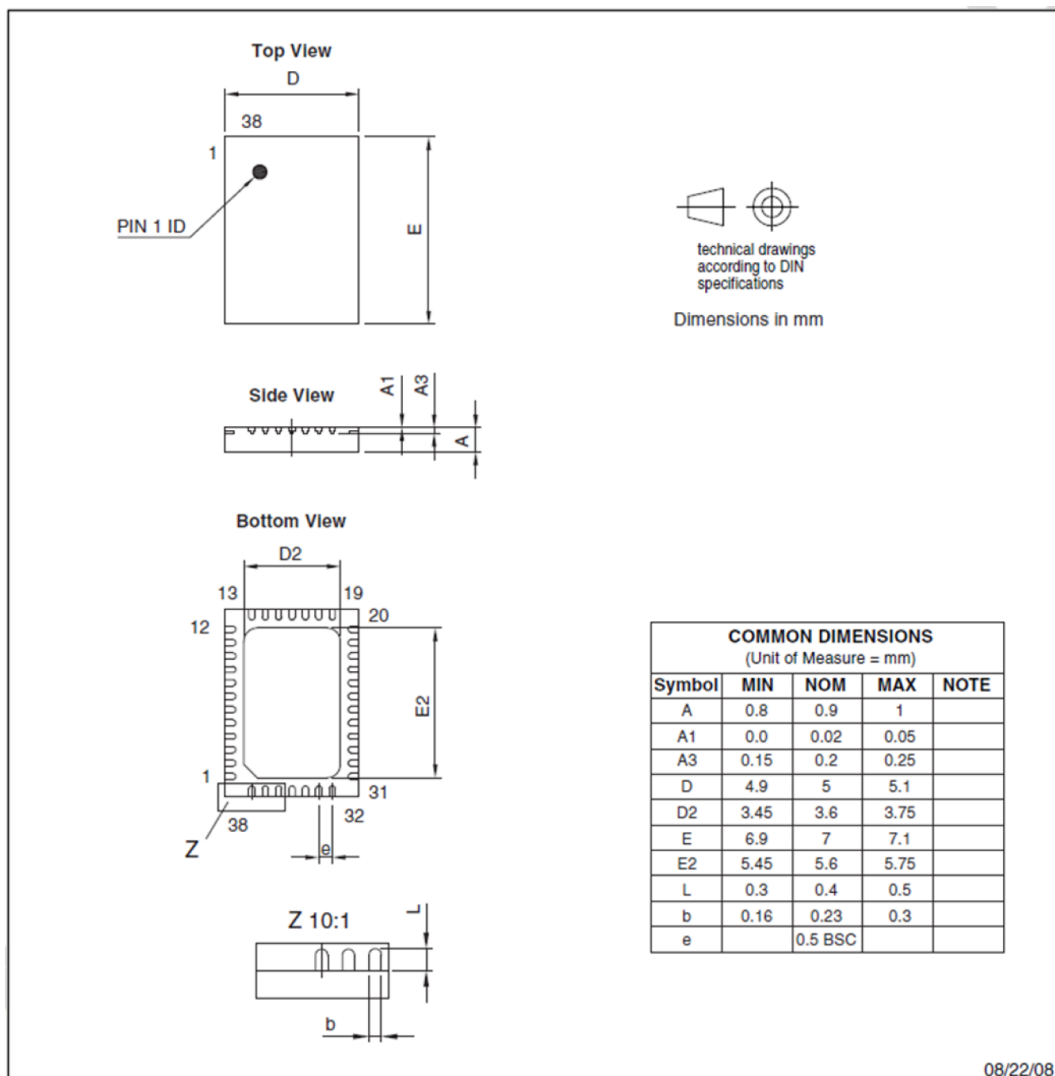
Pin No	Pin Name	Standard Function	Pad Cell Function Wake-up Input	Alternate Function
				TEI: External Timer input clock EXCIN: External Clock Input
15	PD1	I/O port	NPWRON0 Low active power-on signal LED0 LED driver output	PCINT9: Pin Change Interrupt 9 NSS: SPI Not Slave Select INT0: External interrupt 0
16	PD2	I/O port	NPWRON1 Low active power-on signal LED1 LED Output	PCINT10: Pin Change Interrupt 10 TM1: Timer modulator 1 output Event: (Software)
17	DGND	Digital ground	-	-
18	DVCC	Digital Supply Regulator Output	-	-
19	PD3	I/O port	NPWRON2 Low active power-on signal	PCINT11: Pin Change Interrupt 11 CLKOUT: Clock output TM2: Timer modulator 2 output
20	PD4	I/O port	NPWRON3 Low active power-on signal	PCINT12: Pin Change Interrupt 12 INT1: External interrupt 0 TM3: Timer modulator 3 output TMDI: Transparent Mode Data Input
21	PD5	I/O port	NPWRON4 Low active power-on signal	PCINT13: Pin Change Interrupt 13

Pin No	Pin Name	Standard Function	Pad Cell Function Wake-up Input	Alternate Function
				TM0: Timer modulator 0 output TICP: External Timer input capture
22	PD6	I/O port	NPWRON5 Low active power-on signal	PCINT14: Pin Change Interrupt 14 SCL: TWI Serial Clock
23	PD7	I/O port	NPWRON6 Low active power-on signal	PCINT15: Pin Change Interrupt 15 SDA: TWI Serial Data
24	PC0	I/O port	LED2 LED driver Output	-
25	PC1	I/O port	LED3 LED driver output	-
26	PC2	I/O port	PWRON High active power-on signal LED4 LED driver output	LFEVENT: LF receiver hardware controlled event output
27	NRESET	Not Reset	-	-
28	AGND	Analog ground	-	-
29	VC	Power supply voltage for the microcontroller. At this pin a capacitor must be connected capacitance CBUF to buffer the voltage during field supply mode	-	-
30	A3N	Analog negative input coil pin 3 for Channel 3 of LF receiver and transponder	-	-
31	A3P	Analog positive input coil pin 3 for Channel 3 of LF receiver and transponder	-	-
32	A2N	Analog negative input coil pin 2 for Channel 2 of LF receiver and transponder	-	-

Pin No	Pin Name	Standard Function	Pad Cell Function Wake-up Input	Alternate Function
33	A2P	Analog positive input coil pin 2 for Channel 2 of LF receiver and transponder	-	-
34	A1N	Analog negative input coil pin 1 for Channel 1 of LF receiver and transponder	-	-
35	A1P	Analog positive input coil pin 1 for Channel 1 of LF receiver and transponder	-	-
36	ANT_TUNE	Antenna tuning input	-	-
37	RFOUT	Power amplifier output	-	-
38	VS_PA	Power amplifier supply	-	-

2. Package Information

Figure 2-1. ATA5700/ATA5702 Package Details



3. Document Revision History

Rev A - 10/2017

Section	Changes
Document	Initial Release

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