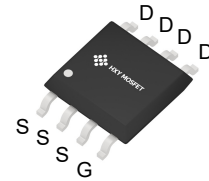




## Description

The NTMS4177P uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

## General Features

$V_{DS} = -30V$   $I_D = -12A$

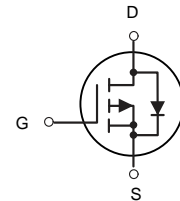
$R_{DS(ON)} < 15m\Omega @ V_{GS}=10V$

## Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NTMS4177P	SOP-8	HXY MOSFET	3000

## Absolute Maximum Ratings( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D @ T_A=25^\circ C$	Drain Current, $V_{GS} @ 10V$	-12	A
$I_D @ T_A=70^\circ C$	Drain Current, $V_{GS} @ 10V$	-9.1	A
$I_{DM}$	Pulsed Drain Current	-40	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation	2.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient	50	$^\circ C/W$



**Electrical Characteristics@T<sub>J</sub>=25 °C(unless otherwise specified)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = -250μA	-30	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V,	-	-	-1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.0	-1.6	-2.5	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>Note3</small>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	10	15	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5A	-	17	24	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> =0V, f=1.0MHz	-	1770	-	pF
C <sub>oss</sub>	Output Capacitance		-	233	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	206	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -15V, I <sub>D</sub> = -5A, V <sub>GS</sub> = -10V	-	22	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.0	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	1.8	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = -15V, I <sub>D</sub> = -10A, V <sub>GS</sub> =-10V, R <sub>GEN</sub> =2.5Ω	-	9	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	13	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	48	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	20	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	-12	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-60	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> = -15A	-	-0.8	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>J</sub> =25°C,	-	64	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = -24V, I <sub>F</sub> =-2.8A, dI/dt=-100A/μs	-	25	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T<sub>J</sub>=25°C, V<sub>GS</sub>=10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=-12.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



## Typical Characteristics



Figure 1. Output Characteristics

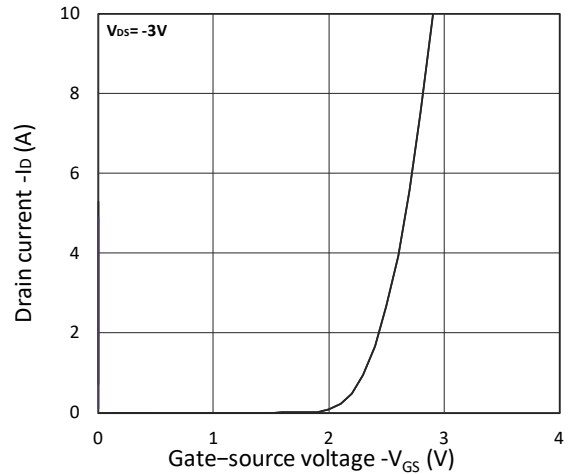


Figure 2. Transfer Characteristics



Figure 3. Forward Characteristics of Reverse

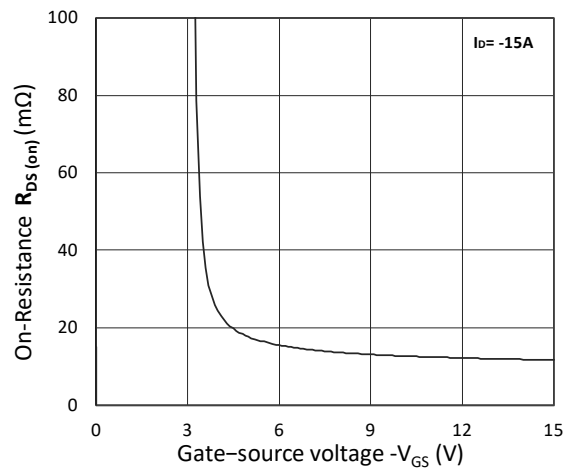


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

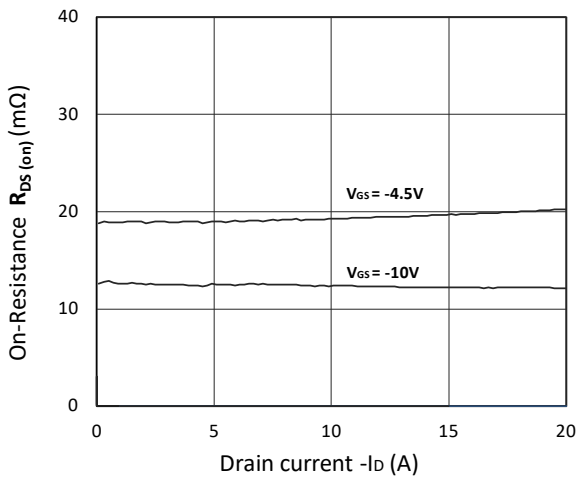


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

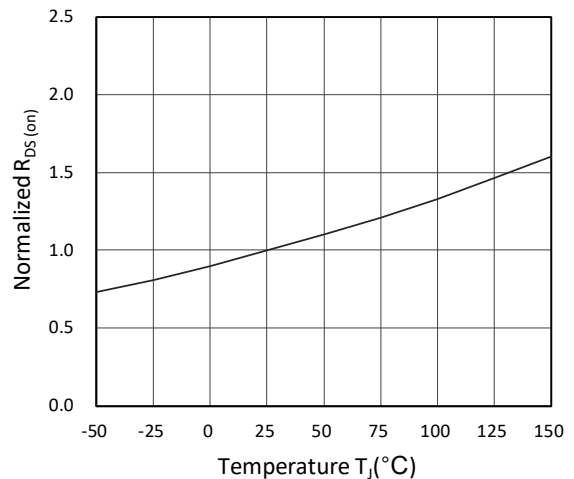


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

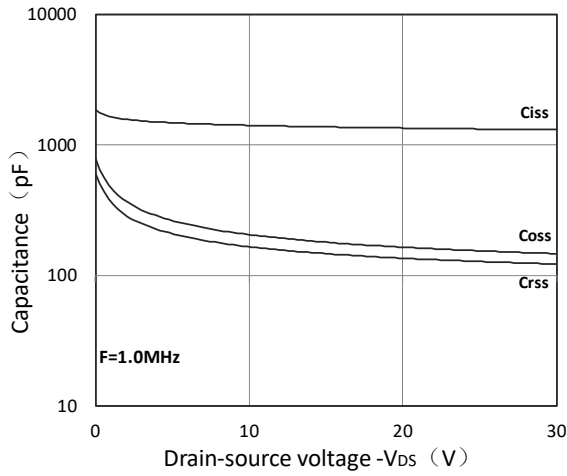


Figure 7. Capacitance Characteristics



Figure 8. Gate Charge Characteristics

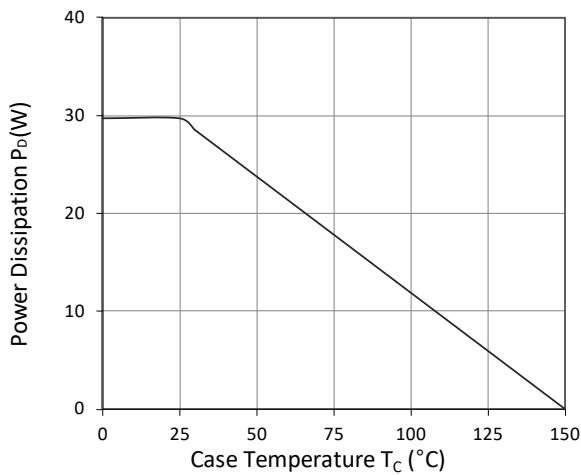


Figure 9. Power Dissipation

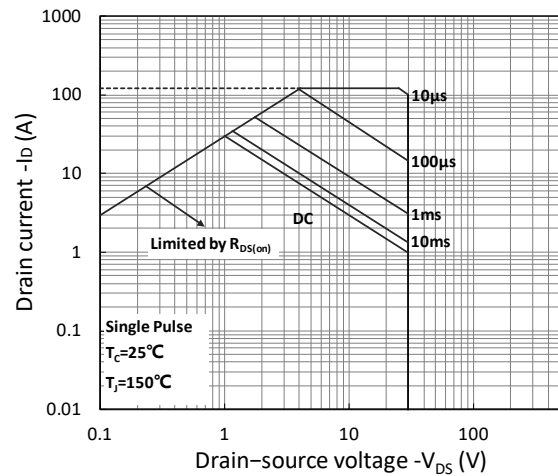


Figure 10. Safe Operating Area

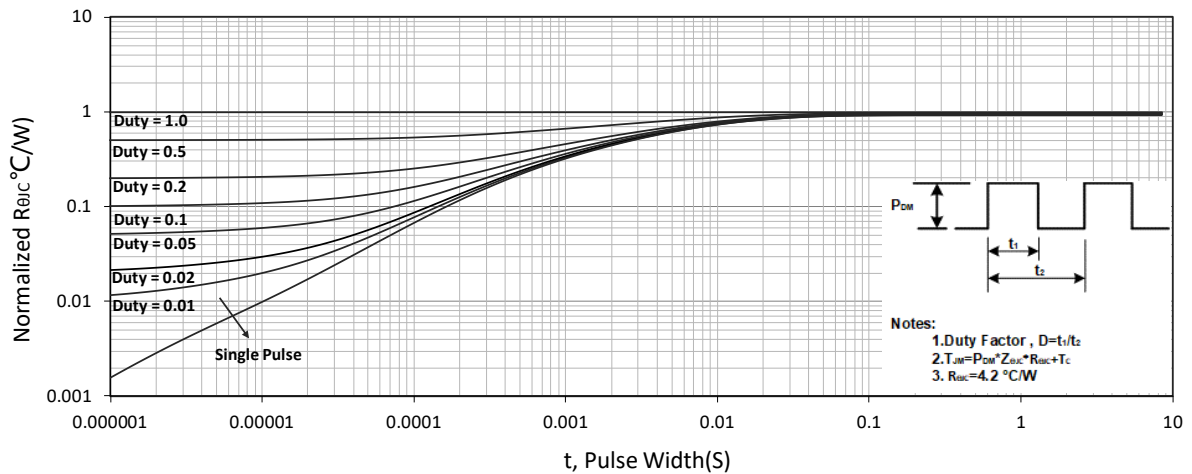


Figure 11. Normalized Maximum Transient Thermal Impedance

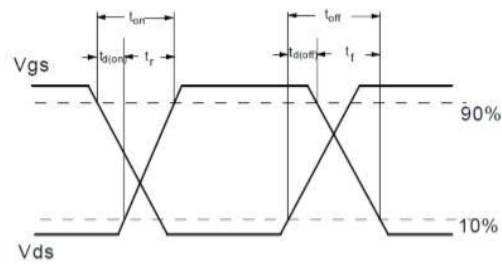
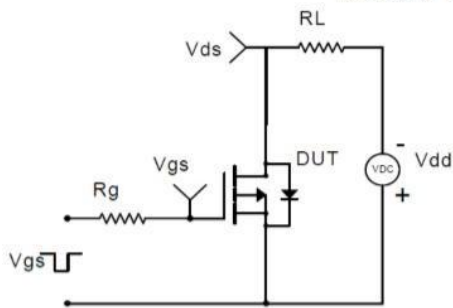


## Test Circuit

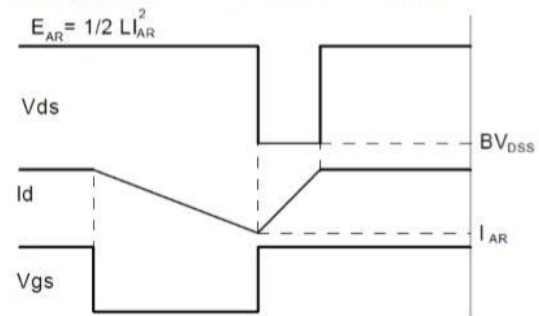
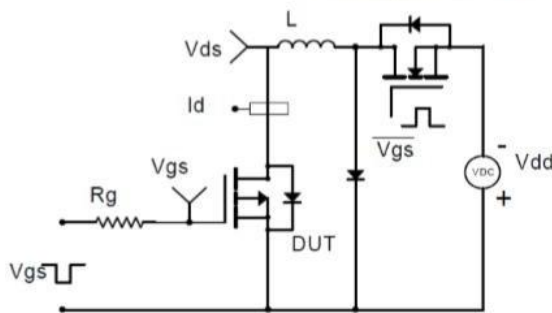
### Gate Charge Test Circuit & Waveform



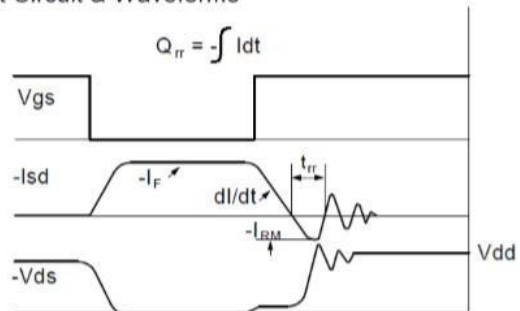
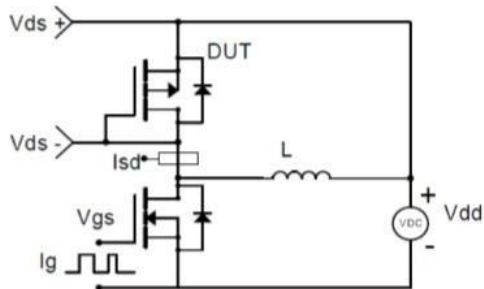
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

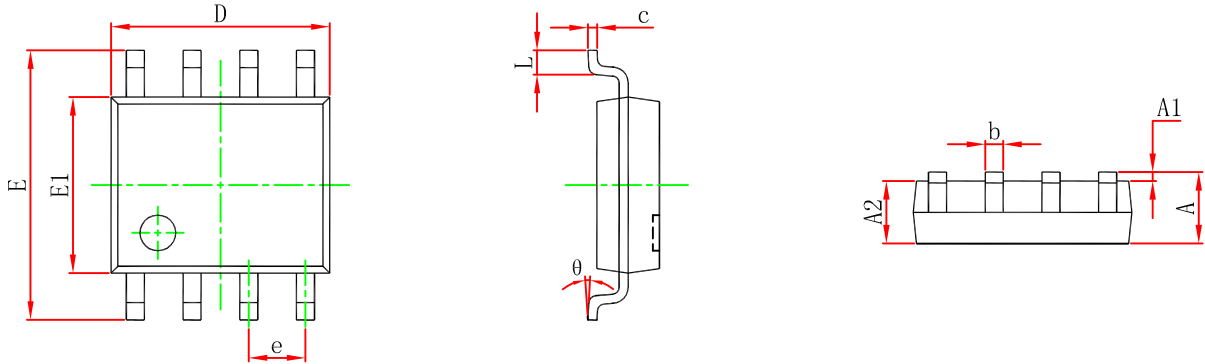


### Diode Recovery Test Circuit & Waveforms





### SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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