NOVOSENSE
纳芯微电子

NSI1303M/Dx

High Reliability Reinforced Isolated Sigma-Delta Modulator with Internal Clock

Datasheet (EN) 1.1

Product Overview

The NSI1303 is a high performance Σ-Δ modulator with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±50mV (±64mV full-scale) or ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The analog input is amplified and continuously sampled by a second-order Σ-Δ modulator and converted to a high speed, single bit data stream. The output bit-stream of the NSI1303 is synchronized to the internally generated clock. NSI1303 can achieve 16 bits resolution and an 85dB (typ) signal to noise ratio (SNR) at 78.125kSPS by using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream from 20MHz internal sampling clock.

The fail-safe functions including input common-mode overvoltage detection and missing AVDD detection simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{RMS} Insulation Voltage
- 10MHz and 20MHz internal clock frequency options
- ±50mV or ±250mV Linear Input Voltage Range
- Excellent DC Performance:
  - Offset Error: ±50µV or ±100µV (Max)
  - Offset Drift: ±1µV/℃ (Max)
  - Gain Error: ±0.2% (Max)
  - Gain Drift: ±40ppm/℃ (Max)
- High CMTI: 150kV/µs (Typ)
- System-Level Diagnostic Features:
  - AVDD monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40℃~125℃
- RoHS-Compliant Packages:
  - SOP8(300mil)
  - SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Shunt current monitoring
- AC motor controls
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	*Package*	*Body Size*
NSI1303M/Dx-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1303M/Dx-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

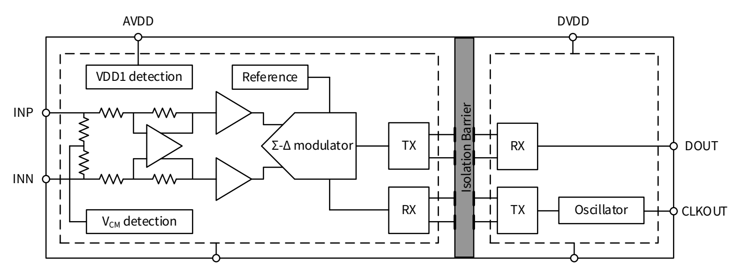


Figure 1. NSI1303M/Dx Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS 3
2. ABSOLUTE MAXIMUM RATINGS(1) 5
3. ESD RATINGS(1) 5
4. RECOMMENDED OPERATING CONDITIONS 5
5. THERMAL INFORMATION 6
6. SPECIFICATIONS 6
6.1. ELECTRICAL CHARACTERISTICS: NSI1303M/D0X 6
6.2. ELECTRICAL CHARACTERISTICS: NSI1303M/D2X 8
6.3. TIMING CHARACTERISTICS 9
6.4. TYPICAL PERFORMANCE CHARACTERISTICS 10
7. HIGH VOLTAGE FEATURE DESCRIPTION 13
7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS 13
7.2. INSULATION CHARACTERISTICS 14
7.3. REGULATORY INFORMATION 15
8. FUNCTION DESCRIPTION 15
8.1. OVERVIEW 15
8.2. ANALOG INPUT 16
8.3. DIGITAL OUTPUT 16
8.4. FAIL-SAFE OUTPUT 17
9. APPLICATION NOTE 18
9.1. TYPICAL APPLICATION CIRCUIT 18
9.2. SHUNT RESISTOR SELECTION 19
9.3. DIGITAL FILTER 19
9.4. PCB LAYOUT 20
10. PACKAGE INFORMATION 21
11. ORDERING INFORMATION 24
12. DOCUMENTATION SUPPORT 24
13. TAPE AND REEL INFORMATION 25
14. REVISION HISTORY 27

1. Pin Configuration and Functions

Table 1.1 NSI1303M/Dx Device Comparison Table

PART NUMBER	LINEAR INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	INTERNAL CLOCK FREQUENCY	DIGITAL OUTPUT INTERFACE
NSI1303M01	±50mV	4.9kΩ	10MHz	Uncoded CMOS (clock rising edge effective)
NSI1303M21	±250mV	22kΩ		
NSI1303M02	±50mV	4.9kΩ	20MHz	
NSI1303M22	±250mV	22kΩ		
NSI1303D01	±50mV	4.9kΩ	10MHz	Uncoded CMOS (clock falling edge effective)
NSI1303D21	±250mV	22kΩ		
NSI1303D02	±50mV	4.9kΩ	20MHz	
NSI1303D22	±250mV	22kΩ		

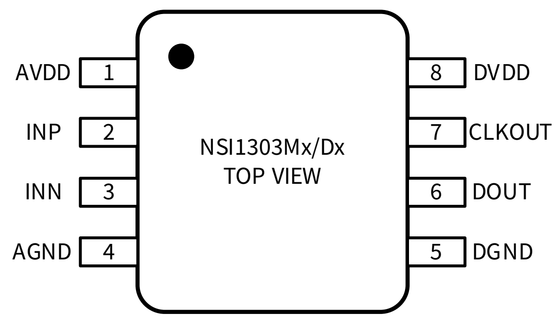


Figure 1.1 NSI1303Mx/Dx Package (SOP8(300mil))

Table 1.2 NSI1303 Pin Configuration and Description (SOP8(300mil))

NSI1303M/Dx PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1303x2x and ±50mV recommended for NSI1303x0x)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	DGND	Digital ground reference
6	DOUT	Modulator data output
7	CLKOUT	Modulator clock output, 10 MHz (on NSI1303M/Dx1) or 20 MHz (on NSI1303M/Dx2) nominal
8	DVDD	Power supply for digital side (3.0V to 5.5V)

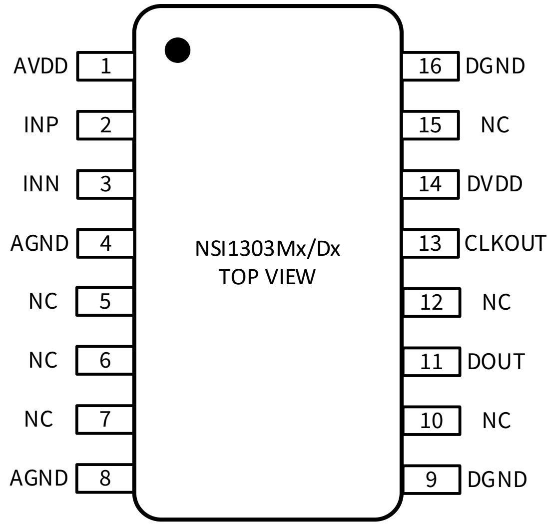


Figure 1.2 NSI1303Mx/Dx Package (SOP16(300mil))

Table 1.3 NSI1303M/Dx Pin Configuration and Description (SOP16(300mil))

NSI1303M/Dx PIN NO.	SYMBOL	FUNCTION
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1303x2x and ±50mV recommended for NSI1303x0x)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
6	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
7	NC	Internally connected to AVDD, this pin can be left floating or tied to AVDD
8	AGND	Analog ground reference
9	DGND	Digital ground reference
10	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
11	DOUT	Modulator data output
12	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
13	CLKOUT	Modulator clock output, 10 MHz (on NSI1303M/Dx1) or 20 MHz (on NSI1303M/Dx2) nominal
14	DVDD	Power supply for digital side (3.0V to 5.5V)
15	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
16	DGND	Digital ground reference

2. Absolute Maximum Ratings(1)

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage(2)	AVDD, DVDD	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Digital Output Voltage	DOUT, CLKOUT	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	Io	-10		10	mA
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃

(1) The device cannot operate beyond the listed Absolute Maximum Ratings to prevent permanent device damage. The device is not fully functional if operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings. Long-time stress of the absolute maximum conditions may affect the device lifetime.

(2) VDD1 to GND1, VDD2 to GND2

3. ESD Ratings(1)

Parameters	Test condition	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Analog Side Power Supply		AVDD	3.0	5.0	5.5	V
Digital Side Power Supply		DVDD	3.0	3.3	5.5	V
NSI1303x01/2	Differential input voltage before clipping output	$V_{Clipping}$		±64		mV
	Linear differential input full scale voltage	V_{FSR}	-50		50	mV
	Operating common-mode input voltage	V_{CM}	-0.032		0.8	V
NSI1303x21/2	Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
	Linear differential input full scale voltage	V_{FSR}	-250		250	mV
	Operating common-mode input voltage	V_{CM}	-0.16		0.8	V
Operating Ambient Temperature		T_A	-40		125	℃

5. Thermal Information

Parameters	Symbol	SOP8(300mil)	SOP16(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{θJA}$	86	82	℃/W
Junction-to-case (top) thermal resistance	$R_{θJC(top)}$	28	42	℃/W
Junction-to-board thermal resistance	$R_{θJB}$	42	46	℃/W
Junction–to-top characterization parameter	$Ψ_{JT}$	4	12	℃/W
Junction-to-board characterization parameter	$Ψ_{JB}$	42	46	℃/W

6. Specifications

6.1. Electrical Characteristics: NSI1303M/D0x

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = AGND = 0V, T_A = -40℃ to 125℃ and $sinc^3$ filter with OSR=256. Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.3	14.8	mA	for M/D01
			11.5	15	mA	for M/D02
Digital Side Supply Current	IDVDD		2.6		mA	for M/D01, C_{LOAD}=15pF
			3.7		mA	for M/D02, C_{LOAD}=15pF
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-95		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min}$ ≤ VIN ≤ $V_{CM\ max}$
	$CMRR_{ac}$		-99		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min}$ ≤ VIN ≤ $V_{CM\ max}$
Input capacitance	C_{IN}		2		pF	INN=AGND
Single-ended input resistance	R_{IN}		4.75		kΩ	INN = AGND
Differential input resistance	R_{IND}		4.9		kΩ	
Input bias current	I_{IB}	-26	-23	-20	μA	INP = INN = AGND, I_{IB} = (I_{IBP} + I_{IBN}) / 2

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input bias current drift	TCI_{IB}		±2		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/µs	Common-mode transient immunity
Input bandwidth	BW		800		kHz	
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	V_{OS}	-50	±2.5	50	µV	INP = INN = AGND
Offset error thermal drift	TCV_{OS}	-0.5	±0.15	0.5	µV/°C	
Gain error	E_G	-0.2%	±0.005%	0.2%		
Gain error thermal drift	TCE_G	-30	±10	30	ppm/°C	
Power supply rejection ratio	PSRR		-100		dB	PSRR vs AVDD, at DC
			-90		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR		84		dB	f_{IN} = 1kHz for M/D01
			83		dB	f_{IN} = 1kHz for M/D02
Signal to noise and distortion	SINAD		82.5		dB	f_{IN} = 1kHz
Total harmonic distortion	THD		-97		dB	f_{IN} = 1kHz
Spurious-free dynamic range	SFDR		96		dB	f_{IN} = 1kHz for M/D01
			97		dB	f_{IN} = 1kHz for M/D02
Digital Input / Output						
Output load capacitance	C_{LOAD}		30		pF	
High-level output voltage	V_{OH}	DVDD-0.1			V	I_{OH} = -20µA
		DVDD-0.4			V	I_{OH} = -4mA
		DVDD-0.8				I_{OH} = -8mA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 20µA
				0.4	V	I_{OL} = 4mA
				0.8	V	I_{OL} = 8mA

6.2. Electrical Characteristics: NSI1303M/D2x

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = AGND = 0V, T_A = -40℃ to 125℃ and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.2	14.3	mA	for M/D21
			11.7	15.1	mA	for M/D22
Digital Side Supply Current	IDVDD		2.6	4.5	mA	for M/D21, CLOAD=15pF
			3.7		mA	for M/D22, CLOAD=15pF
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-106		dB	INP = INN, fIN = 0 Hz, VCM min ≤ VIN ≤ VCM max
	$CMRR_{ac}$		-104		dB	INP = INN, fIN = 10 kHz, VCM min ≤ VIN ≤ VCM max
Input capacitance	C_{IN}		2		pF	INN=AGND
Single-ended input resistance	R_{IN}		19		kΩ	INN = AGND
Differential input resistance	R_{IND}		22		kΩ	
Input bias current	I_{IB}	-24	-18	-12	µA	INP = INN = AGND, IIB = (IIBP + IIBN) / 2
Input bias current drift	TCI_{IB}		±1		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/µs	Common-mode transient immunity
Input bandwidth	BW		800		kHz	
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	V_{OS}	-100	±2.5	100	µV	INP = INN = AGND
Offset error thermal drift	TCV_{OS}	-1	±0.15	1	µV/°C	
Gain error	E_G	-0.2%	±0.005%	0.2%		

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Gain error thermal drift	TCE_G	-40	±20	40	ppm/°C	
Power supply rejection ratio	PSRR		-106		dB	PSRR vs AVDD, at DC
			-95		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR		85		dB	fIN = 1kHz for M/D21
			84.5		dB	fIN = 1kHz for M/D22
Signal to noise and distortion	SINAD		82.5		dB	fIN = 1kHz
Total harmonic distortion	THD		-90	-82	dB	fIN = 1kHz for M/D21
			-95	-82	dB	fIN = 1kHz for M/D22
Spurious-free dynamic range	SFDR		90		dB	fIN = 1kHz for M/D21
			92		dB	fIN = 1kHz for M/D22
Digital Input / Output						
Output load capacitance	C_{LOAD}		30		pF	
High-level output voltage	V_{OH}	DVDD-0.1			V	IOH = -20µA
		DVDD-0.4			V	IOH = -4mA
		DVDD-0.8				IOH = -8mA
Low-level output voltage	V_{OL}			0.1	V	IOL = 20µA
				0.4	V	IOL = 4mA
				0.8	V	IOL = 8mA

6.3. Timing Characteristics

Unless otherwise noted, Typical values are at AVDD = 5V, DVDD = 3.3V, T_A = 25℃.Over operating ambient temperature range (unless otherwise noted)

PARAMETERS	Symbol	MIN	TYP	MAX	Unit	Comments
clock frequency	f_{CLK}	9.6	10	10.4	MHz	For NSI1303xx1
		19.2	20	20.8	MHz	For NSI1303xx2
Duty Cycle	Duty	45%	50%	55%		For NSI1303M/Dx
DOUT rising time	t_R		1.8	3.5	ns	C_{LOAD} = 15pF
DOUT falling time	t_F		1.8	3.5	ns	C_{LOAD} = 15pF
DOUT hold time after rising edge of CLKOUT	t_H	7	10		ns	For NSI1303M/Dx, C_{LOAD} = 15pF

PARAMETERS	*Symbol*	*MIN*	*TYP*	*MAX*	*Unit*	*Comments*
Rising edge of CLKOUT to DOUT valid delay	t_D		11	15	ns	For NSI1303M/Dx, C_{LOAD} = 15pF
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

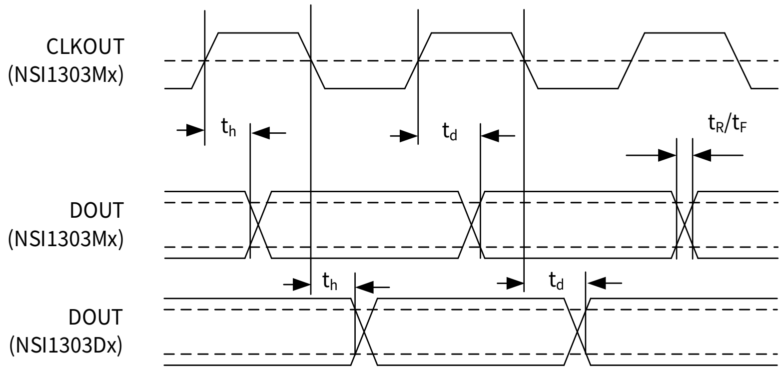


Figure 6.1 NSI1303x digital interface timing

6.4. Typical Performance Characteristics

Unless otherwise noted, test at AVDD = 5V, DVDD = 3.3V, Vin = -250mV to 250mV (NSI1303x2x) or -50mV to 50mV (NSI1303x0x), and sinc^3 filter with OSR=256.

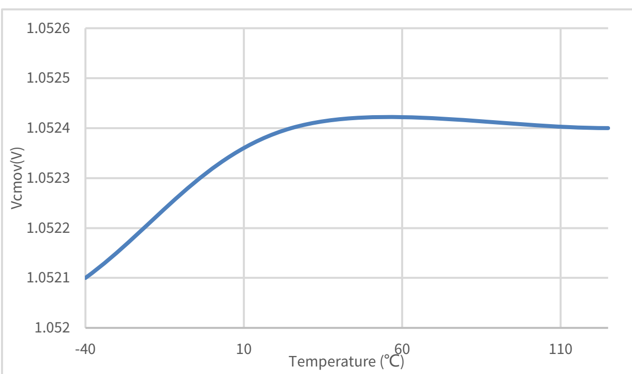


Figure 6.2 Common-Mode Overvoltage Detection Level vs Temperature

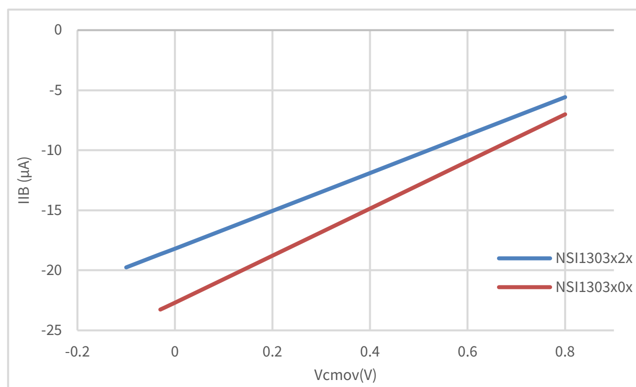


Figure 6.4 Input Bias Current vs Common-Mode voltage

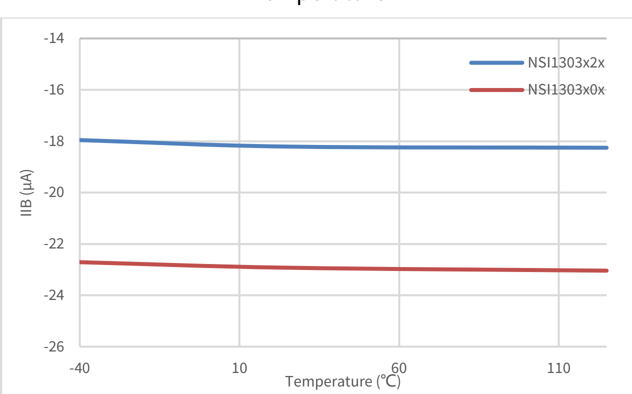


Figure 6.3 Input Bias Current vs Temperature

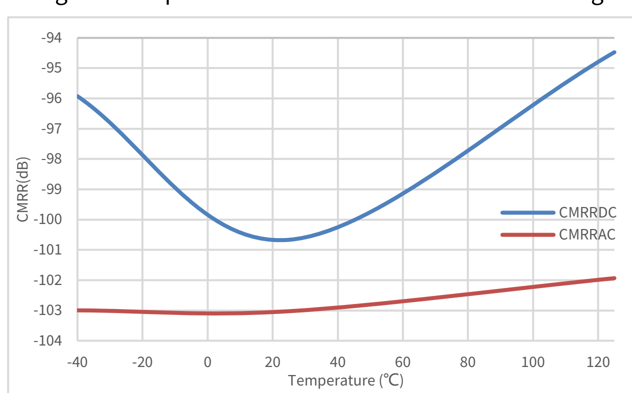


Figure 6.5 Common-Mode Rejection Ratio vs Temperature

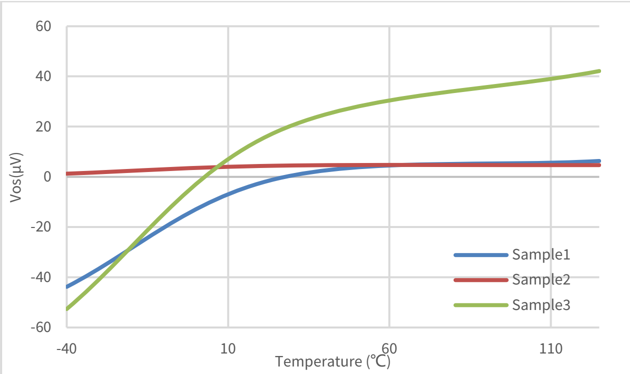


Figure 6.6 Input Offset Voltage vs Temperature

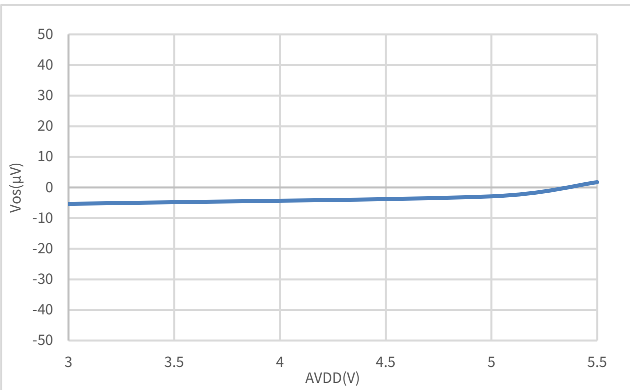


Figure 6.7 Input Offset Voltage vs Analog Side Supply Voltage

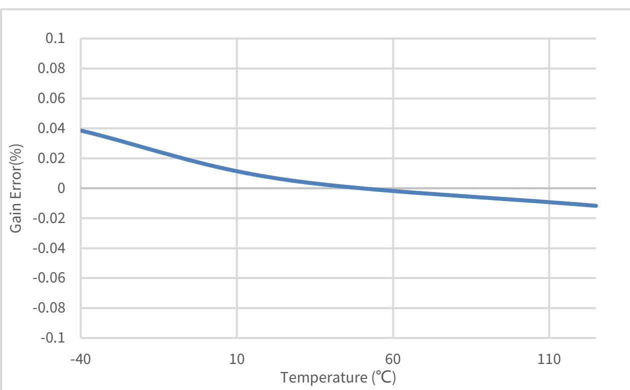


Figure 6.8 Gain Error vs Temperature

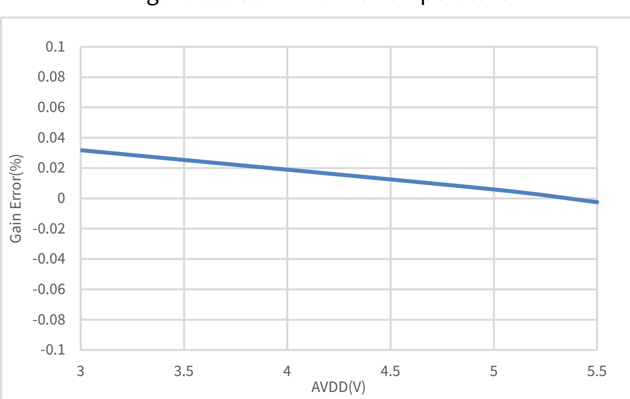


Figure 6.9 Gain Error vs Analog Side Supply Voltage

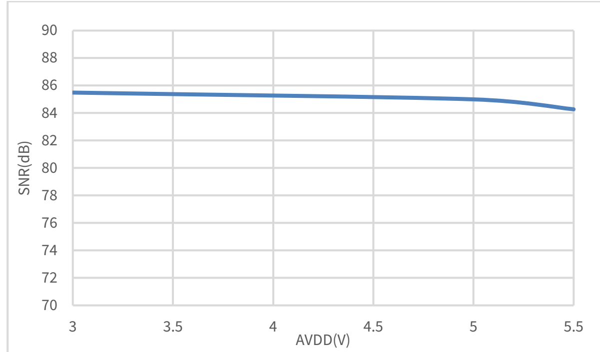


Figure 6.10 Signal-to-Noise Ratio vs Analog Side Supply Voltage

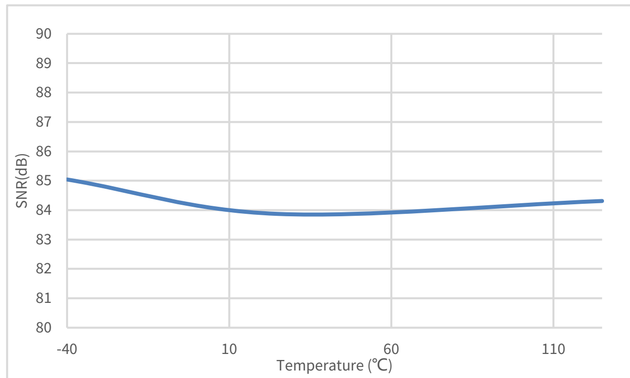


Figure 6.11 Signal-to-Noise Ratio vs Temperature

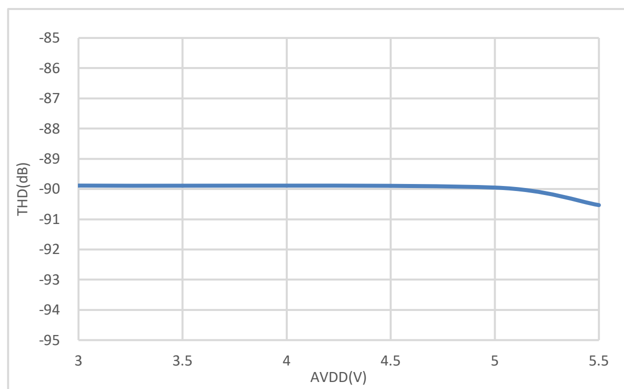


Figure 6.12 Total Harmonic Distortion vs Analog Side Supply Voltage

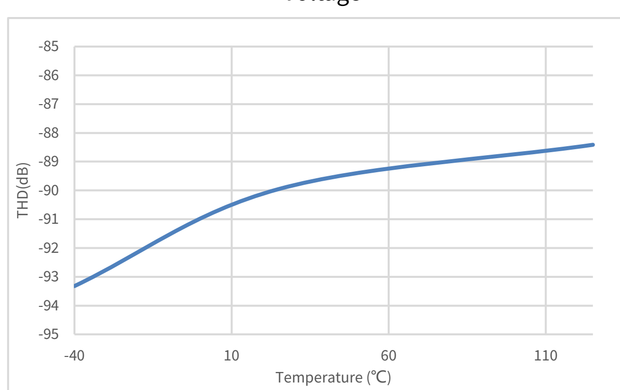


Figure 6.13 Total Harmonic Distortion vs Temperature

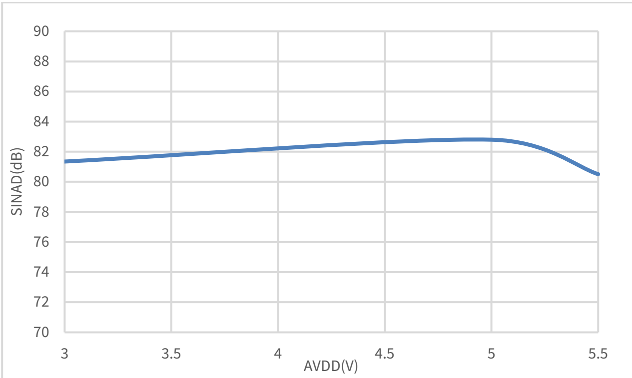


Figure 6.14 Signal-to-Noise + Distortion vs Analog Side Supply Voltage

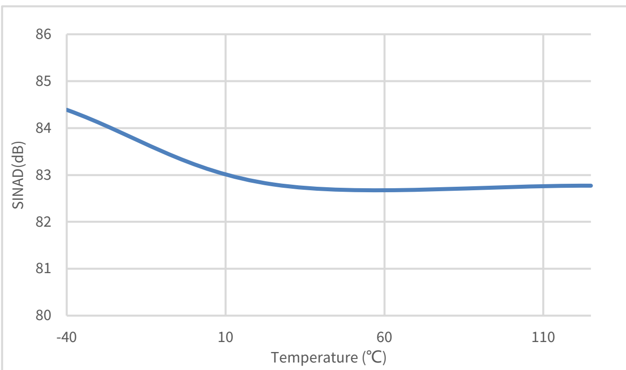


Figure 6.15 Signal-to-Noise + Distortion vs Temperature

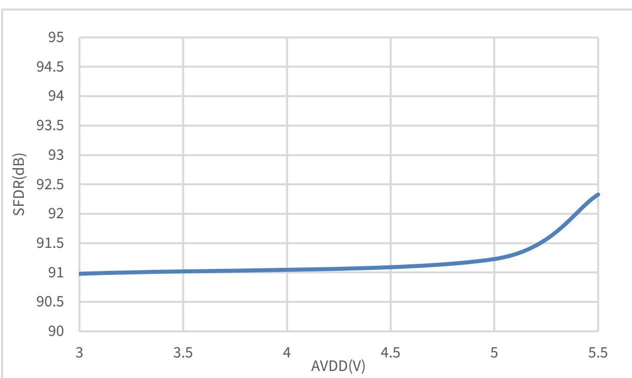


Figure 6.16 Spurious-Free Dynamic Range vs Analog Side Supply Voltage

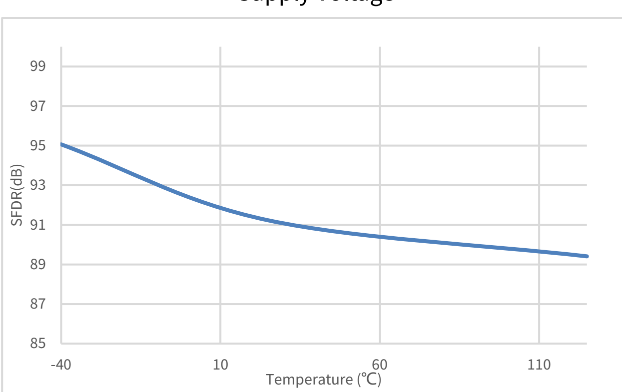


Figure 6.17 Spurious-Free Dynamic Range vs Temperature

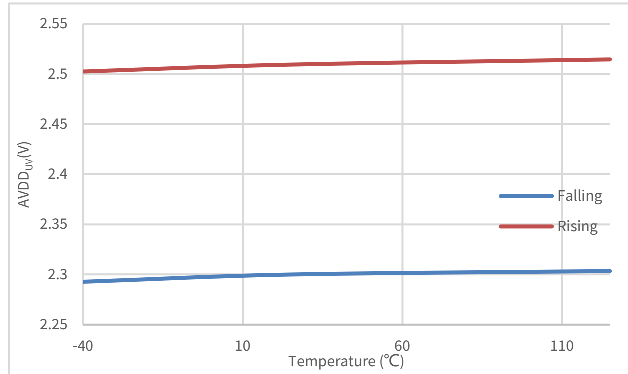


Figure 6.18 Analog Side Under-Voltage Detection Level vs Temperature

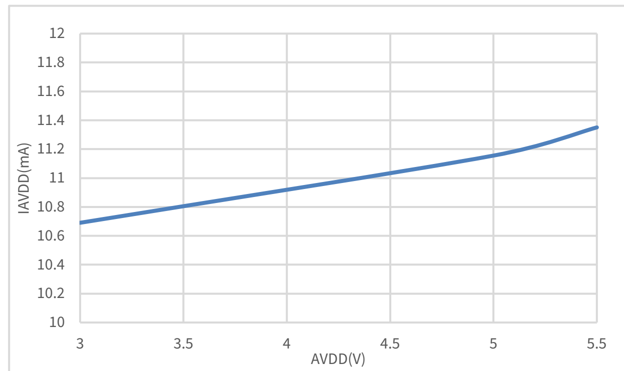


Figure 6.19 Analog Side Supply Current vs Supply Voltage

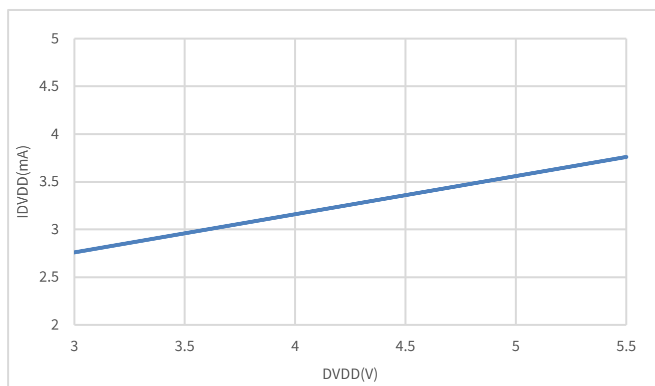


Figure 6.20 Digital Side Supply Current vs Supply Voltage

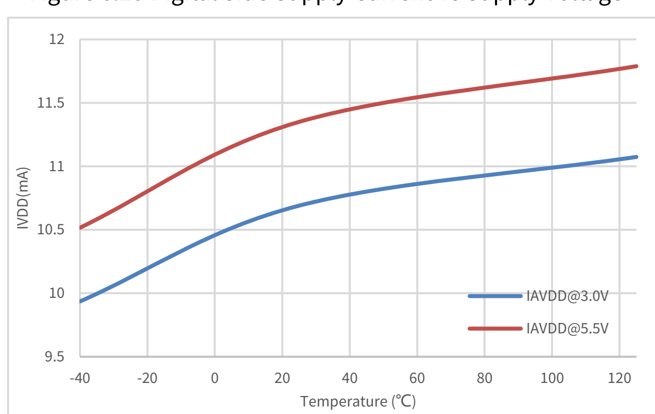


Figure 6.21 Supply Current vs Temperature

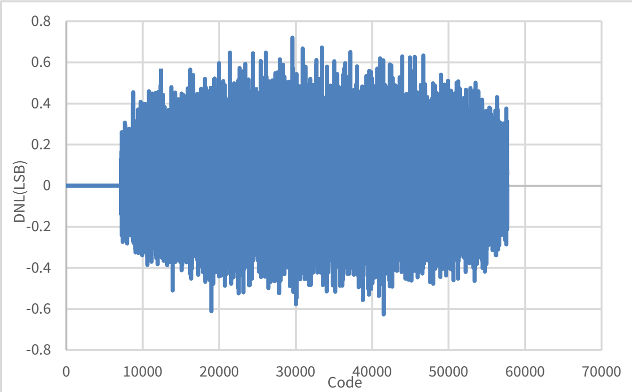


Figure 6.22 Typical Differential Nonlinearity

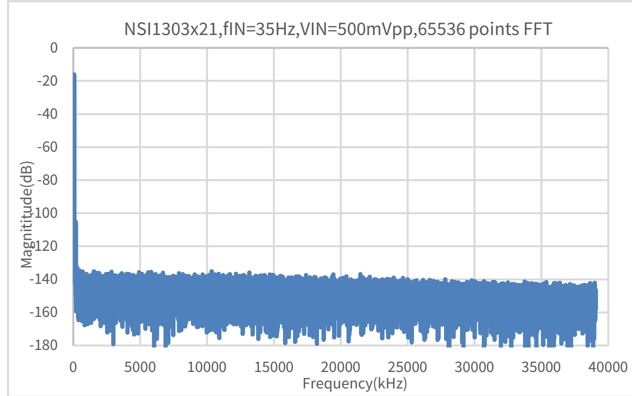


Figure 6.24 Frequency Spectrum

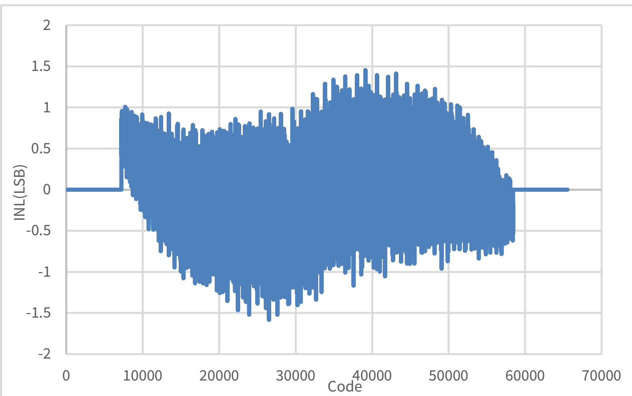


Figure 6.23 Typical Integral Nonlinearity

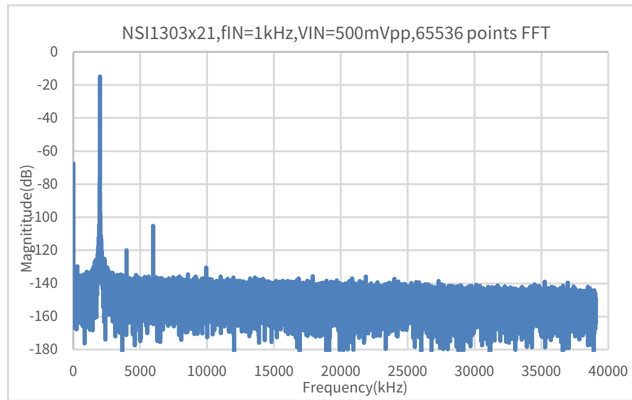


Figure 6.25 Frequency Spectrum

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III

Description	Test Condition	Value
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value SOW8	Value SOW16	Unit
DIN EN IEC 60747-17 (VDE 0884-17)					
Maximum repetitive isolation voltage		V_{IORM}	2121	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC Voltage		2121	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s				
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd (m)}$=1.875*V_{IORM}, t_m=1s（method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)				
Maximum transient isolation voltage	t = 60sec	V_{IOTM}	8000	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	10000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	$>10^{9}$	$>10^{9}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	1.2	1.2	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	1453	1524	mW
Safety input, output, or supply current	θ_{JA} = 137.7℃/W for SOP8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Is	/	/	mA
	θ_{JA} = 86℃/W for SOW8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃		264	277	mA

Description	Test Condition	Symbol	Value		Unit
			SOW8	SOW16	
Maximum safety temperature		Ts	150	150	℃
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	5000	5000	V_{RMS}

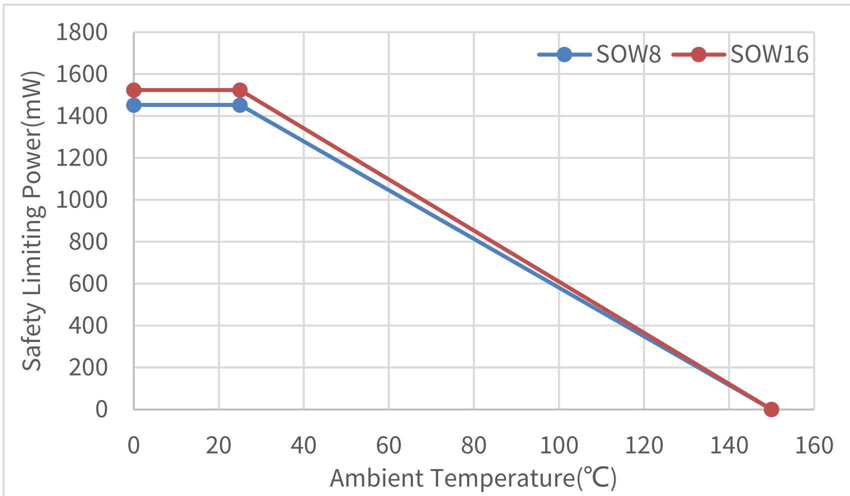


Figure 7.1 NSI1303 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Regulatory Information

The NSI1303 are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121 V_{PEAK} V_{IOTM}=8000 V_{PEAK} V_{IOSM}=10000 V_{PEAK}	Reinforced insulation
Certificate No.E500602	Certificate No.E500602	40052820	CQC20001264938 for SOW8 CQC20001264939 for SOW16

8. Function Description

8.1. Overview

The NSI1303 is a high performance isolated modulator that accept fully-differential input with internal clock. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream that is synchronous to the internally-generated clock at the CLKOUT pin. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier, as shown in the Functional Block Diagram. The extended clock frequency of 20 MHz on the NSI1303xx2 supports faster control loops and higher performance levels compared to the other solutions available on the market. NSI1303 meets the requirements of different sampling edge in the external digital system, clock rising edge effective for NSI1303Mx and clock falling edge effective for NSI1303Dx.

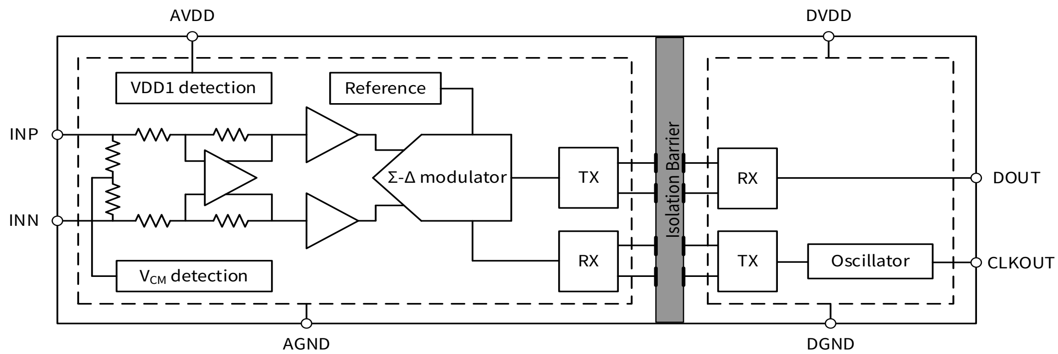


Figure 8.1 Function Block Diagram of NSI1303Mx/NSI1303Dx

8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

8.3. Digital Output

The digital output provides a stream of ones and zeros that can accurately represent the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 250mV input signal (for the NSI1303x2x), the modulator outputs a bitstream with 89.06% high time. For a -250mV input signal (for the NSI1303x2x), the modulator outputs a bitstream with 10.94% high time.

If the input signal is greater than or equal to 320mV (64 mV for the NSI1303x0x), the modulator clips with a steam of all ones. If the input signal is less than or equal to -320mV (–64 mV for the NSI1303x0x), the output of the modulator clips with a stream of all zeros. In this case, however, the NSI1303 generates a single 0 (if the input is at positive full-scale) or 1 every 128 clock cycles to indicate proper device function (see section8.4 for more details).

Figure 8.2 shows the data output vs isolated modulator input voltage.

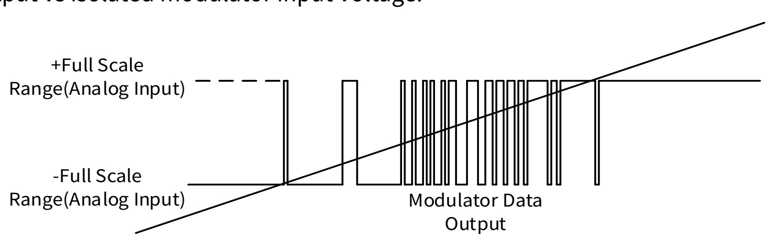


Figure 8.2 Data output vs input voltage

Within full-scale input range, Equation 1 calculates the ones and zeros density of output bitstream for input voltage:

$$Density = (V_{IN}+V_{CLIPPING})/(2*V_{CLIPPING}) \quad \text{Equation 8.1}$$

Besides the data output signal at the DOUT pin, the NSI1303M/Dx also provides clock signal at the CLKOUT pin. See the Timing Characteristics in section 5.3 for more details.

8.4. Fail-safe Output

NSI1303 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe function will be activated in following conditions:

- When the undervoltage of AVDD is detected (AVDD< $AVDD_{UV}$), DOUT pin output a uncoded bitstream of all logic zeros, as shown in Figure 8.3 and Figure 8.4.
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}), DOUT pin output a uncode bitstream of all logic ones, as shown in Figure 8.3 and Figure 8.4.

NOTE: If both of the faults above occur at the same time, DOUT pin output a uncode bitstream of all logic zeros. (AVDD missing has a higher priority).

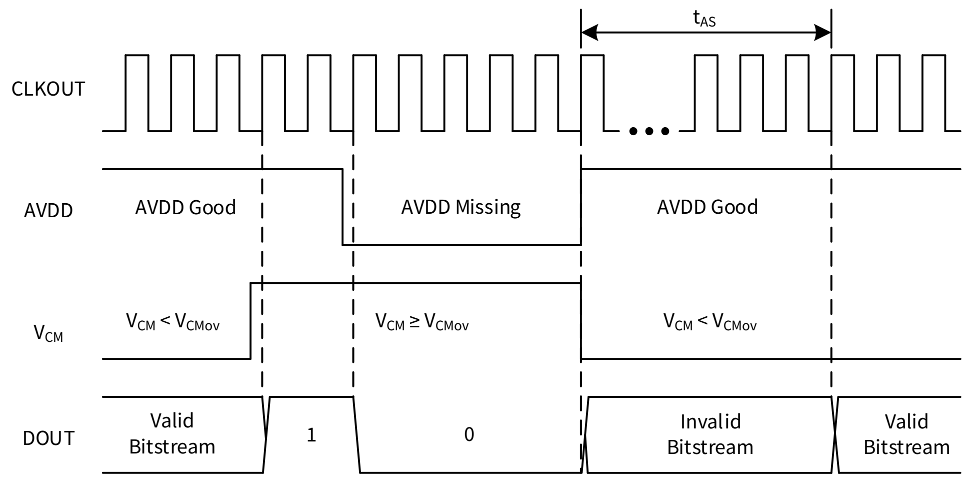


Figure 8.3 Fail-safe Bitstream Output of NSI1303Mx

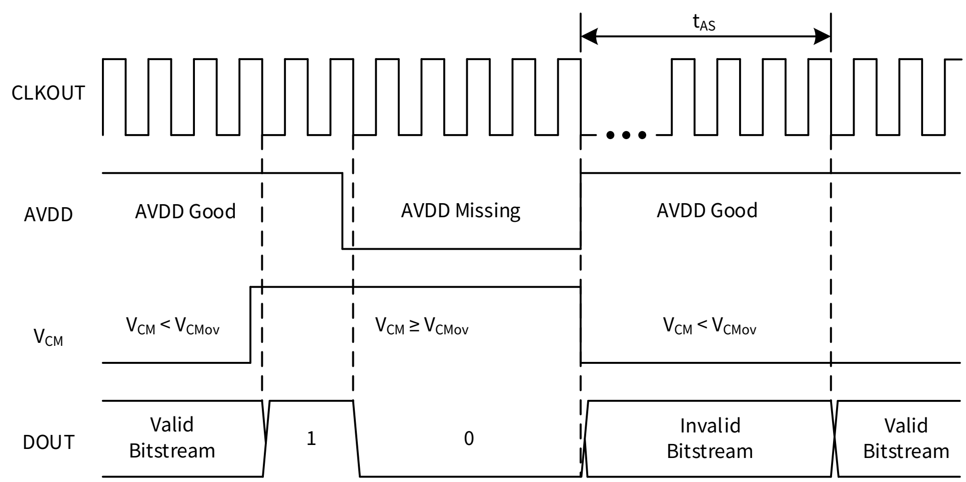


Figure 8.4 Fail-safe Bitstream Output of NSI1303Dx

If an overrange input signal is applied to the NSI1303 (V_{IN} ≥ $V_{Clipping}$), the output generates a single 0 or 1 every 128 bits at DOUT, as shown in Figure 8.5 and Figure 8.6.

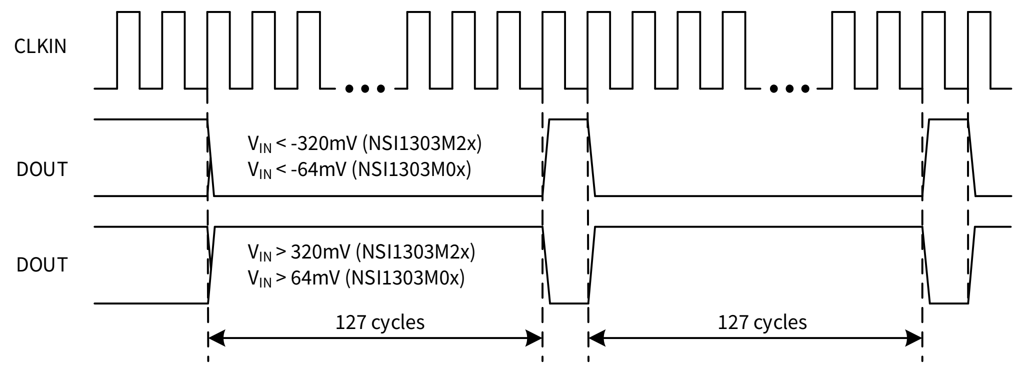


Figure 8.5 Overrange Bitstream Output of NSI1303Mx

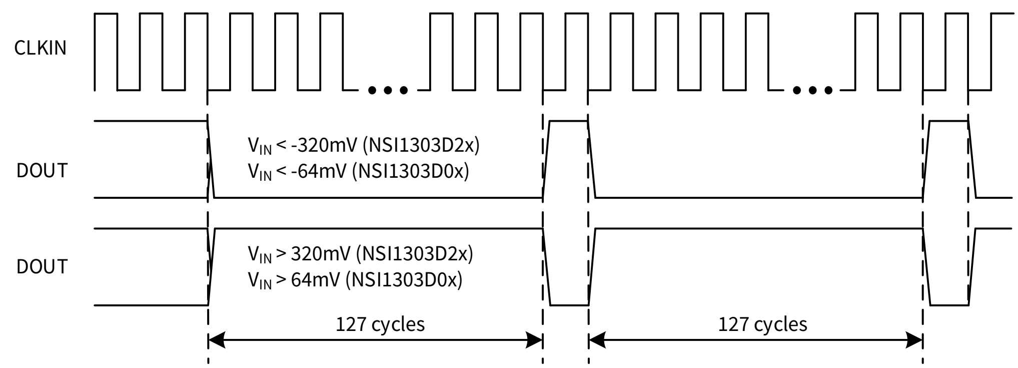


Figure 8.6 Overrange Bitstream Output of NSI1303Dx

9. Application Note

9.1. Typical Application Circuit

NSI1303 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 9.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1303 through a RC filter. The internal second-order sigma-delta modulator converts the analog input to a single-bit output stream. The CLKOUT pin outputs the internally generated clock, which is synchronized with the output bit-stream. The external digital system receives the clock signal and provides a digital filter for decimation and quantization noise filtering. NSI1303 is suitable for both rising and falling edge sampling, clock rising edge effective for NSI1303Mx and clock falling edge effective for NSI1303Dx.

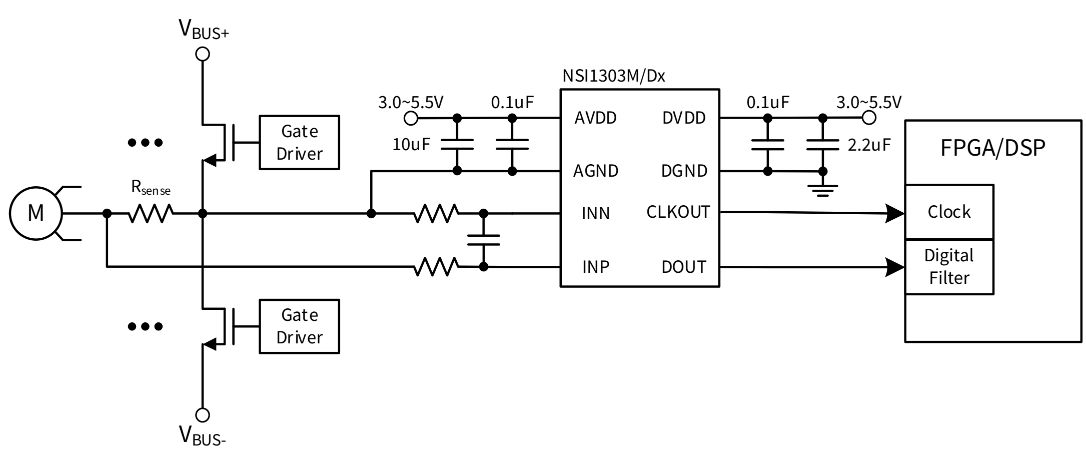


Figure 9.1 Typical application circuit of NSI1303M/Dx in phase current sensing

9.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq$ FSR.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

9.3. Digital Filter

The Σ-Δ modulator has characteristics of noise shaping. Most of the quantization noise is pushed from a low frequency to a higher frequency.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \qquad \text{Equation 9.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 9.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR}\frac{(1-Z^{-DR})}{(1-Z^{-1})}\right)^{N} \qquad \text{Equation 9.2}$$

where:

DR is the decimation rate;

N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 9.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \qquad \text{Equation 9.3}$$

The filter characteristics for a third-order sinc filter are summarized in Table 9.1.

Table 9.1 Sinc3 Filter Characteristics for 20 MHz CLKIN

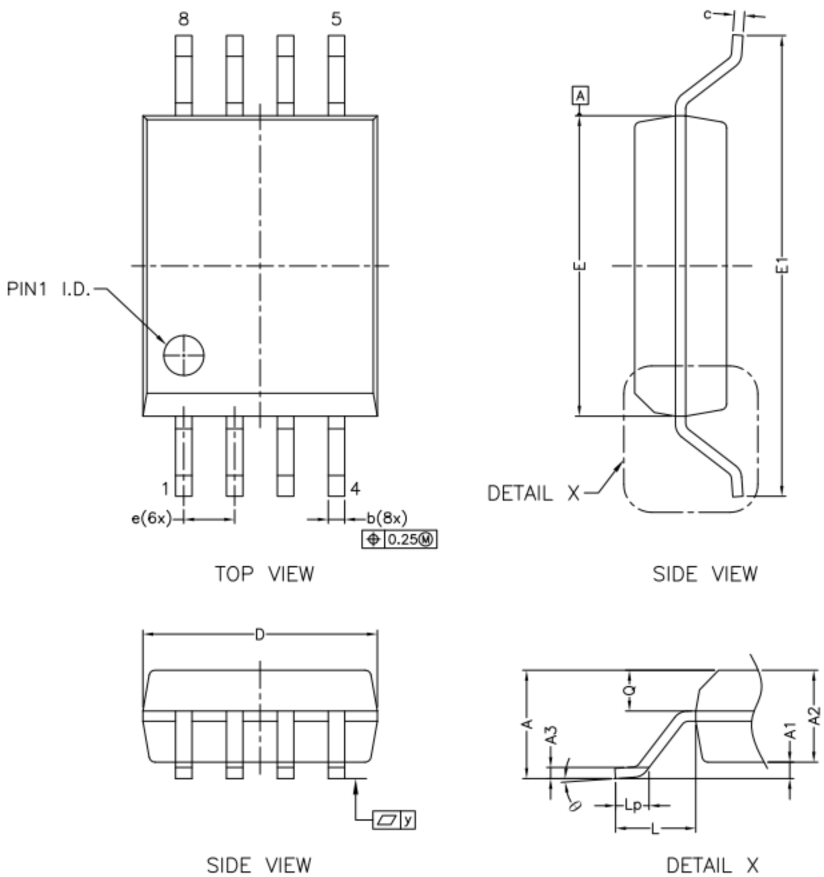
Decimation Rate (DR)	Data Output Rate (kHz)	Data Size (bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

9.4. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1303 requires a 0.1µF bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10µF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1303. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1303. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

10. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

Figure 10.1 SOW8 Package Shape and Dimension in millimeters

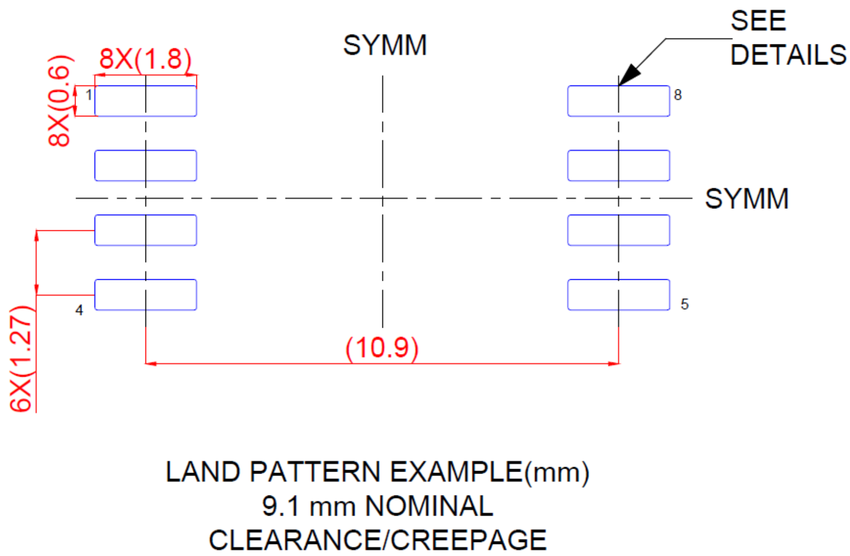
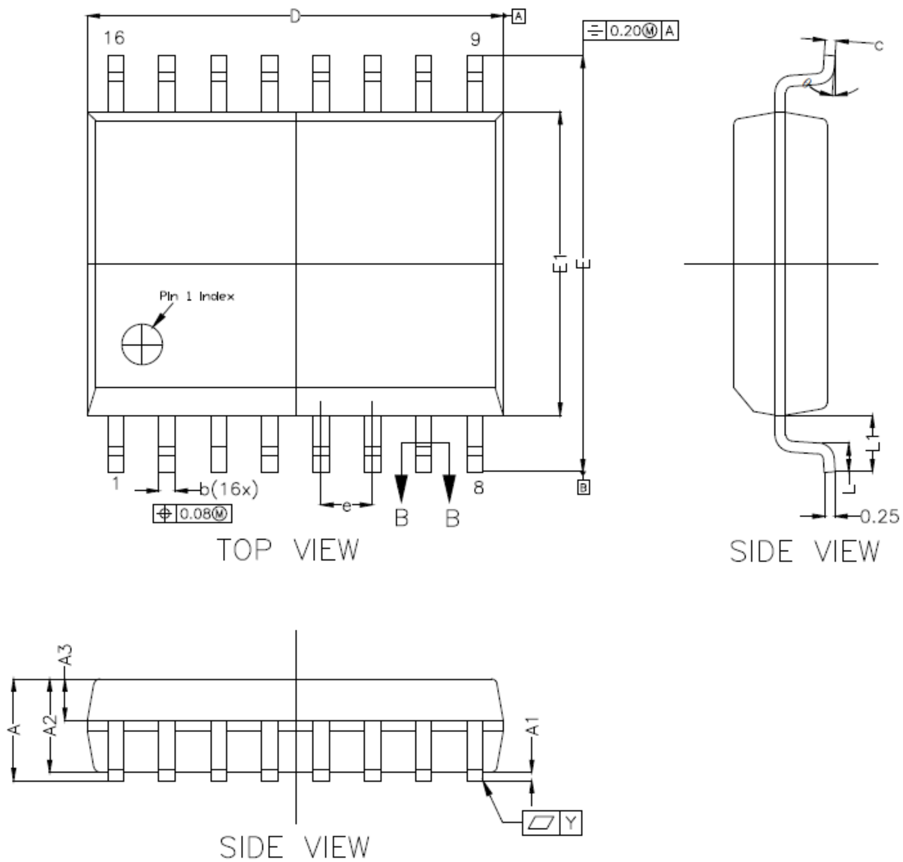


Figure 10.2 SOW8 Package Board Layout Example



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.3 SOW16 package shape and dimension in millimeters

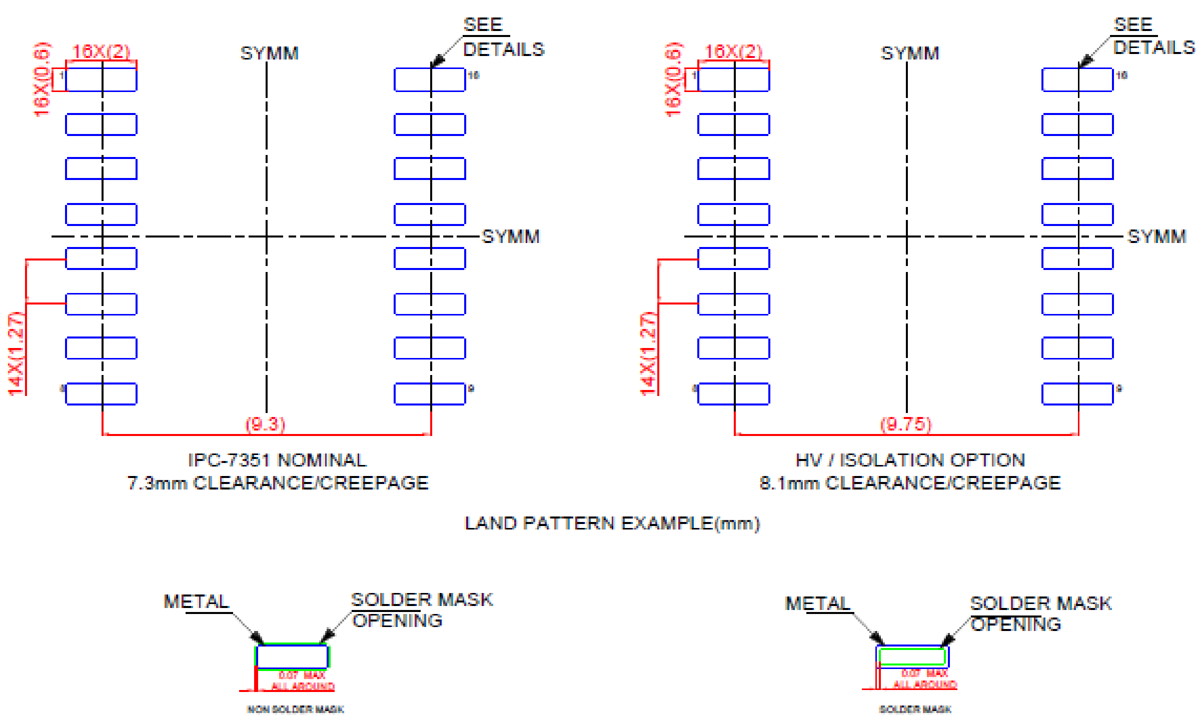


Figure 10.4 SOW16 Package Board Layout Example

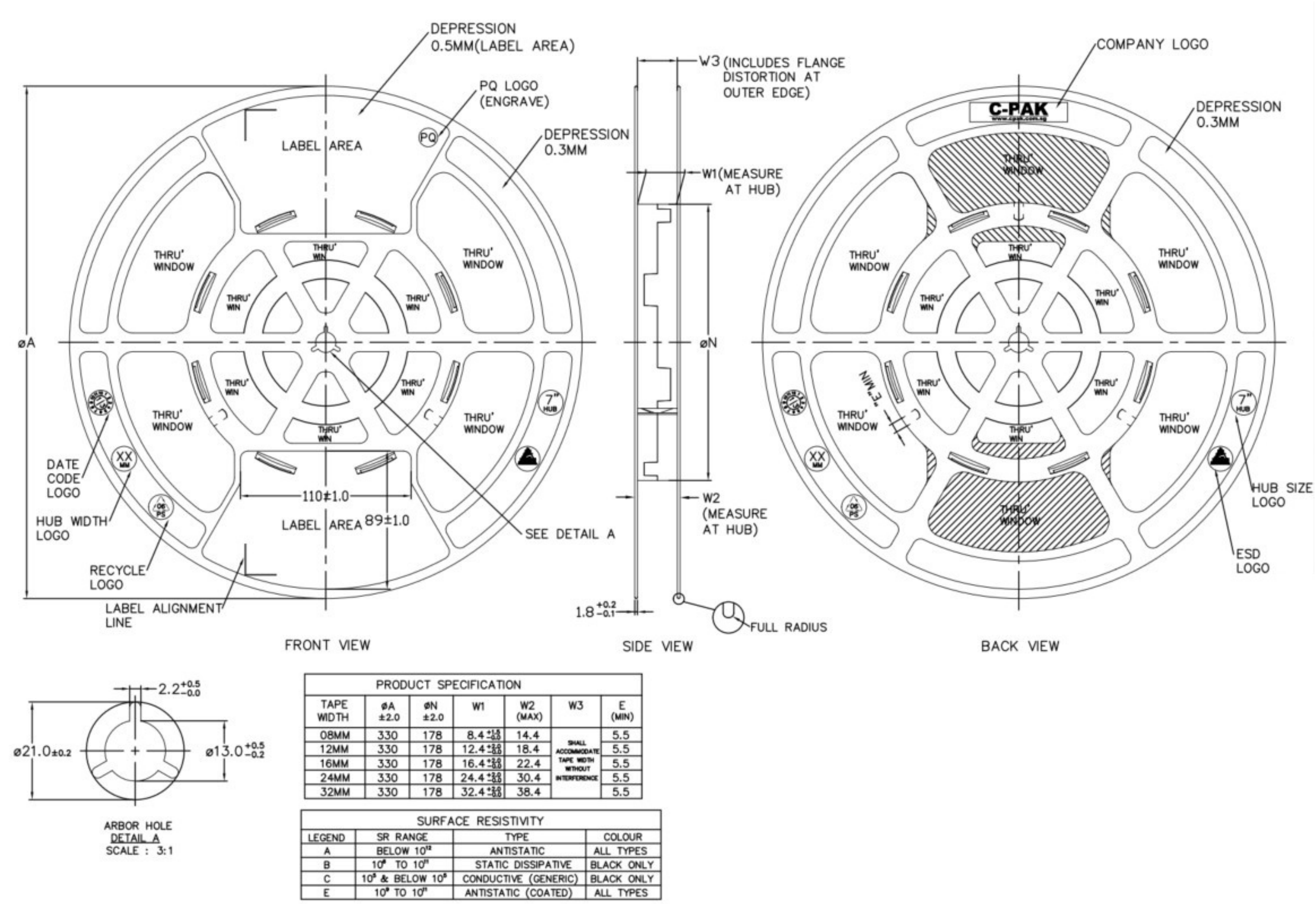
11. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI1303M01-DSWVR	5	-50 ~ 50	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303M21-DSWVR	5	-250 ~ 250	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303M02-DSWVR	5	-50 ~ 50	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303M22-DSWVR	5	-250 ~ 250	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303D01-DSWVR	5	-50 ~ 50	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303D21-DSWVR	5	-250 ~ 250	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303D02-DSWVR	5	-50 ~ 50	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303D22-DSWVR	5	-250 ~ 250	Level-3	-40 to 125℃	No	SOP8 (300mil)	SOW8	1000
NSI1303M01-DSWR	5	-50 ~ 50	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303M21-DSWR	5	-250 ~ 250	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303M02-DSWR	5	-50 ~ 50	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303M22-DSWR	5	-250 ~ 250	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303D01-DSWR	5	-50 ~ 50	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303D21-DSWR	5	-250 ~ 250	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303D02-DSWR	5	-50 ~ 50	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000
NSI1303D22-DSWR	5	-250 ~ 250	Level-2	-40 to 125℃	No	SOP16 (300mil)	SOW16	1000

12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI1303	Click here	Click here	Click here	Click here

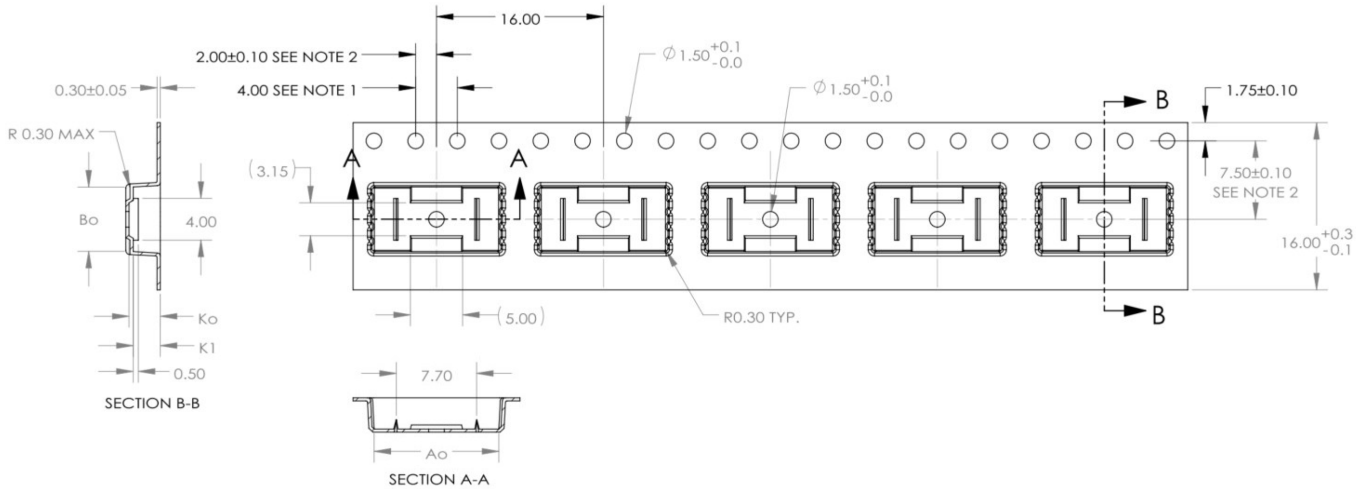
13. Tape and Reel Information

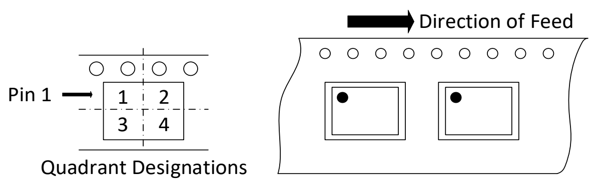


PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 $^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 $^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	16.4 $^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	24.4 $^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	32.4 $^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{3} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

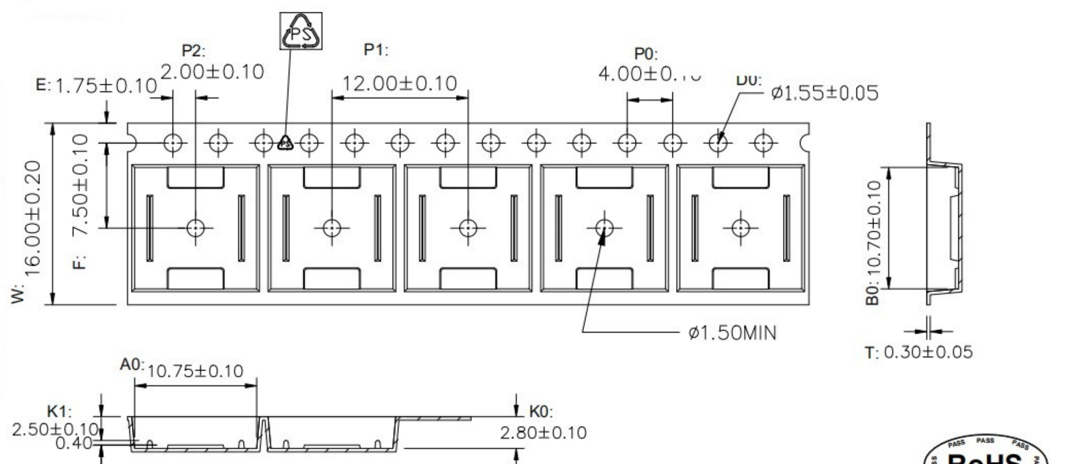
Figure 13.1 Tape Information





	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

Figure 13.2 Reel Information of SOP8(300mil)



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122）
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :$10^5 \sim 10^{10}\Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

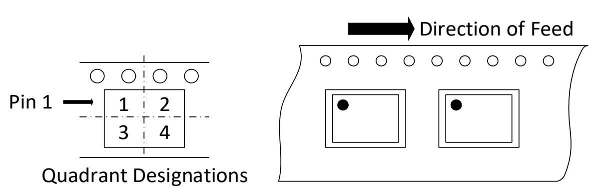


Figure 13.3 Reel Information of SOP16(300mil)

14. Revision History

Revision	Description	Date
1.0	Initial Release	2023/2/9
1.1	● Updated the standard in Safety Regulatory Approvals; ● Corrected the HBM rating from ±24000V to ±2000V in Section. 3; ● Updated Insulation voltage per UL of SOW8 from 3000V V_{RMS} to 5000V V_{RMS} in Section. 7.2; ● Updated Figure10.2 SOW8 Package Board Layout Example in Section. 10.	2024/6/13

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products and technologies, please contact Novosense (www.novosns.com).

Suzhou Novosense Microelectronics Co., Ltd